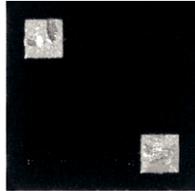


NiCr Thin Film, Top-Contact Resistor



Product may not be to scale

FEATURES

- Chip size: 20 inches square
- Resistance range: 10 Ω to 510 kΩ
- Resistor material: nichrome
- Oxidized silicon substrate
- 250 mW power

The SFN series resistor chips offer a combination of nichrome stability, good power rating and small size.

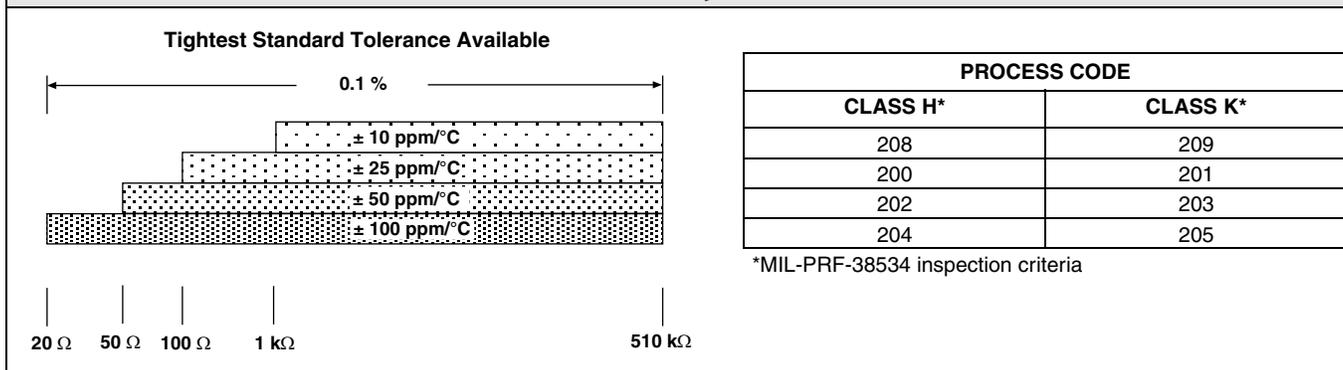
The SFNs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The SFNs are 100 % electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

Vishay EFI SFN resistor chips are widely used in hybrid packages where space is limited. Designed with capacity to handle substantial power loads, they also have the benefit of nichrome stability.

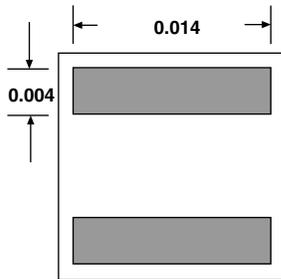
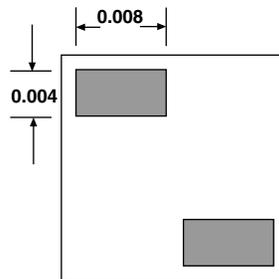
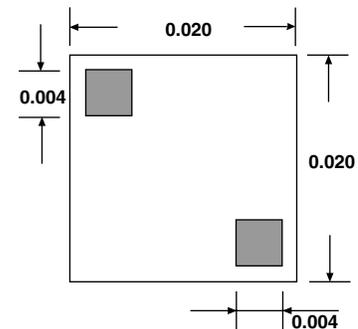
Recommended for hermetic environments where die is not exposed to moisture.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308 100 Ω - 250 kΩ < 100 Ω or > 251 kΩ	- 35 dB typical - 20 dB typical
Stability, 1000 hours, + 125 °C, 50 mW	± 0.25 % maximum ΔR/R
Operating temperature range	- 55 °C to + 125 °C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25 % maximum ΔR/R
High temperature exposure, + 150 °C, 100 hours	± 0.5 % maximum ΔR/R
Dielectric voltage breakdown	200 V
Insulation resistance	10 ¹² minimum
Operating voltage	100 V maximum
DC power rating at + 70 °C (derated to zero at + 175 °C)	250 mW
5 x rated power short-time overload, + 25 °C, 5 seconds	± 0.25 % maximum ΔR/R

DIMENSIONS in inches

TYPICAL RANGE
 10 Ω - 55 Ω

TYPICAL RANGE
 56 Ω - 7.4 kΩ

TYPICAL RANGE
 7.5 kΩ - 510 kΩ

SCHEMATIC


MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.020 x 0.020 ± 0.003 (0.51 x 0.51 ± 0.05 mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05 mm)
Chip substrate material	Oxidized silicon, 10 kÅ minimum SiO ₂
Resistor material	Nichrome (Passivation Optional)
Bonding pad size	0.004 x 0.004 (0.10 x 0.10 mm)
Number of pads	2
Pad material	15 kÅ minimum Gold
Backing	None, lapped semiconductor silicon; Au back optional

OPTIONS: Aluminum Pads
 Passivation (thermal set plastic)
 Consult Applications Engineer

ORDERING INFORMATION					
Example: 100 % visual, 10 kΩ, ± 1 %, ± 50 ppm/°C TCR, Gold Pads, Class H Visual inspection					
W	SFN	202	1000	1	F
INSPECTION/ PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100 % visually inspected parts in matrix tray per MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4 % AQL)		See Process Code Table	Use the first 4 significant digits of the resistance	B = 0.01 A = 0.1 0 = 1 1 = 10 2 = 100 3 = 1000 4 = 10 000	B = 0.1 % C = 0.2 % D = 0.5 % F = 1.0 % G = 2.0 % H = 2.5 % J = 5.0 % K = 10 %



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