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- **Members of the Texas Instruments** Widebus™ Family
- Inputs Are TTL-Voltage Compatible
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- Flow-Through Architecture Optimizes **PCB Layout**
- Distributed V_{CC} and GND Pin Configuration **Minimizes High-Speed Switching Noise**
- **EPIC™** (Enhanced-Performance Implanted CMOS) 1-um Process
- 500-mA Typical Latch-Up Immunity at
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center **Pin Spacings**

description

The 'ACT16646 are 16-bit bus transceivers consisting of D-type flip-flops and control circuitry with 3-state outputs arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The devices can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental busmanagement functions that can be performed with the bus transceivers and registers.

54ACT16646...WD PACKAGE 74ACT16646...DL PACKAGE (TOP VIEW)

_	Г	U		L —
1DIR	1	_	56	
1CLKAB [2		55] 1CLKBA
1SAB [3		54] 1SBA
GND [4		53] GND
1A1 [5		52] 1B1
1A2 [6		51] 1B2
V _{CC} [7		50] v _{cc}
1A3 [8		49] 1B3
1A4 [9		48] 1B4
1A5 [10		47] 1B5
GND [11		46] GND
1A6 [12		45] 1B6
1A7 [13		44] 1B7
1A8 [14		43] 1B8
2A1 [15		42] 2B1
2A2 [16		41] 2B2
2A3 [17		40] 2B3
GND [18		39] GND
2A4 [19		38] 2B4
2A5 [20		37] 2B5
2A6 [21		36] 2B6
V _{CC} [22		35] v _{cc}
2A7 [23		34] 2B7
2A8 [24		33] 2B8
GND [25		32] GND
2SAB [26		31] 2SBA
2CLKAB [27		30	2CLKBA
2DIR [28		29] 2 <mark>0E</mark>

Output-enable (OE) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when $\overline{\mathsf{OE}}$ is low. In the isolation mode ($\overline{\mathsf{OE}}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The 74ACT16646 is packaged in TI's shrink small-outline package, which provides twice the functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16646 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT16646 is characterized for operation from -40°C to 85°C.

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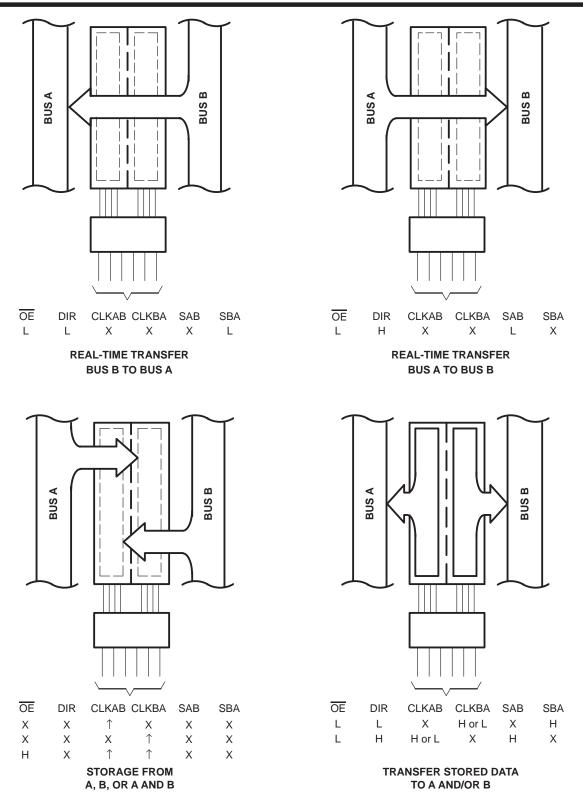


Figure 1. Bus-Management Functions



54ACT16646, 74ACT16646 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

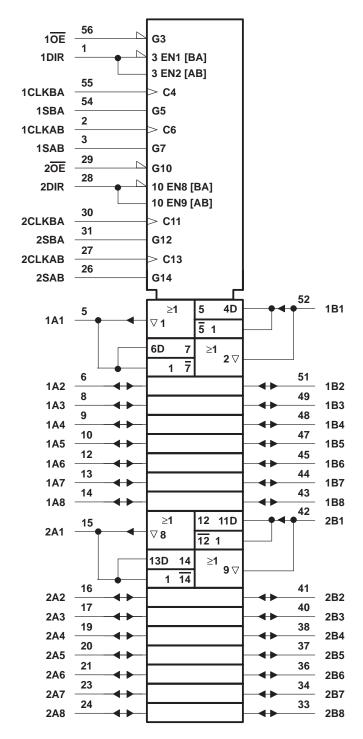
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FUNCTION TABLE

		INP	UTS			DATA	A 1/0†	OPERATION OR FUNCTION
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	OPERATION OR FUNCTION
Х	Х	1	Х	Х	Х	Input Unspecified		Store A, B unspecified [†]
Х	X	Χ	1	Χ	X	Unspecified	Input	Store B, A unspecified [†]
Н	Х	1	1	Χ	Х	Input	Input	Store A and B data
Н	X	H or L	H or L	Χ	X	Input	Input	Isolation, hold storage
L	L	Х	Χ	Χ	L	Output	Input	Real-time B data to A bus
L	L	Χ	H or L	Χ	Н	Output	Input	Stored B data to A bus
L	Н	Х	Х	L	Х	Input	Output	Real-time A data to B Bus
L	Н	H or L	Χ	Н	Χ	Input	Output	Stored A data to bus

[†] The data-output functions may be enabled or disabled by various signals at $\overline{\mathsf{OE}}$ or DIR. Data-input functions are always enabled, i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

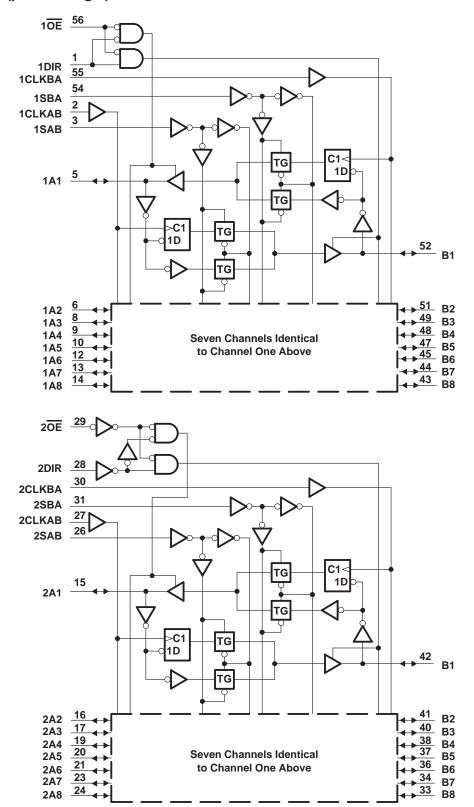
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)





54ACT16646, 74ACT16646 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	\dots –0.5 V to 7 V
Input voltage range, V _I (see Note 1)	$5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, V _O (see Note 1)	$5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	$\dots \dots \pm 20 \; mA$
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	$\dots \dots \pm 50 \; mA$
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	$\dots \dots \pm 50 \; mA$
Continuous current through V _{CC} or GND	$\dots \dots \pm 400 \; mA$
Maximum package power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 2): DL package	1.4 W
Storage temperature range, T _{stq}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 3)

		54ACT	16646	74ACT	16646	UNIT
		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage (see Note 4)	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2	3	2		V
VIL	Low-level input voltage		0.8		0.8	V
٧ _I	Input voltage	0	Vcc	0	VCC	V
٧o	Output voltage	0	Vcc	0	VCC	V
IOH	High-level output current	2	-24		-24	mA
loL	Low-level output current	30/	24		24	mA
Δt/Δν	Input transition rise or fall rate	Q 0	10	0	10	ns/V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTES: 3. Unused inputs must be held high or low to prevent them from floating.

^{2.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

^{4.} All V_{CC} and GND pins must be connected to the proper voltage power supply.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DA.	RAMETER	TEST CONDITIONS	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	T,	_Δ = 25°C		54ACT	16646	74ACT	16646	UNIT	
PAI	RAWETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII	
		Jan - 50 "A	4.5 V	4.4			4.4		4.4			
		IOH = -50 μA	5.5 V	5.4			5.4		5.4			
\ \/ - · ·		I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		V	
VOH		10H = -24 IIIA	5.5 V	4.94			4.7		4.8		V	
		$I_{OH} = -50 \text{ mA}^{\dagger}$	5.5 V				3.85					
		I _{OH} = -75 mA [†]	5.5 V						3.85			
		I 50 A	4.5 V			0.1		0.1		0.1		
		I _{OL} = 50 μA	5.5 V			0.1		0.1		0.1		
.		lo 24 mA	4.5 V			0.36	<	0.5		0.44	.,	
VOL		I _{OL} = 24 mA	5.5 V			0.36	, 'Q'	0.5		0.44	V	
		$I_{OL} = 50 \text{ mA}^{\dagger}$	5.5 V				90	1.65				
		I _{OL} = 75 mA [†]	5.5 V				PA			1.65		
Ιį	Control inputs	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μΑ	
loz	A or B ports [‡]	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μΑ	
Icc	•	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μА	
ΔlCC§		One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.9		1		1	mA	
Ci	Control inputs	V _I = V _{CC} or GND	5 V		4						pF	
C _{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		12						pF	

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, (unless otherwise noted) (see Figure 2)

			T _A = :	25°C	54ACT	16646	74ACT	16646	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
fclock	Clock frequency	0	90	0	90	0	90	MHz	
t _W	Pulse duration, CLKAB or CLKBA high or low	5.5		5.5	10,7	5.5		ns	
	Octor for Abeles OlkAPA - Pheles OlkPAA	Data high	4		4		4		no
t _{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	Data low	6		6		6		ns
th	Hold time, A before CLKAB↑ or B before CLKBA↑	1.5		1.5		1.5		ns	

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCC.

54ACT16646, 74ACT16646 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, (unless otherwise noted) (see Figure 2)

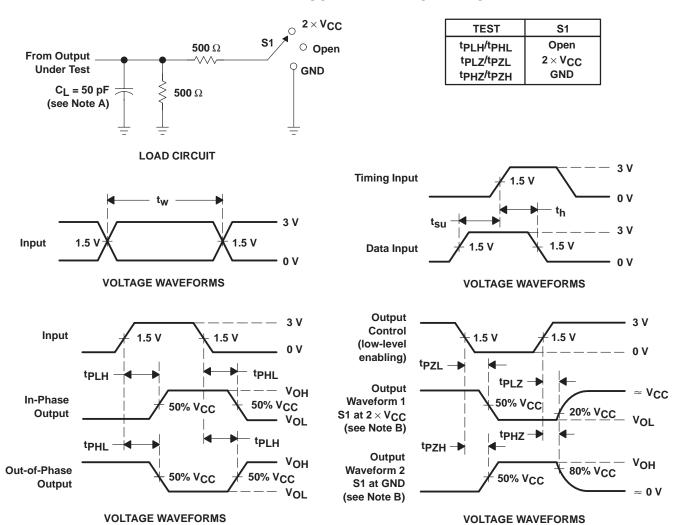
PARAMETER	FROM	то	Т,	λ = 25°C	;	54ACT	16646	74ACT	16646	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII	
f _{max}			90			90		90		MHz	
^t PLH	A or B	B or A	3.9	7.5	9.4	3.9	11.5	3.9	10.6	ns	
t _{PHL}	AOIB	BUIA	3.4	7.6	10.6	3.4	12.2	3.4	11.4	115	
^t PZH	ŌĒ	A or B	3.2	7.7	10.8	3.2	12.9	3.2	11.9	ns	
t _{PZL}	OE	AOIB	4.2	9	12.2	4.2	14.6	4.2	13.5	115	
^t PHZ	ŌĒ	A or B	5.3	7.7	9.6	5.3	10.4	5.3	10.2	no	
tPLZL	OE	AOIB	4.9	7.3	9.2	4.9	10.3	4.9	9.9	ns	
^t PLH	CLKBA or CLKAB	A or B	4.9	8.9	11.1	4.9	13.1	4.9	12.2	ns	
t _{PHL}	CLNBA OI CLNAB	AOIB	5.1	9	11	5.1	13.1	5.1	12.3	115	
^t PLH	SAB or SBA [†]	A or B	5.2	10.3	13.8	5.2	17.2	5.2	15.6	ns	
^t PHL	(with A or B high)	AOIB	4.9	8.2	10.6	4.9	12.5	4.9	11.7	115	
t _{PLH}	SBA or SAB [†]	A or B	4.3	7.8	9.9	4.3	12.1	4.3	11.1	ns	
^t PHL	(with A or B high)	AOIB	5.9	11.2	14.9	5.9	18.2	5.9	16.7	115	
^t PZH	DIR	A or B	4.5	9.5	13.6	4.5	16.2	4.5	15.2	ns	
t _{PZL}	DIK	A UI B	4.3	9.2	11.8	4.3	14.2	4.3	13.1	115	
^t PHZ	DIR	A or B	4.5	7.9	10.2	4.5	11.2	4.5	10.8	ne	
t _{PLZ}	DIK	7016	4.4	7.5	9.8	4.4	10.8	4.4	10.4	ns	

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CON	TYP	UNIT		
C .	Dower discipation conscitance per transceiver	Outputs enabled	$C_1 = 50 pF$	f = 1 MHz	58	n.E
Cpd	Power dissipation capacitance per transceiver	Outputs disabled	CL = 50 pr,	I = I IVIIIZ	13	p⊦

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_{\rm O} = 50~\Omega$, $t_{\rm f} = 3~{\rm ns}$, $t_{\rm f} = 3~{\rm ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ACT16646DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT16646DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT16646DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT16646DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

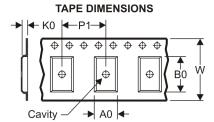
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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ACT16646DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ACT16646DLR	SSOP	DL	56	1000	346.0	346.0	49.0

DL (R-PDSO-G**)

48 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

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