Innovative Service Around the Globe YAGEO

DATA SHEET

MULTILAYER CHIP VARISTORS

VR0402/0603

5.5 V TO 18 V

Phycomp

Product Specification – Sep 15, 2004 V.4

Multilayer Chip Varistors sizes 0402 and 0603

VR0402/0603 5.5 V to 18 V

FEATURES

- Excellent clamping voltage
- Compact size (0402)
- Quick response time (<1n sec.)
- Low capacitance
- High transient current capability
- Symmetrical voltage-current characteristics

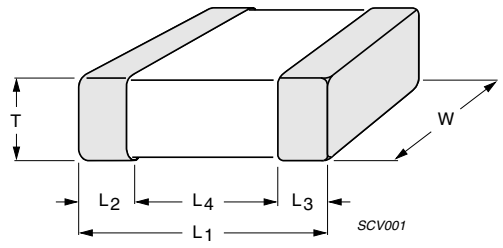
APPLICATIONS

- Consumer electronics (CE)
- Telecommunications
- Electronic data processing (EDP)
- Automotive

DESCRIPTION

Yageo Multilayer Chip Varistors are designed to protect sensitive electronics devices against high voltage transient surges in the low voltage region. They offer excellent transient energy absorption due to improved energy volume distribution and power dissipation. The wide operating voltage and energy range make them suitable for numerous applications on Vcc protection, I/O protection, Keyboard protection, LCD protection and Sensor protection…etc.

MECHANICAL DATA



For dimensions see Table 1.

Fig.1 Component outline.

Physical dimensions

Table 1 Capacitor dimensions

CASE SIZE	L_1	W	T		L_2 and L_3		L_4 MIN.
			MIN.	MAX.	MIN.	MAX.	
Dimensions in millimetres							
0402	1.0 ±0.05	0.5 ±0.05	0.45	0.55	0.15	0.30	0.40
0603	1.6 ±0.10	0.8 ±0.07	0.73	0.87	0.20	0.60	0.40

THICKNESS CLASSIFICATION AND PACKING QUANTITIES

THICKNESS CLASSIFICATION (mm)	8 mm TAPE WIDTH QUANTITY PER REEL
	∅180 mm; 7"
	Paper
0.50 ±0.05	10,000
0.80 ±0.07	4,000

ORDERING INFORMATIONG

Components are ordered by using Phycomp clear text code.

Phycomp clear text code

ORDERING EXAMPLE

The ordering code of a VR0402 varistor, value 68pF with ±10 % tolerance, 5.5 V, supplied on 7" paper tape packing is: VRS0402SR55R680N

Series name	Chip type	Size code	Varistor voltage tolerance	Packing style	Working voltage	Capacitance	Process code
VR = varistor	S = single chip	0402 0603	K = ±10 % L= ±15 % M = ±20 % S = special range	R = 180 mm; 7" paper	55R = 5.5 V 140 = 14 V 180 = 18 V	680 = 68 pF; the first 2 digits indicate the capacitance value; letter R is used as a decimal point; the third digit signifies the multiplying factor: 0 = × 1 1 = × 10	N = Normal E = ESD control

ELECTRICAL CHARACTERISTICS

TYPE/ PHYCOMP CTC	VARISTOR VOLTAGE/ BREAKDOWN VOLTAGE	MAXIMUN CONTINOUS VOLTAGE/ OPERATING VOLTAGE (U_r)	CLAMPING VOLTAGE		ENERGY	PEAK CURRENT	RESISTANCE		CAP.
							R.T. (5~35 °C)		
	V (1mA)	D.C. max.	8/20 μs	Current	10/1000 μs max.	8/20 μs max.	Vol.	Resistance min.	1MHz, 1 V_{rms}
	(V)	(V)	(V)	(A)	(Joule)	(A)	(V)	(MΩ)	(pF)
VRS0402MR55R201N	6.4 to 9.6	5.5	19	1	0.05	20	3	1	200
VRS0402MR55R151N	6.4 to 9.6	5.5	19	1	0.05	20	3	1	150
VRS0402MR55R470N	6.4 to 9.6	5.5	19	1	0.03	10	3	1	47
VRS0402SR55R101N	10 to 14	5.5	27	1	0.05	20	3	1	100
VRS0402SR55R500N	10 to 14	5.5	27	1	0.03	10	3	1	50
VRS0402SR140101N	18 to 24	14	45	1	0.05	20	3	1	100
VRS0402SR140500N	18 to 24	14	45	1	0.03	10	3	1	50
VRS0402SR180150N	24 to 32	18	58	1	0.005	5	3	1	15
VRS0603MR55R681N	6.4 to 9.6	5.5	19	1	0.1	30	3	1	680
VRS0603MR55R301N	6.4 to 9.6	5.5	19	1	0.05	20	3	1	300

Standard testing condition

- Temperature: 15 °C to 35 °C
- Humidity: 25% RH to 85% RH
- Atmospheric pressure: 86 to 106 kPa

ESD (Electrostatic Discharge) Test

ESD discharge circuit according to IEC 61000-4-2

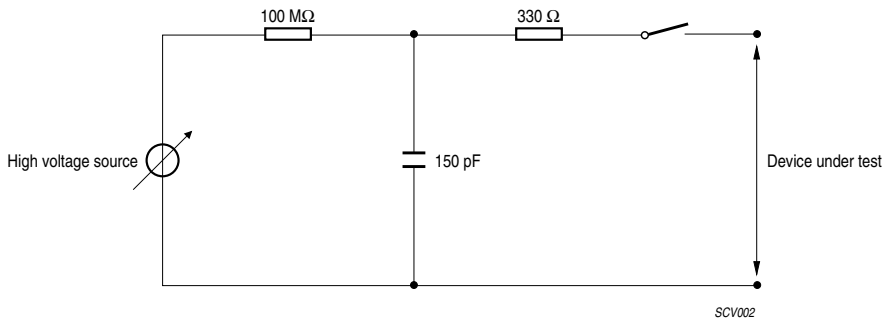


Fig.2 ESD discharge circuit diagram.

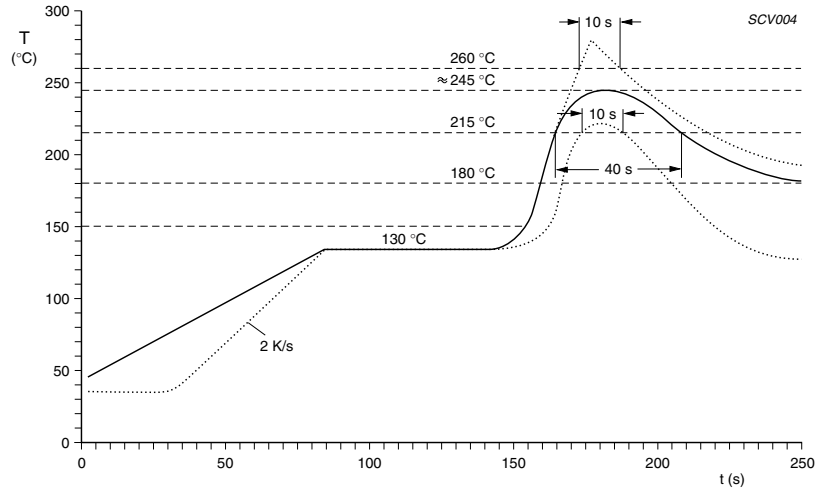
Specification of electrostatic discharge (ESD) test:

- According to standard EN 61000-4-2, up to 8 KV (contact discharge)

METHOD OF MOUNTING AND FOOTPRINT DIMENSIONS

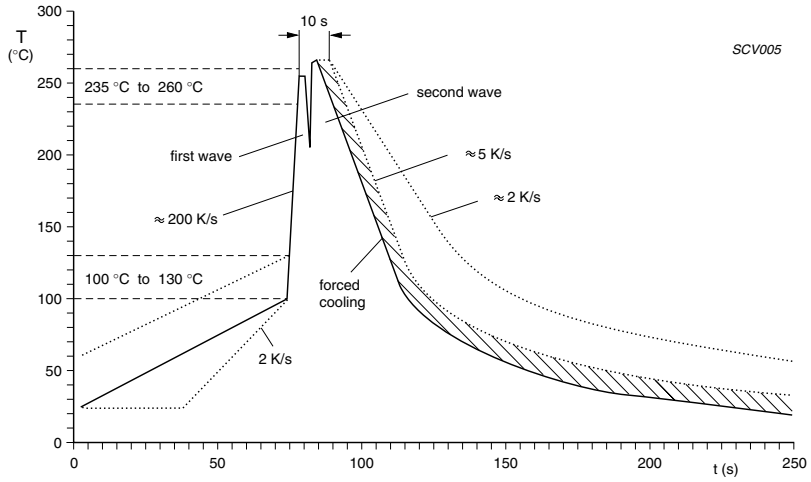
For normal use the varistor may be mounted on printed-circuit boards or ceramic substrates by applying wave soldering, reflow soldering (including vapour phase soldering) or conductive adhesive in accordance with CECC 00802 classification A. For advised soldering profiles see Figs 3, 4, and 5.

An improper combination of soldering, substrate and chip size can lead to a damaging of the component. The risk increases with the chip size and with temperature fluctuations (>100 °C). Therefore, it is advised to use the smallest possible size and follow the dimensional recommendations given in Tables 2 and 3 for reflow and wave soldering. More detailed information is available on request.



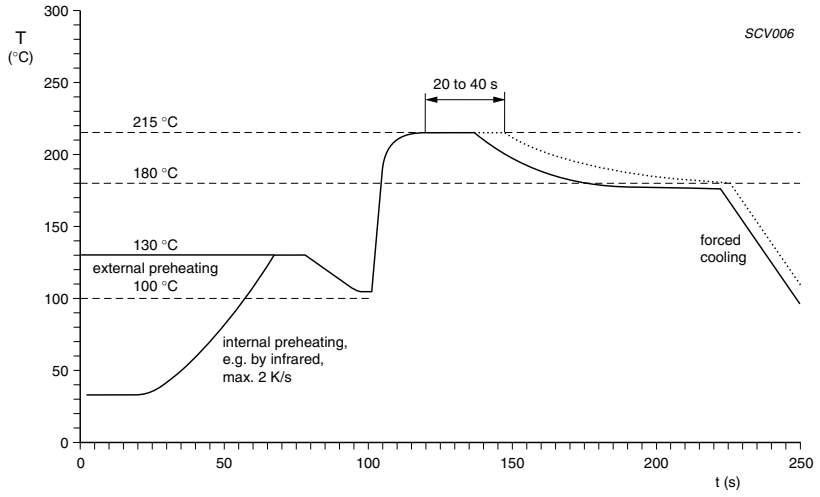
Typical values (solid line).
Process limits (dotted lines).

Fig.3 Reflow soldering.



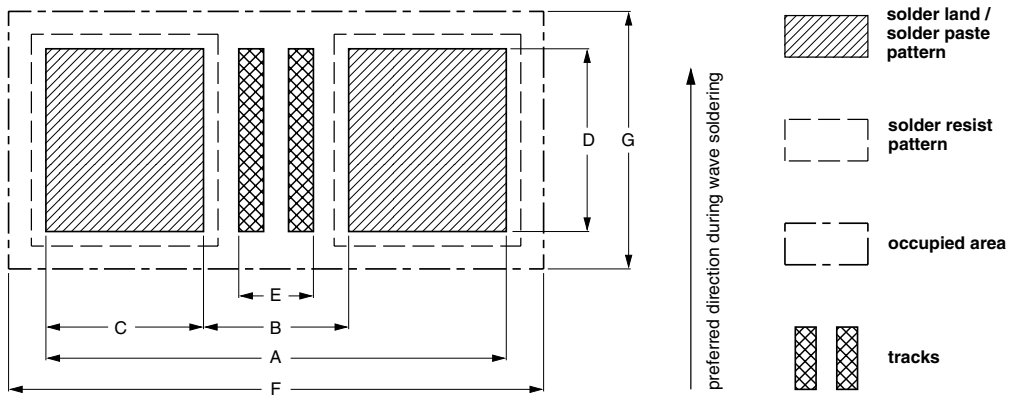
Typical values (solid line).
Process limits (dotted lines).
The capacitors may be soldered twice in accordance with this method if desired.

Fig.4 Double wave soldering.



Typical values (solid line).
Process limits (dotted lines).

Fig.5 Vapour phase soldering.



For dimension see table 2-3

Fig.6 Recommended footprint dimensions.

Table 2 Reflow soldering; for footprint dimensions see Fig.6

SIZE CODE	FOOTPRINT DIMENSIONS (mm)							PROCESSING REMARKS	PLACEMENT ACCURACY (mm)
	A	B	C	D	E	F	G		
0402	1.5	0.5	0.5	0.5	0.10	1.75	0.95	IR or hot plate soldering	±0.15
0603	2.3	0.7	0.8	0.9	0.26	2.7	1.5		±0.15
0603	2.3	0.5	0.9	0.9	0.0	2.7	1.5		±0.25

Table 3 Wave soldering (no dummy tracks allowed for ≥500 V); for footprint dimensions see Fig.6

SIZE CODE	FOOTPRINT DIMENSIONS (mm)							PROPOSED NUMBER AND DIMENSIONS OF DUMMY TRACKS (mm)	PLACEMENT ACCURACY (mm)
	A	B	C	D	E	F	G		
0603	2.4	1.0	0.7	0.8	0.2	3.0	1.9	1 × (0.2 × 0.8)	±0.10
0603	2.7	0.9	0.9	0.8	0.0	3.2	2.1	1 × (0.3 × 0.8)	±0.25

PACKING

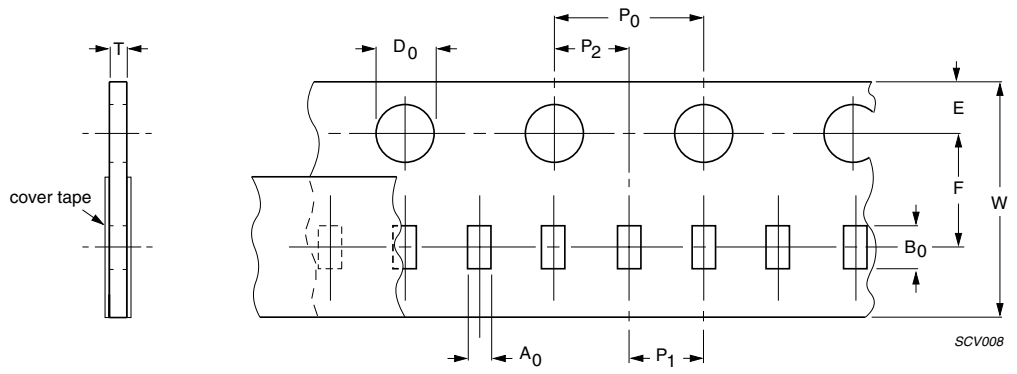
Tape and reel specifications

All tape and reel specifications are in accordance with *"IEC 60286-3"*. Basic dimensions are given in Figs 1, 2 and 5, and Tables 1, 2 and 3.

Peel-off force

Peel-off forces of both paper and blister tapes are in accordance with *"IEC 60286-3"*; that is, at a peel-off speed of 300 ±10 mm/minute, 0.1 N to 1.0 N for 8 mm tape and 0.1 N to 1.3 N for tape larger than 8 mm. The peel-off angle should be between 165° and 180°.

PAPER TAPE



For dimension see table 4

Fig.7 Paper tape.

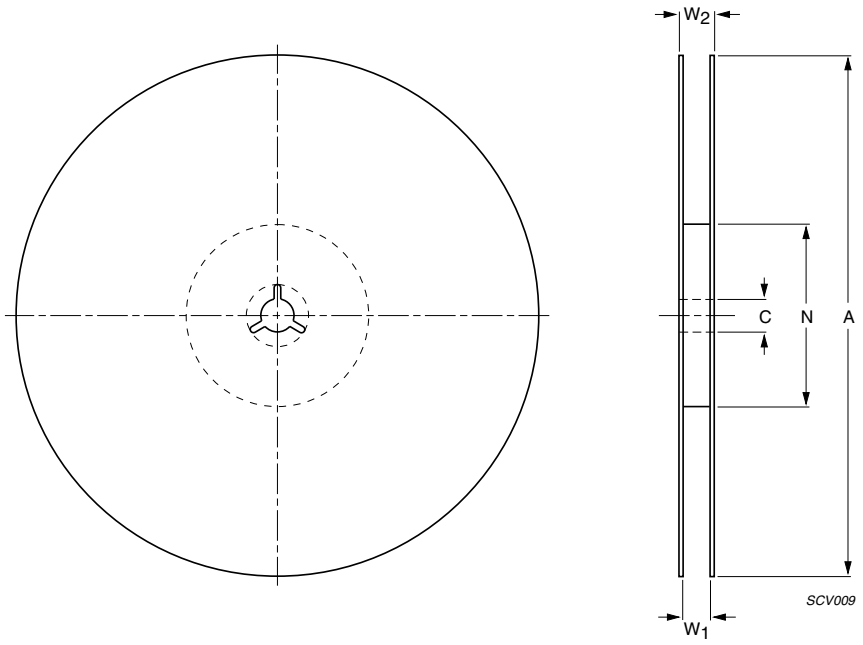
Table 4 Dimensions of paper tape for relevant chip size; see Fig.7

SYMBOL	PRODUCT SIZE CODE				UNIT
	0402		0603		
	Size	Tol.	Size	Tol.	
A_0	0.64	±0.05	1.10	±0.05	mm
B_0	1.14	±0.05	1.81	±0.05	mm
W	8.0	±0.20	8.0	±0.20	mm
E	1.75	±0.10	1.75	±0.10	mm
F	3.5	±0.05	3.5	±0.05	mm
D_0	1.5	+0.1/–0	1.5	+0.1/–0	mm
P_0; note 1	4	±0.05	4	±0.05	mm
P_1	2	±0.05	4	±0.05	mm
P_2	2	±0.05	2	±0.05	mm
T	0.6	±0.05	0.95	±0.05	mm

Note

1. P_0 pitch tolerance over any 10 pitches is ±0.2 mm.

Reel specifications



Dimensions in mm.
For reel dimensions see Table 5.

Fig.8 Reel.

Table 5 Reel dimensions; see Fig.8

Tape width (mm)	A (mm)	N (mm)	C (mm)	W_1 (mm)	W_2 MAX. (mm)
8	180	60 ±1.0	13 +0.50/–0.20	8.4 +1.5/–0.0	14.4
8	330	100 ±1.0	13 +0.50/–0.20	8.4 +1.5/–0.0	14.4
12	180	60 ±1.0	13 +0.50/–0.20	12.4 +2.0/–0.0	18.4

Properties of reel

Material: polystyrene

Surface resistance: $<10^{10}$ Ω/sq.

Leader/trailer tape specification

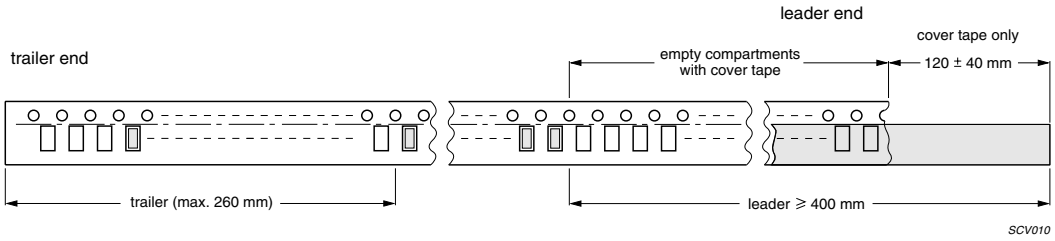


Fig.9 Leader/trailer tape.

Table 6 Leader/trailer tape data

DESCRIPTION	VALUE
Minimum length of empty compartments at leader end	≥ 400 mm of which a minimum 240 mm of empty compartments are covered with cover tape and 120 ±40 mm cover tape only
Minimum length of empty compartments at trailer end	208 mm or 260 mm. If the length is 260 mm an extra product is placed at 208 mm to mark this position.

TESTS AND REQUIREMENTS

Table 7 Test condition, method and requirements

CECC 4200 CLAUSE	IEC 1051-1 CLAUSE	TEST	CONDITION/METHOD	REQUIREMENTS
4.6	4.7	capacitance	f = 1 KHz; measuring voltage 1 V_{rms} at 25 °C	within specified tolerance
4.9	4.10	bond strength of plating on end face	to be soldered on the glass-epoxy (thickness 1.6 mm), the load shall be put on the board bends 1 mm	no visible damage
4.10	4.11	solderability	unmounted chips completely immersed for 2 ±0.5 s (dipping time) in a solder bath at 235 ±2 °C	the termination should be well tinned
4.10.2	4.12	resistance to soldering heat	solder bath temperature: 260 ±5 °C dipping time: 10 ±0.5 s	ΔV_{1mA} / V_{1mA} <10%
4.12	4.13	rapid change of temperature	5 cycles with following detail: 30 minutes at −40 °C; 30 minutes at +85 °C	ΔV_{1mA} / V_{1mA} <10%
4.17	4.18	damp heat with load	duration and conditions: 500 ±12 hours at 40 ±2 °C; 90 to 95% RH; U_r applied	ΔV_{1mA} / V_{1mA} <10%
4.19	4.20	endurance	duration and conditions: 500 ±12 hours at 85 °C; U_r applied	ΔV_{1mA} / V_{1mA} <10%
4.20	4.20	endurance at upper category temperature	duration and conditions: 1,000 ±12 hours at 85 °C	ΔV_{1mA} / V_{1mA} <10%
Tests in accordance with the schedule of IEC publication 60384-1				
IEC 60384-1 CLAUSE		**TEST**	**CONDITION/METHOD**	**REQUIREMENTS**
4.34		adhesion	a force of 2N applied for 10 seconds to the line joining the terminations and in a plane parallel to the substrate	no visible damage
4.25		cold temperature storage	duration and conditions: 1,000 ±12 hours at −40 ±2 °C	ΔV_{1mA} / V_{1mA} <10%

REVISION HISTORY

Revision	Date	Change Notification	Description
Rev.4	2004 Sep 15	-	- Varistor voltage updated
Rev.3	2004 Jul 23	-	- Working voltage extended from 5.5 V to 18 V
Rev.2	2004 Mar 10	-	- Tests and requirements revised
Rev.1	2004 Feb 20	-	- ESD discharge circuit diagram revised
Rev.0	2004 Feb 12	-	-