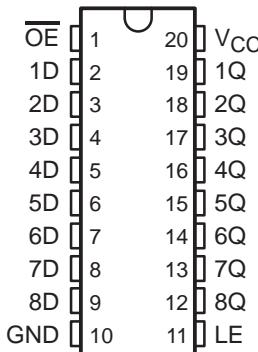


SN54HC573A, SN74HC573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

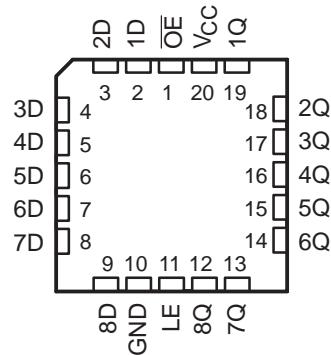
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- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Drive Bus Lines Directly or Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 21$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Bus-Structured Pinout

SN54HC573A . . . J OR W PACKAGE
SN74HC573A . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54HC573A . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These octal transparent D-type latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs respond to the data (D) inputs. When LE is low, the outputs are latched to retain the data that was set up.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC573AN	SN74HC573AN
	SOIC – DW	Tube of 40	SN74HC573ADW	HC573A
		Reel of 2500	SN74HC573ADWR	
	SSOP – DB	Reel of 2000	SN74HC573ADBR	HC573A
-55°C to 125°C	TSSOP – PW	Reel of 2000	SN74HC573APWR	HC573A
		Reel of 250	SN74HC573APWT	
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC573AJ	SNJ54HC573AJ
	CFP – W	Tube of 150	SNJ54HC573AW	SNJ54HC573AW
	LCCC – FK	Tube of 55	SNJ54HC573AFK	SNJ54HC573AFK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54HC573A, SN74HC573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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description/ordering information (continued)

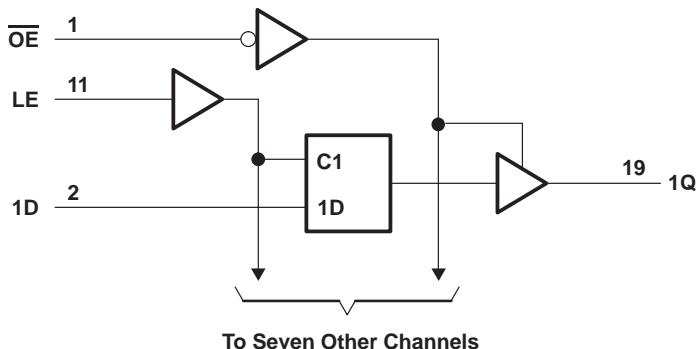
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

FUNCTION TABLE (each latch)

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND	± 70 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	70°C/W
DW package	58°C/W
N package	69°C/W
PW package	83°C/W
Storage temperature range, T_{Stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54HC573A, SN74HC573A
OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

			SN54HC573A			SN74HC573A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5				V
		V _{CC} = 4.5 V	3.15		3.15				
		V _{CC} = 6 V	4.2		4.2				
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		0.5			V
		V _{CC} = 4.5 V		1.35		1.35			
		V _{CC} = 6 V		1.8		1.8			
V _I	Input voltage		0	V _{CC}		0	V _{CC}		V
V _O	Output voltage		0	V _{CC}		0	V _{CC}		V
t _t	Input transition (rise and fall) time	V _{CC} = 2 V		1000		1000			ns
		V _{CC} = 4.5 V		500		500			
		V _{CC} = 6 V		400		400			
T _A	Operating free-air temperature		-55	125	-40	85			°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HC573A		SN74HC573A		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998	1.9		1.9		V	
			4.5 V	4.4	4.499	4.4		4.4			
			6 V	5.9	5.999	5.9		5.9			
		I _{OH} = -6 mA	4.5 V	3.98	4.3	3.7		3.84			
			6 V	5.48	5.8	5.2		5.34			
		I _{OL} = 20 μA	2 V		0.002	0.1		0.1			
V _{OL}	V _I = V _{IH} or V _{IL}		4.5 V		0.001	0.1		0.1			
			6 V		0.001	0.1		0.1			
			I _{OL} = 6 mA	4.5 V		0.17	0.26	0.4	0.33		
			I _{OL} = 7.8 mA	6 V		0.15	0.26	0.4	0.33		
I _I	V _I = V _{CC} or 0	6 V		±0.1	±100	±1000		±1000		nA	
I _{OZ}	V _O = V _{CC} or 0	6 V		±0.01	±0.5	±10		±5		μA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0	6 V			8	160		80		μA	
C _i		2 V to 6 V		3	10	10		10		pF	

**SN54HC573A, SN74HC573A
OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS**

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V _{CC}	T _A = 25°C		SN54HC573A		SN74HC573A		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high			2 V	80	120	100			ns
	4.5 V	16		24	20					
	6 V	14		20	17					
t _{su}	Setup time, data before LE↓			2 V	50	75	63			ns
	4.5 V	10		15	13					
	6 V	9		13	11					
t _h	Hold time, data after LE↓			2 V	20	24	24			ns
	4.5 V	5		5	5					
	6 V	5		5	5					

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC573A		SN74HC573A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	D	Q	2 V	77	175		265		220		ns
			4.5 V	26	35		53		44		
			6 V	23	30		45		38		
	LE	Any Q	2 V	87	175		265		220		ns
			4.5 V	27	35		53		44		
			6 V	23	30		45		38		
t _{en}	OE	Any Q	2 V	68	150		225		190		ns
			4.5 V	24	30		45		38		
			6 V	21	26		38		32		
t _{dis}	OE	Any Q	2 V	47	150		225		190		ns
			4.5 V	23	30		45		38		
			6 V	21	26		38		32		
t _t		Any Q	2 V	28	60		90		75		ns
			4.5 V	8	12		18		15		
			6 V	6	10		15		13		

SN54HC573A, SN74HC573A
OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC573A		SN74HC573A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	D	Q	2 V	95	200	300	250				ns
			4.5 V	33	40	60	50				
			6 V	21	34	51	43				
	LE	Any Q	2 V	103	225	335	285				
			4.5 V	33	45	67	57				
			6 V	29	38	57	48				
t _{en}	OE	Any Q	2 V	85	200	300	250				ns
			4.5 V	29	40	60	50				
			6 V	26	34	51	43				
t _t		Any Q	2 V	60	210	315	265				ns
			4.5 V	17	42	63	53				
			6 V	14	36	53	45				

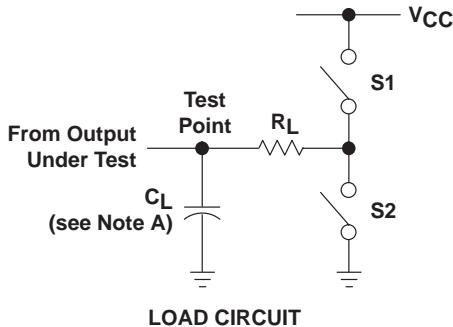
operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per latch	No load	50	pF

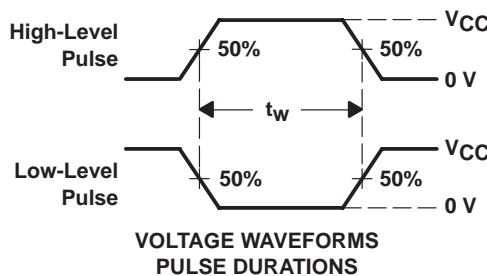
SN54HC573A, SN74HC573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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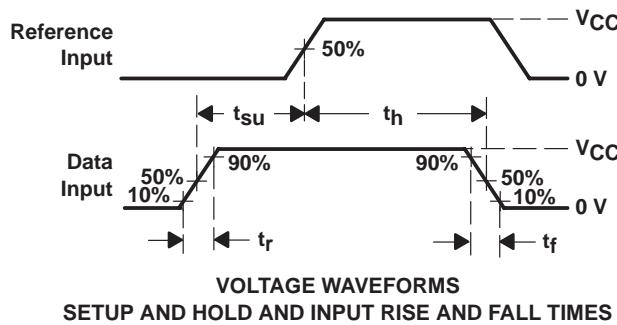
PARAMETER MEASUREMENT INFORMATION



PARAMETER		R _L	C _L	S1	S2
t _{en}	tPZH	1 k Ω	50 pF or 150 pF	Open	Closed
	tPZL			Closed	Open
t _{dis}	tPHZ	1 k Ω	50 pF	Open	Closed
	tPLZ			Closed	Open
t _{pd} or t _t		--	50 pF or 150 pF	Open	Open

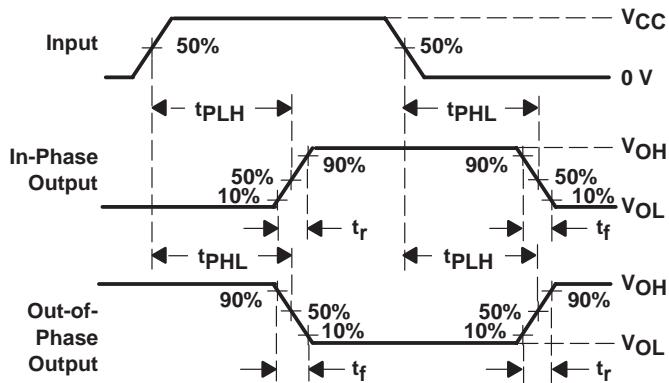


VOLTAGE WAVEFORMS PULSE DURATIONS



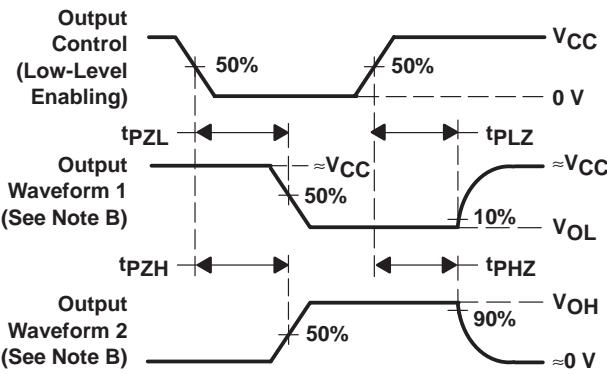
VOLTAGE WAVEFORMS

SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS

PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES:

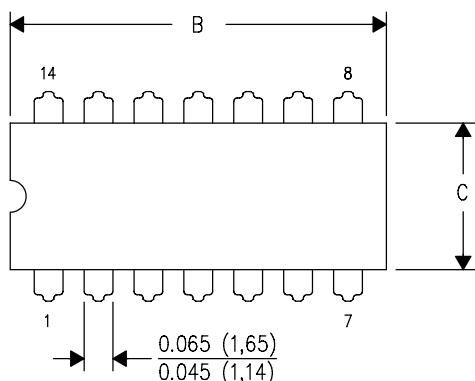
- A. C_L includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

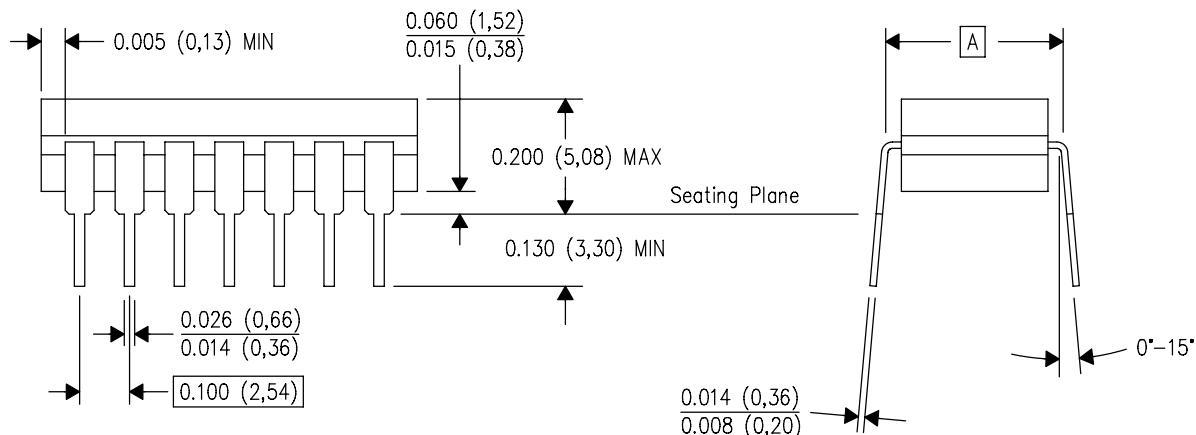
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

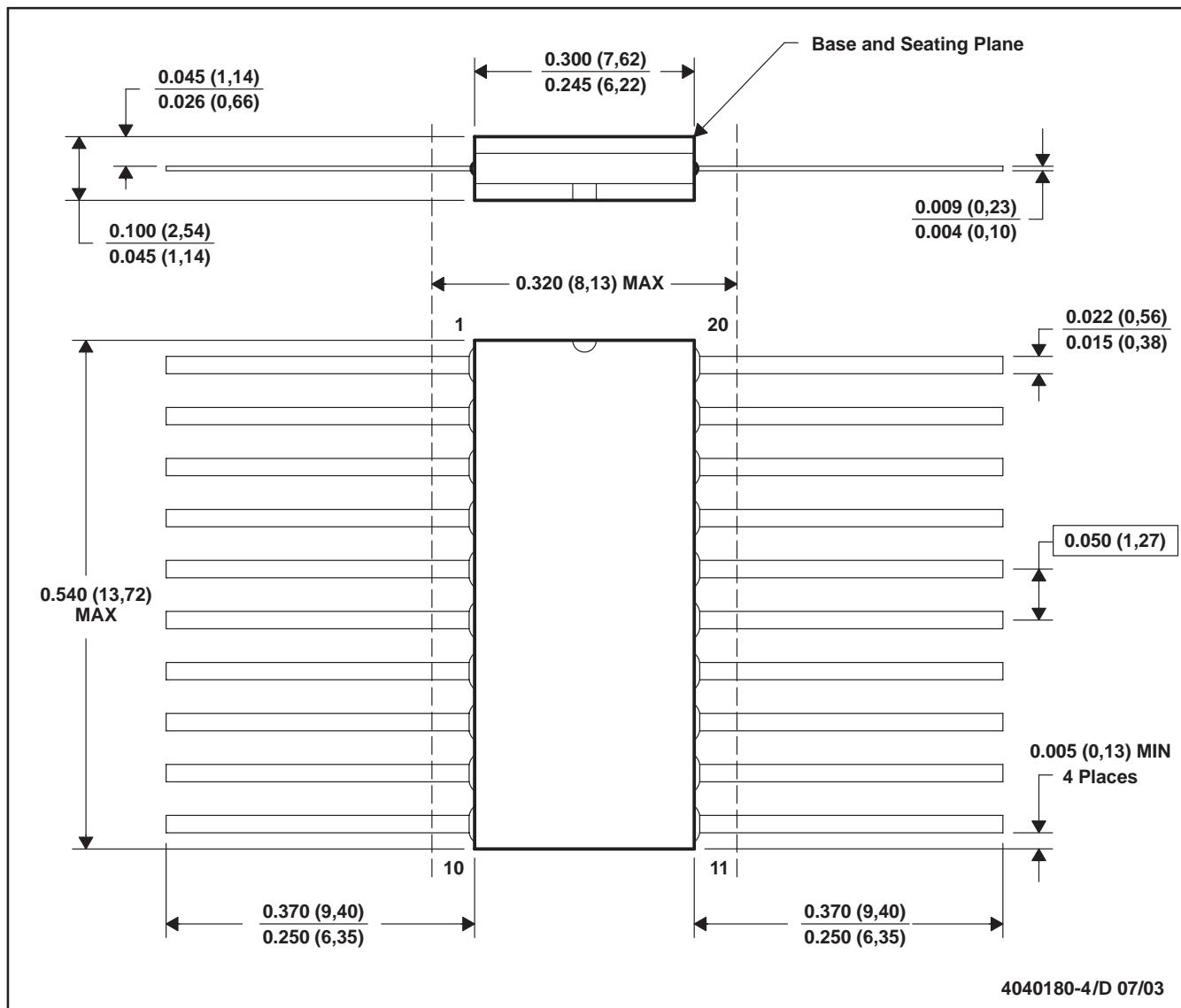


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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



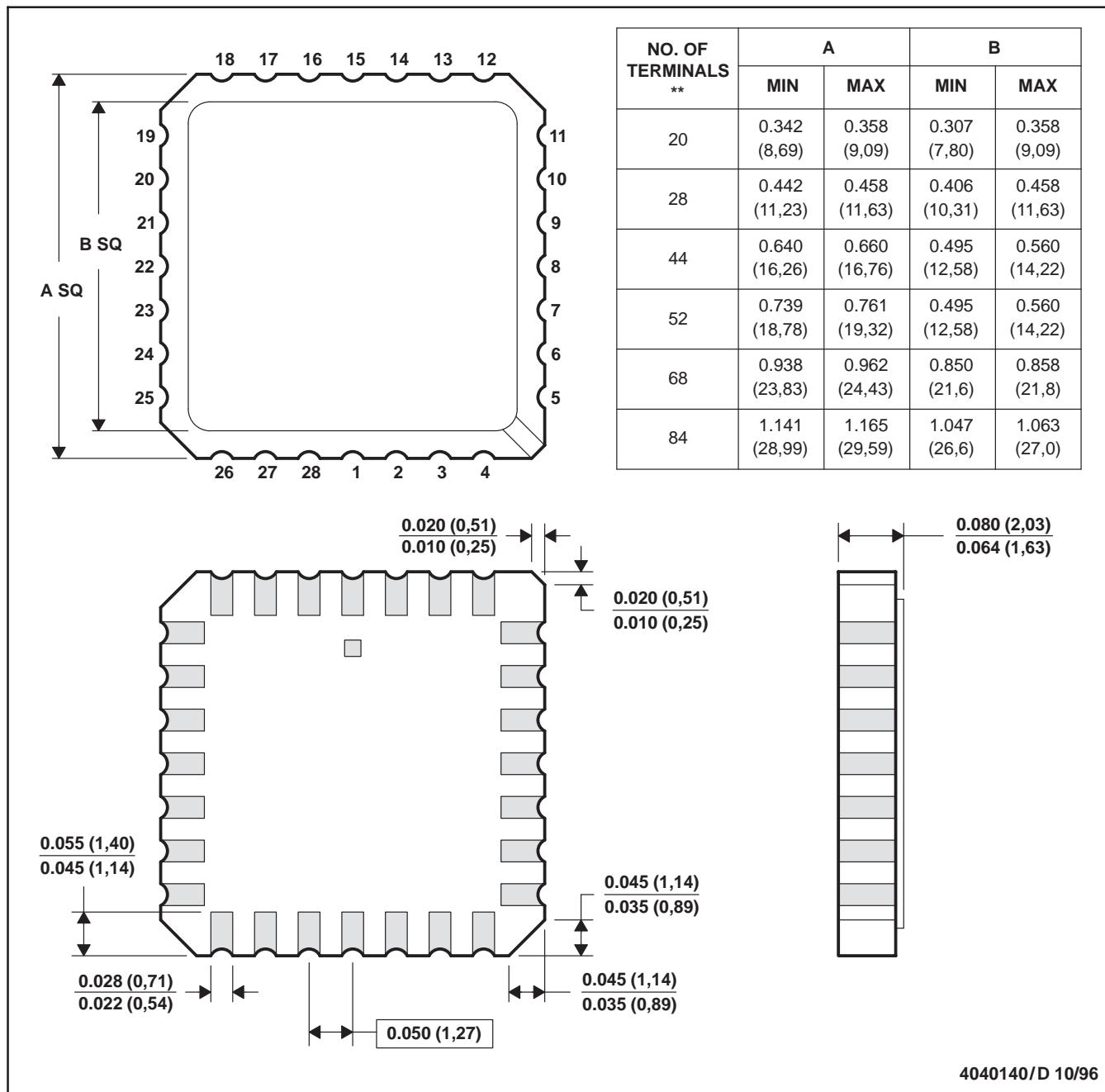
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within Mil-Std 1835 GDGP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004

N (R-PDIP-T**)

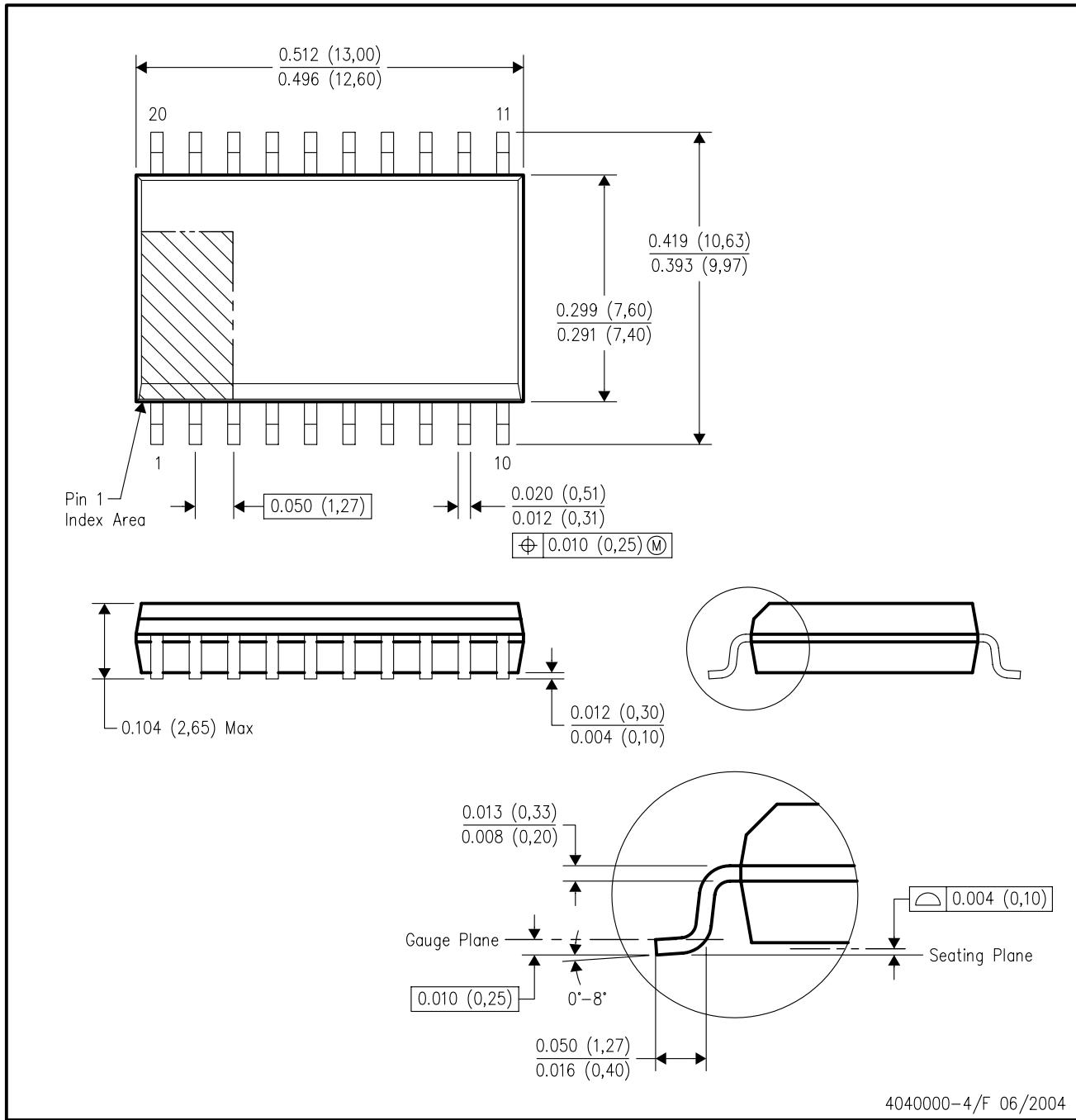
16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



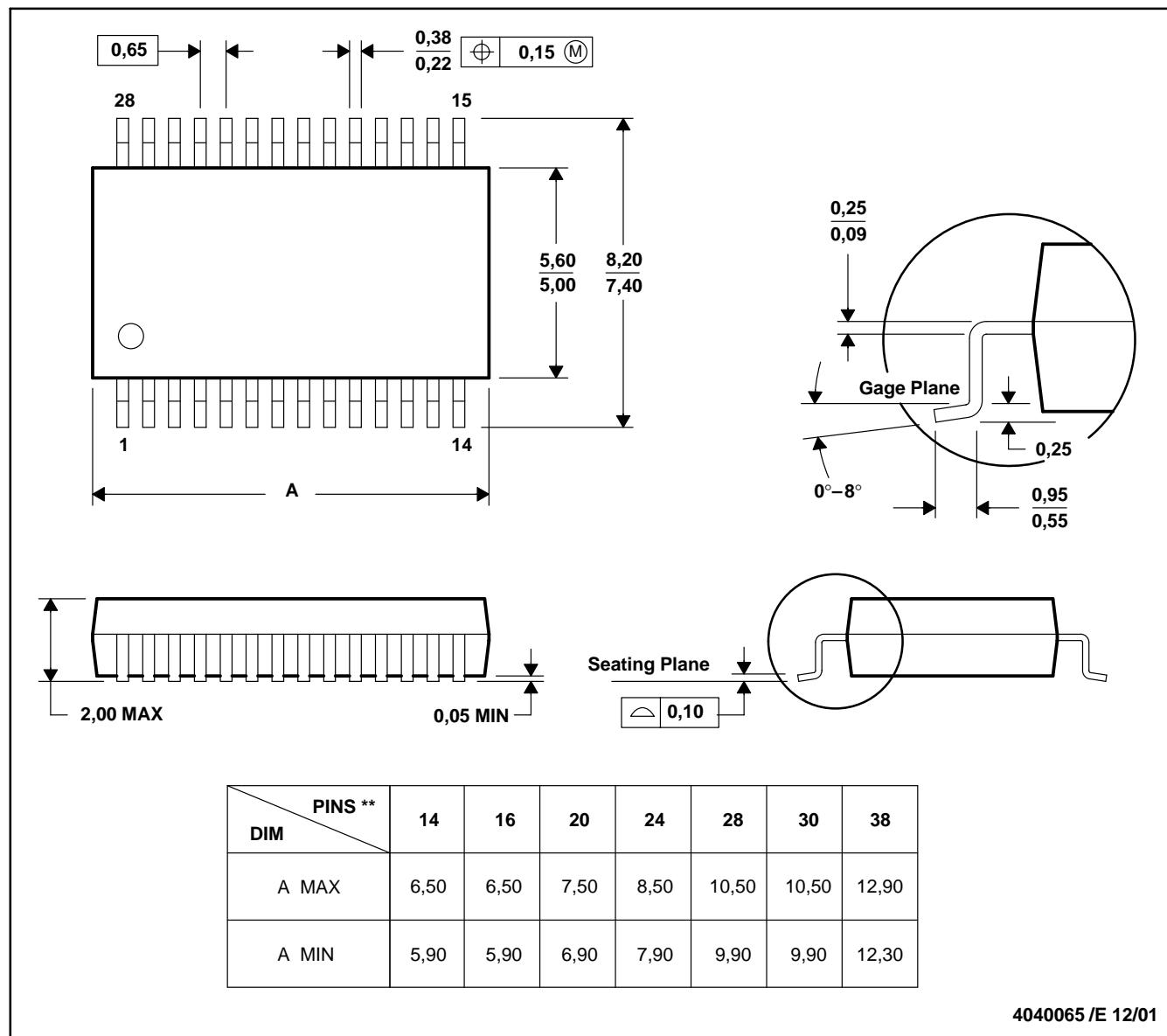
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-013 variation AC.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

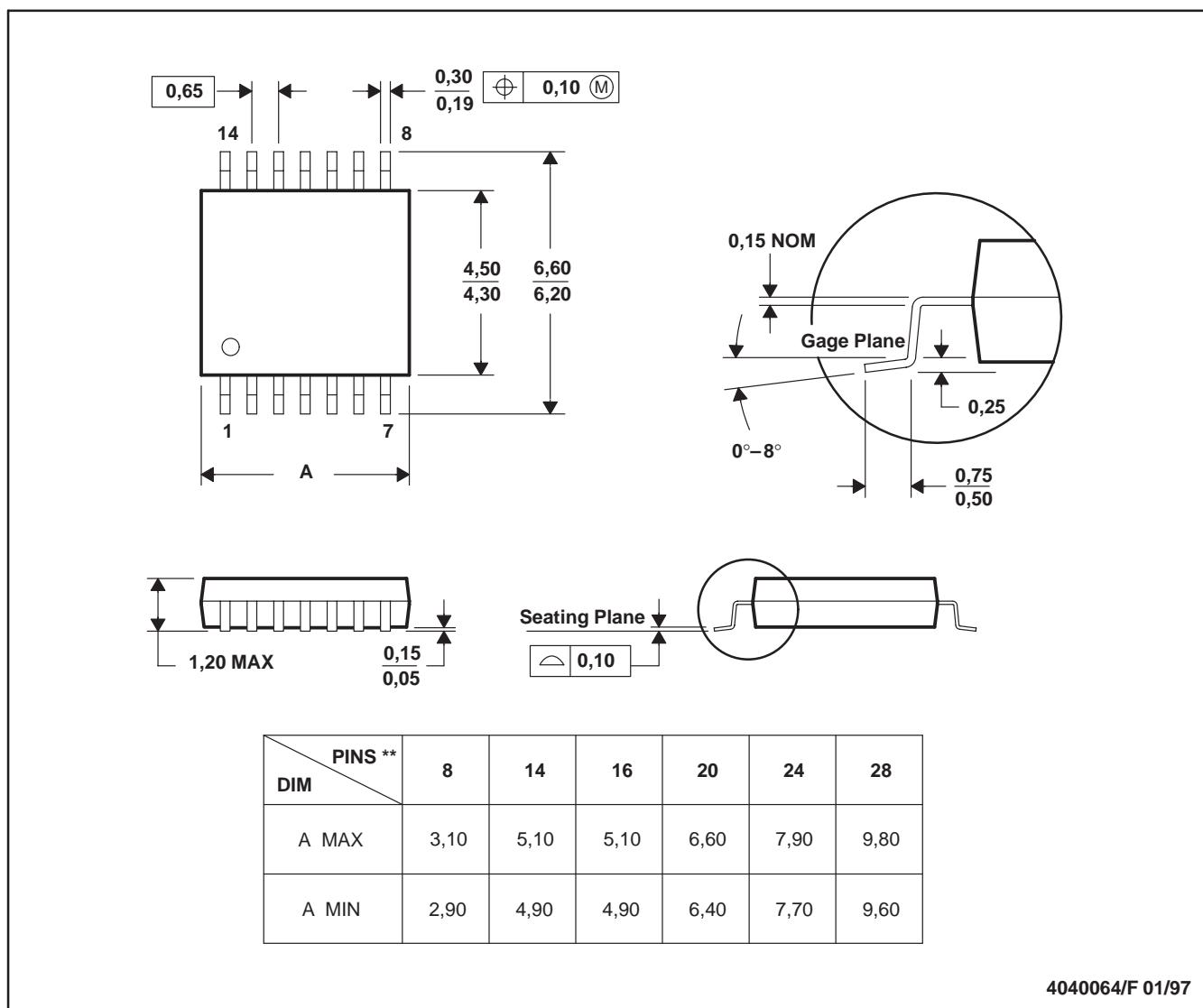


NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- Falls within JEDEC MO-153

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