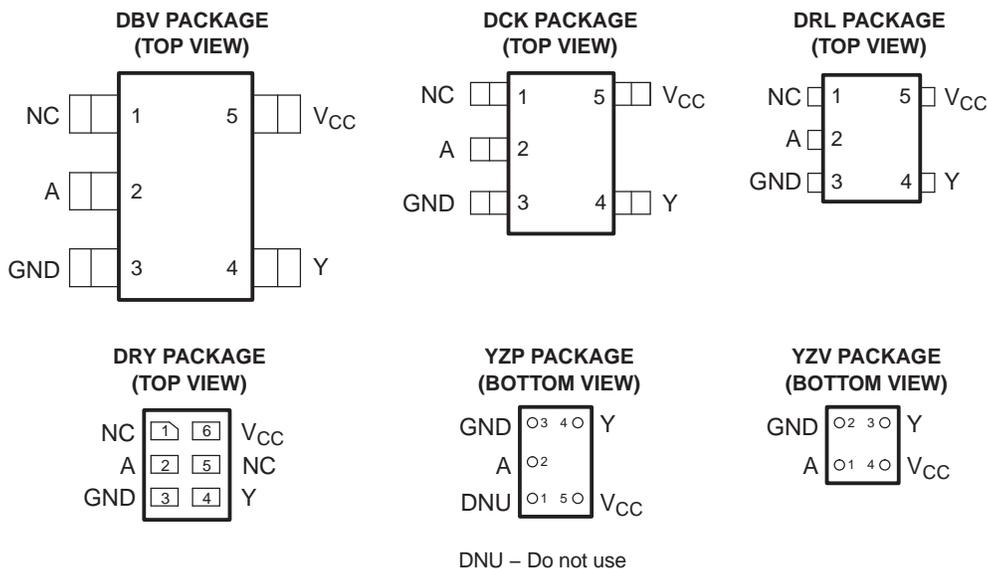


FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 3.3 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



NC – No internal connection
See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single inverter gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G04 performs the Boolean function $Y = \bar{A}$.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

SN74LVC1G04 SINGLE INVERTER GATE

SCES214U–APRIL 1999–REVISED FEBRUARY 2007

ORDERING INFORMATION

| T _A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING ⁽²⁾ |
|---------------------|---|-----------------|-----------------------|---------------------------------|
| –40°C to 85°C | NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free) | | SN74LVC1G04YZPR | ___ CC_ |
| | NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZV (Pb-free) | | SN74LVC1G04YZVR | ___ CC_ |
| | SON – DRY | Reel of 5000 | SN74LVC1G04DRYR | CC_ |
| | | | SN74LVC1G04DRYRG4 | |
| | SOT (SOT-23) – DBV | Reel of 3000 | SN74LVC1G04DBVR | C04_ |
| | | Reel of 250 | SN74LVC1G04DBVT | |
| | SOT (SC-70) – DCK | Reel of 3000 | SN74LVC1G04DCKR | CC_ |
| | | Reel of 250 | SN74LVC1G04DCKT | |
| SOT (SOT-553) – DRL | Reel of 4000 | SN74LVC1G04DRLR | | |

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) DBV/DCK/DRL/DRY: The actual top-side marking has one additional character that designates the assembly/test site. YZP/YZV: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

LOGIC DIAGRAM (POSITIVE LOGIC) (DBV, DCK, DRL, DRY, AND YZP PACKAGE)



LOGIC DIAGRAM (POSITIVE LOGIC) (YZV PACKAGE)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|---|-------------|----------------|------|
| V_{CC} | Supply voltage range | –0.5 | 6.5 | V |
| V_I | Input voltage range | –0.5 | 6.5 | V |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | –0.5 | 6.5 | V |
| V_O | Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾ | –0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I < 0$ | –50 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ | –50 | mA |
| I_O | Continuous output current | | ±50 | mA |
| | Continuous current through V_{CC} or GND | | ±100 | mA |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | DBV package | 206 | °C/W |
| | | DCK package | 252 | |
| | | DRL package | 142 | |
| | | DRY package | 234 | |
| | | YZP package | 132 | |
| | | YZV package | TBD | |
| T_{stg} | Storage temperature range | –65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

SN74LVC1G04 SINGLE INVERTER GATE

SCES214U–APRIL 1999–REVISED FEBRUARY 2007

Recommended Operating Conditions⁽¹⁾

| | | MIN | MAX | UNIT | |
|-----------------|------------------------------------|---|------------------------|------------------------|------|
| V _{CC} | Supply voltage | Operating | 1.65 | 5.5 | V |
| | | Data retention only | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | | |
| | | V _{CC} = 3 V to 3.6 V | 2 | | |
| | | V _{CC} = 4.5 V to 5.5 V | 0.7 × V _{CC} | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | | 0.7 | |
| | | V _{CC} = 3 V to 3.6 V | | 0.8 | |
| | | V _{CC} = 4.5 V to 5.5 V | | 0.3 × V _{CC} | |
| V _I | Input voltage | 0 | 5.5 | V | |
| V _O | Output voltage | 0 | V _{CC} | V | |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | | –4 | mA |
| | | V _{CC} = 2.3 V | | –8 | |
| | | V _{CC} = 3 V | | –16 | |
| | | V _{CC} = 4.5 V | | –24 | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | | 4 | mA |
| | | V _{CC} = 2.3 V | | 8 | |
| | | V _{CC} = 3 V | | 16 | |
| | | V _{CC} = 4.5 V | | 32 | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V | | 20 | ns/V |
| | | V _{CC} = 3.3 V ± 0.3 V | | 10 | |
| | | V _{CC} = 5 V ± 0.5 V | | 5 | |
| T _A | Operating free-air temperature | –40 | 85 | °C | |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------|---------|--|-----------------|-----------------------|--------------------|------|------|
| V _{OH} | | I _{OH} = -100 μA | 1.65 V to 5.5 V | V _{CC} - 0.1 | | | V |
| | | I _{OH} = -4 mA | 1.65 V | 1.2 | | | |
| | | I _{OH} = -8 mA | 2.3 V | 1.9 | | | |
| | | I _{OH} = -16 mA | 3 V | 2.4 | | | |
| | | I _{OH} = -24 mA | | 2.3 | | | |
| | | I _{OH} = -32 mA | 4.5 V | 3.8 | | | |
| V _{OL} | | I _{OL} = 100 μA | 1.65 V to 5.5 V | | | 0.1 | V |
| | | I _{OL} = 4 mA | 1.65 V | | | 0.45 | |
| | | I _{OL} = 8 mA | 2.3 V | | | 0.3 | |
| | | I _{OL} = 16 mA | 3 V | | | 0.4 | |
| | | I _{OL} = 24 mA | | | | 0.55 | |
| | | I _{OL} = 32 mA | 4.5 V | | | 0.55 | |
| I _I | A input | V _I = 5.5 V or GND | 0 to 5.5 V | | | ±5 | μA |
| I _{off} | | V _I or V _O = 5.5 V | 0 | | | ±10 | μA |
| I _{CC} | | V _I = 5.5 V or GND I _O = 0 | 1.65 V to 5.5 V | | | 10 | μA |
| ΔI _{CC} | | One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | 3 V to 5.5 V | | | 500 | μA |
| C _i | | V _I = V _{CC} or GND | 3.3 V | | | 3.5 | pF |

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 5 V ± 0.5 V | | UNIT |
|-----------------|--------------|-------------|----------------------------------|-----|---------------------------------|-----|---------------------------------|-----|-------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A | Y | 2 | 6.4 | 1 | 4.2 | 0.7 | 3.3 | 0.7 | 3.1 | ns |

Switching Characteristics

over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (see [Figure 2](#))

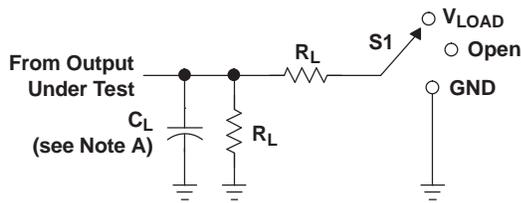
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 5 V ± 0.5 V | | UNIT |
|-----------------|--------------|-------------|----------------------------------|-----|---------------------------------|-----|---------------------------------|-----|-------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A | Y | 3 | 7.5 | 1.4 | 5.2 | 1 | 4.2 | 1 | 3.7 | ns |

Operating Characteristics

T_A = 25°C

| PARAMETER | TEST CONDITIONS | V _{CC} = 1.8 V | V _{CC} = 2.5 V | V _{CC} = 3.3 V | V _{CC} = 5 V | UNIT | |
|-----------------|-------------------------------|-------------------------|-------------------------|-------------------------|-----------------------|------|----|
| | | TYP | TYP | | TYP | | |
| C _{pd} | Power dissipation capacitance | f = 10 MHz | 16 | 18 | 18 | 20 | pF |

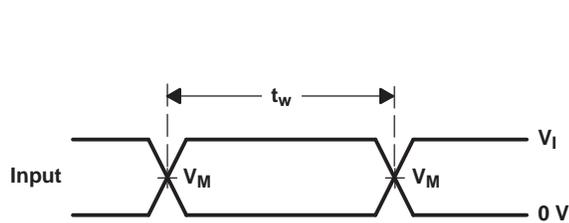
PARAMETER MEASUREMENT INFORMATION



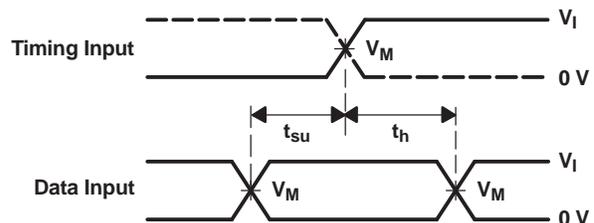
LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

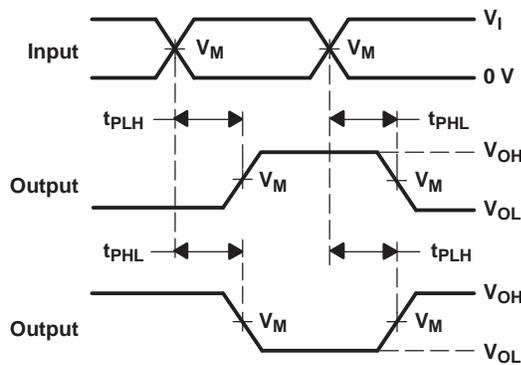
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 15 pF | 1 M Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.3 V |



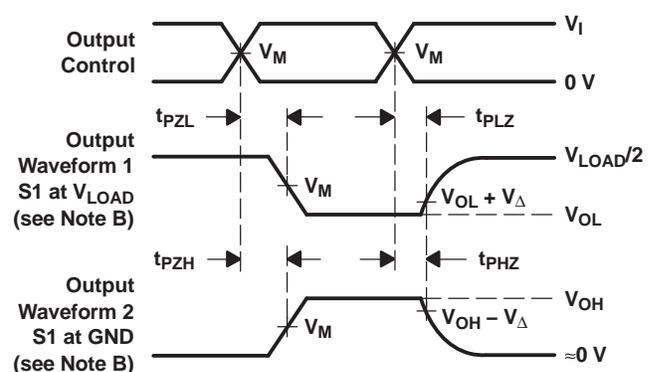
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

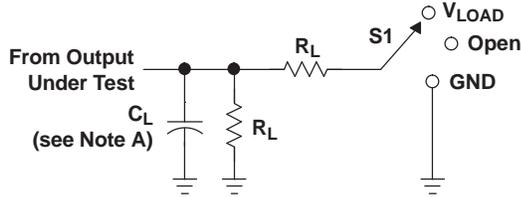


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

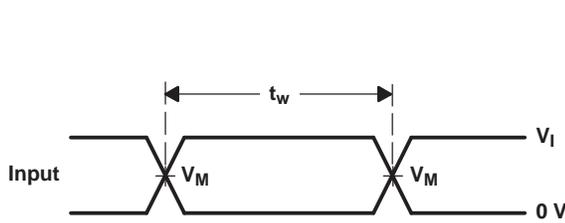
PARAMETER MEASUREMENT INFORMATION



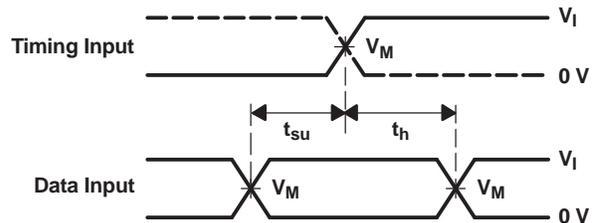
LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

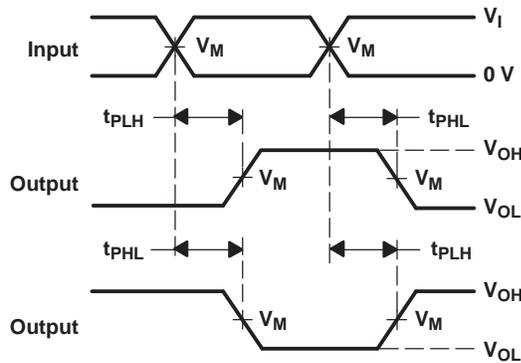
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



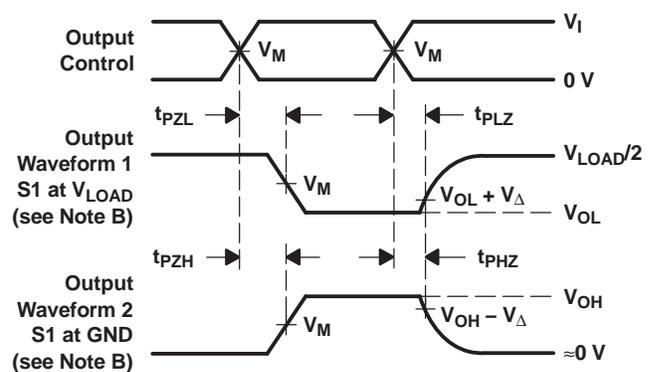
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|--------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74LVC1G04DBVBR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G04DBVRE4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G04DBVBRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G04DBVBT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G04DBVTE4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G04DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G04DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G04DCKRE4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G04DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G04DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G04DCKTE4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G04DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G04DRLR | ACTIVE | SOP | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G04DRLRG4 | ACTIVE | SOP | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G04DRYR | ACTIVE | SON | DRY | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G04DRYRG4 | ACTIVE | SON | DRY | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G04YZPR | ACTIVE | WCSP | YZP | 5 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM |
| SN74LVC1G04YZVR | ACTIVE | DSBGA | YZV | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

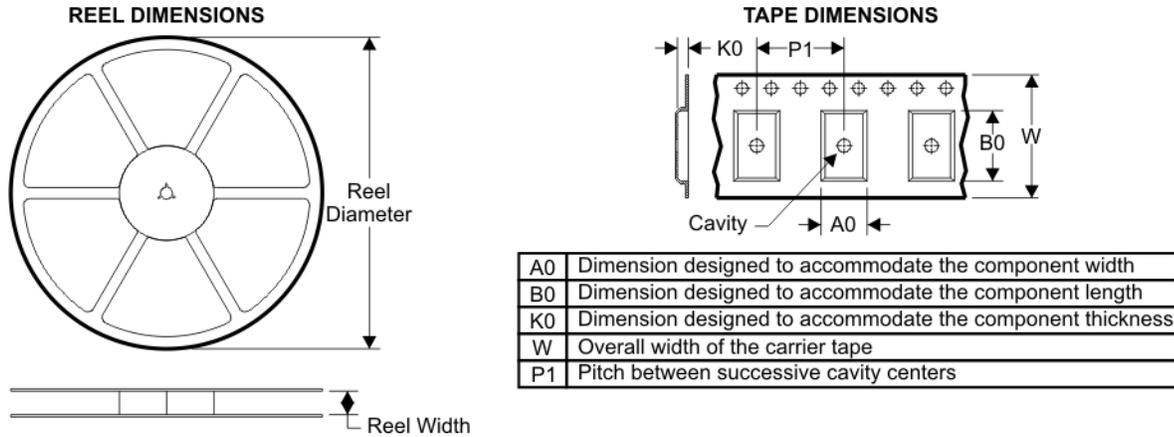
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

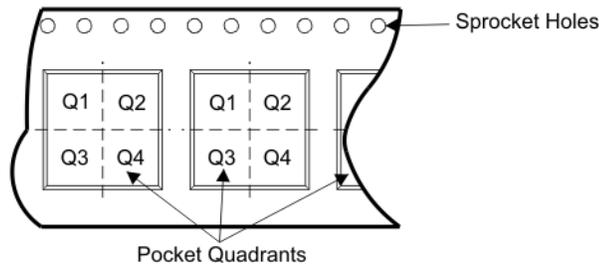
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TAPE AND REEL BOX INFORMATION

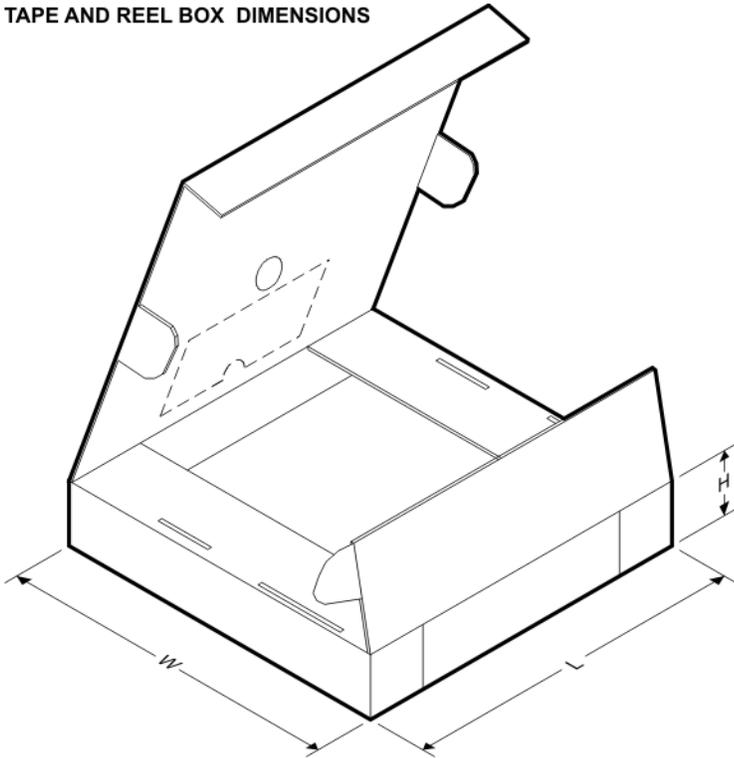


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| Device | Package | Pins | Site | Reel Diameter (mm) | Reel Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|---------|------|---------|--------------------|-----------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC1G04DBVR | DBV | 5 | SITE 34 | 180 | 9 | 3.23 | 3.17 | 1.37 | 4 | 8 | Q3 |
| SN74LVC1G04DBVR | DBV | 5 | SITE 45 | 0 | 0 | 3.23 | 3.17 | 1.37 | 4 | 8 | Q3 |
| SN74LVC1G04DBVT | DBV | 5 | SITE 34 | 180 | 9 | 3.23 | 3.17 | 1.37 | 4 | 8 | Q3 |
| SN74LVC1G04DBVT | DBV | 5 | SITE 45 | 330 | 16 | 10.6 | 15.8 | 4.9 | 16 | 24 | Q3 |
| SN74LVC1G04DCKR | DCK | 5 | SITE 34 | 180 | 9 | 2.24 | 2.34 | 1.22 | 4 | 8 | Q3 |
| SN74LVC1G04DCKT | DCK | 5 | SITE 34 | 180 | 9 | 2.24 | 2.34 | 1.22 | 4 | 8 | Q3 |
| SN74LVC1G04DRLR | DRL | 5 | SITE 35 | 180 | 9 | 1.78 | 1.78 | 0.69 | 4 | 8 | Q3 |
| SN74LVC1G04DRYR | DRY | 6 | SITE 48 | 179 | 8 | 1.2 | 1.65 | 0.7 | 4 | 8 | Q1 |
| SN74LVC1G04YZPR | YZP | 5 | SITE 12 | 180 | 8 | 1.02 | 1.52 | 0.66 | 4 | 8 | Q1 |
| SN74LVC1G04YZVR | YZV | 4 | SITE 12 | 180 | 8 | 1.02 | 1.02 | 0.56 | 4 | 8 | Q1 |

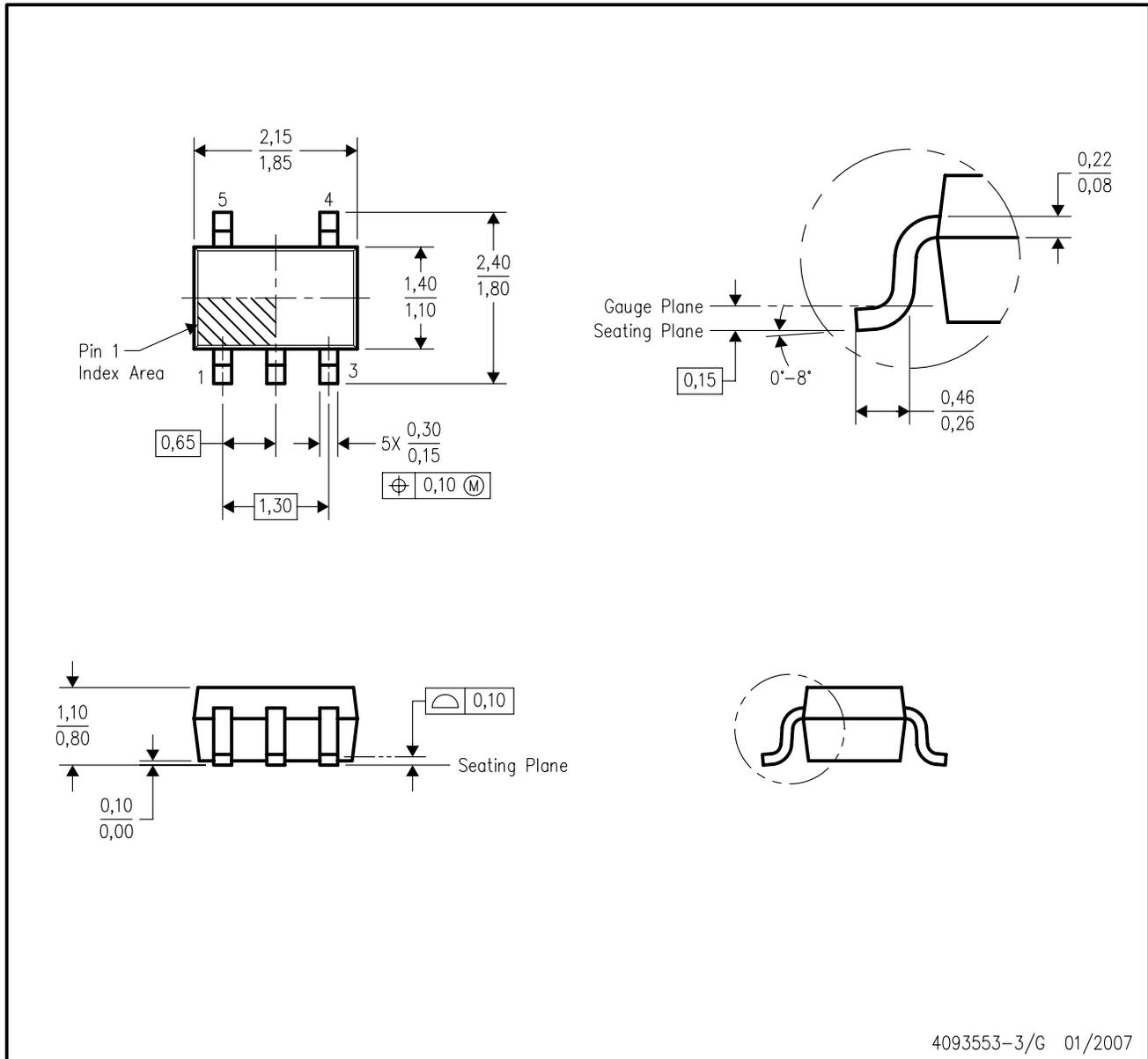
TAPE AND REEL BOX DIMENSIONS



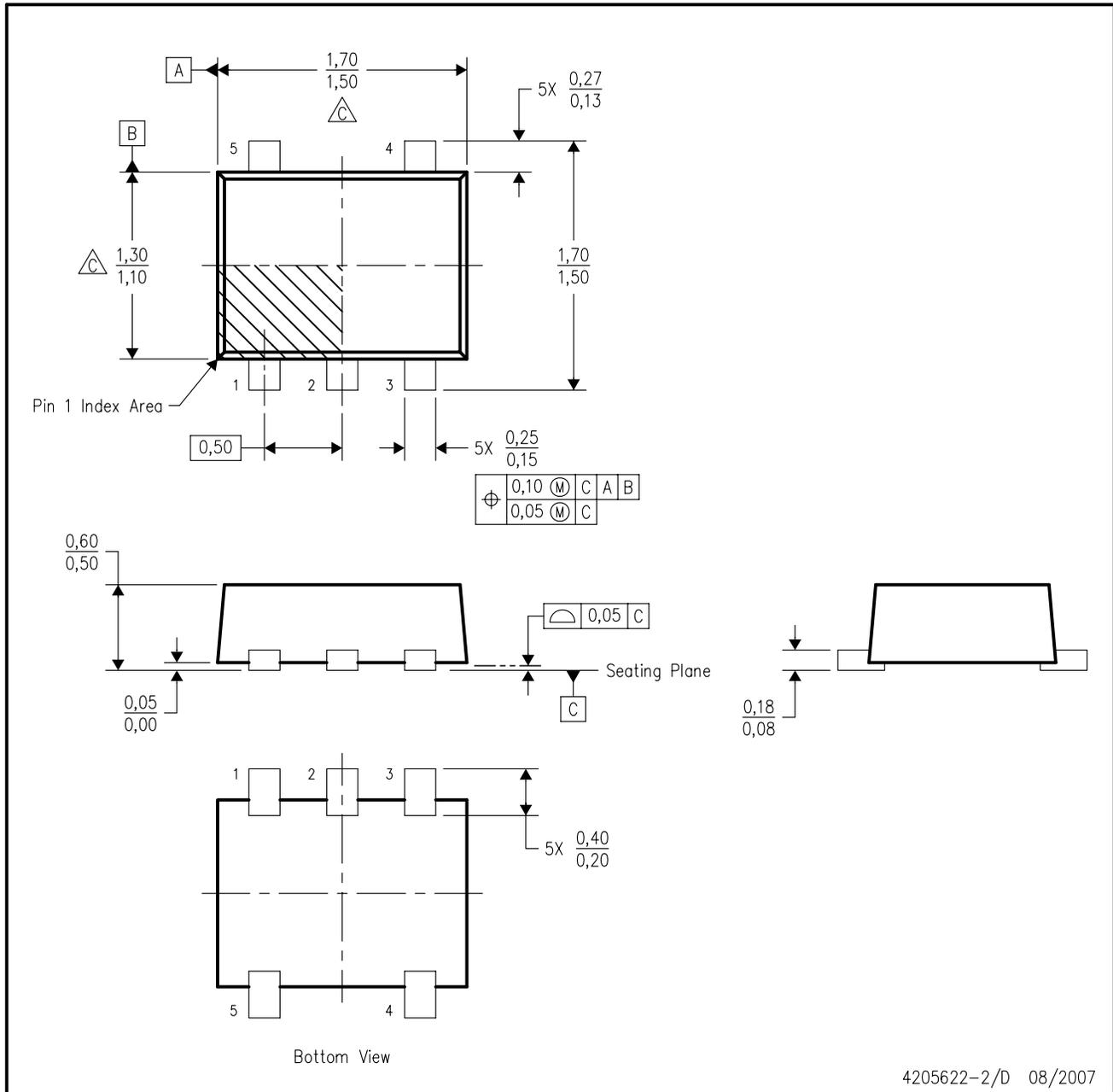
| Device | Package | Pins | Site | Length (mm) | Width (mm) | Height (mm) |
|-----------------|---------|------|---------|-------------|------------|-------------|
| SN74LVC1G04DBVR | DBV | 5 | SITE 34 | 205.0 | 200.0 | 33.0 |
| SN74LVC1G04DBVR | DBV | 5 | SITE 45 | 0.0 | 185.0 | 220.0 |
| SN74LVC1G04DBVT | DBV | 5 | SITE 34 | 201.0 | 192.0 | 26.0 |
| SN74LVC1G04DBVT | DBV | 5 | SITE 45 | 0.0 | 0.0 | 0.0 |
| SN74LVC1G04DCKR | DCK | 5 | SITE 34 | 205.0 | 200.0 | 33.0 |
| SN74LVC1G04DCKT | DCK | 5 | SITE 34 | 201.0 | 192.0 | 26.0 |
| SN74LVC1G04DRLR | DRL | 5 | SITE 35 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G04DRYR | DRY | 6 | SITE 48 | 220.0 | 205.0 | 50.0 |
| SN74LVC1G04YZPR | YZP | 5 | SITE 12 | 220.0 | 220.0 | 0.0 |
| SN74LVC1G04YZVR | YZV | 4 | SITE 12 | 220.0 | 220.0 | 0.0 |

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



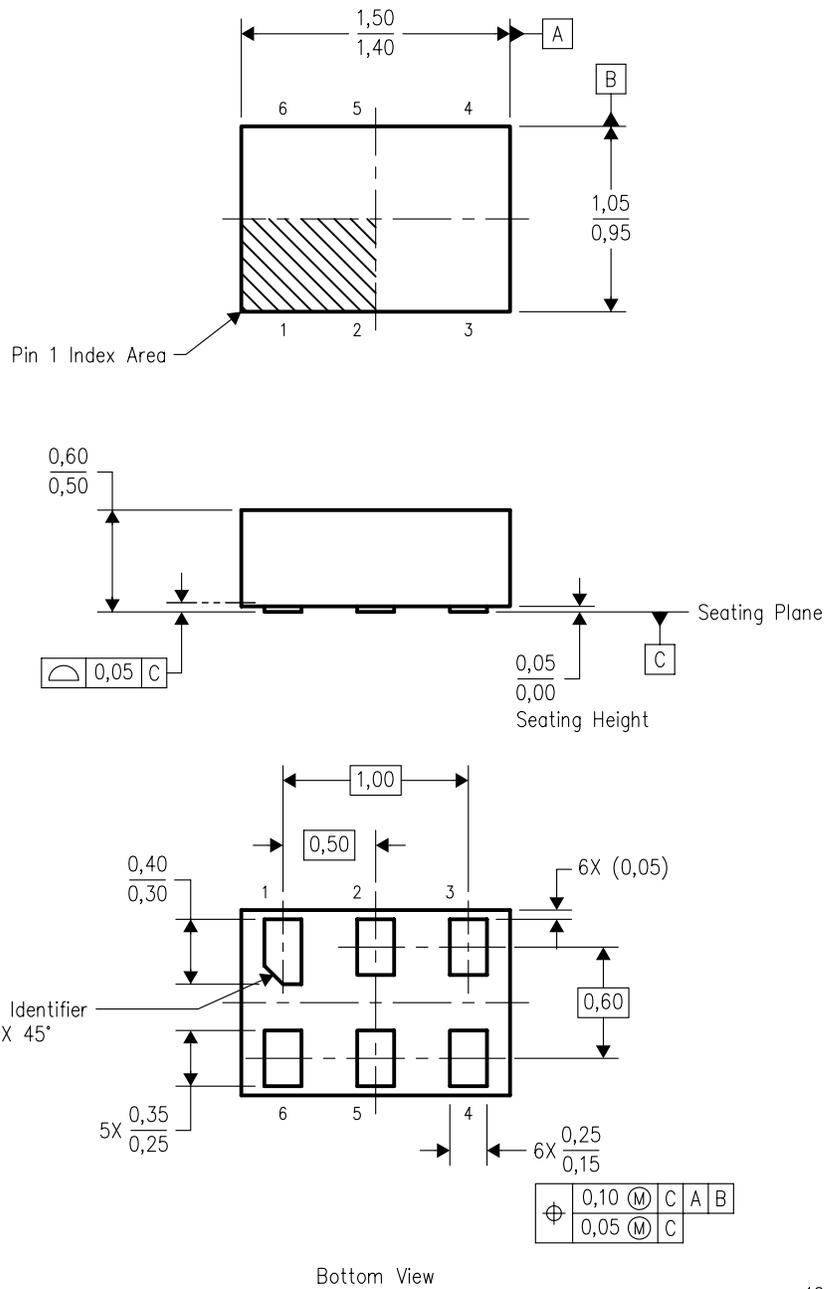
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.

DRY (R-PDSO-N6)

PLASTIC SMALL OUTLINE

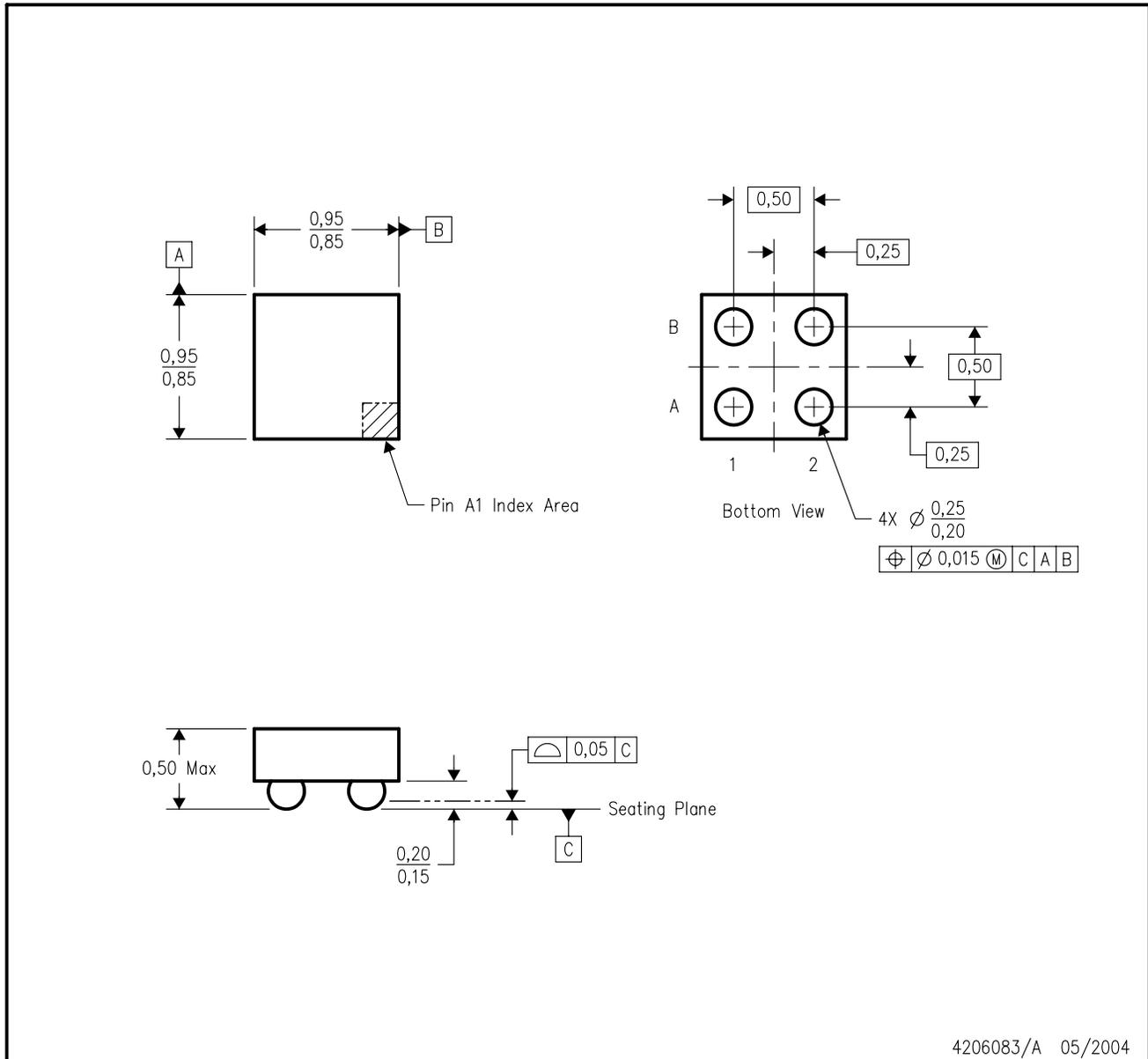


4207181/A 07/2005

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Reference JEDEC MO-252.

YZV (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package contains lead-free balls. Refer to the 4 YEV package (drawing 4206082) for tin-lead (SnPb) balls.

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