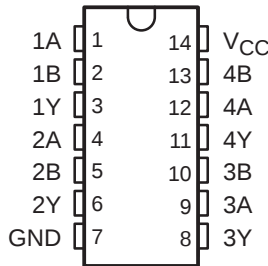


SN54LVC00A, SN74LVC00A QUADRUPLE 2-INPUT POSITIVE-NAND GATES

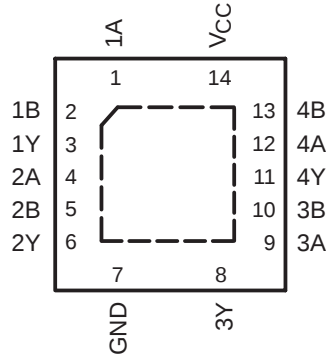
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- Operate From 1.65 V to 3.6 V
- Specified From -40°C to 85°C , -40°C to 125°C , and -55°C to 125°C
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.3 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) $<0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $>2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

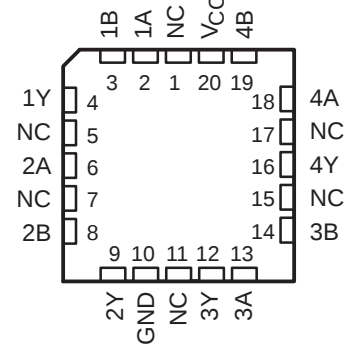
SN54LVC00A ... J OR W PACKAGE
SN74LVC00A ... D, DB, NS, OR PW PACKAGE
(TOP VIEW)



SN74LVC00A ... RGY PACKAGE
(TOP VIEW)



SN54LVC00A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The SN54LVC00A quadruple 2-input positive-NAND gate is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC00A quadruple 2-input positive-NAND gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The 'LVC00A devices perform the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC00ARGYR	LC00A
-40°C to 125°C	SOIC – D	Tube of 50	SN74LVC00AD	LVC00A
		Reel of 2500	SN74LVC00ADR	
		Reel of 250	SN74LVC00ADT	
	SOP – NS	Reel of 2000	SN74LVC00ANSR	LVC00A
	SSOP – DB	Reel of 2000	SN74LVC00ADBR	LC00A
-55°C to 125°C	TSSOP – PW	Tube of 90	SN74LVC00APW	LC00A
		Reel of 2000	SN74LVC00APWR	
		Reel of 250	SN74LVC00APWT	
	CDIP – J	Tube of 25	SNJ54LVC00AJ	SNJ54LVC00AJ
	CFP – W	Tube of 150	SNJ54LVC00AW	SNJ54LVC00AW
	LCCC – FK	Tube of 55	SNJ54LVC00AFK	SNJ54LVC00AFK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVC00A, SN74LVC00A
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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FUNCTION TABLE
(each gate)

INPUTS		OUTPUT Y
A	B	
H	H	L
L	X	H
X	L	H

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	86°C/W
(see Note 3): DB package	96°C/W
(see Note 3): NS package	76°C/W
(see Note 3): PW package	113°C/W
(see Note 4): RGY package	47°C/W
Storage temperature range, T_{stg}	–65°C to 150°C
Power dissipation, P_{tot} ($T_A = -40^\circ\text{C}$ to 125°C) (see Notes 5 and 6)	500 mW

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.
 5. For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.
 6. For the DB, NS, and PW packages: above 60°C, the value of P_{tot} derates linearly with 5.5 mW/K.

SN54LVC00A, SN74LVC00A QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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recommended operating conditions (see Note 7)

			SN54LVC00A		UNIT
			-55 TO 125°C		
			MIN	MAX	
V _{CC}	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V	0.8		V
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V	-12		mA
		V _{CC} = 3 V	-24		
I _{OL}	Low-level output current	V _{CC} = 2.7 V	12		mA
		V _{CC} = 3 V	24		

NOTE 7: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions (see Note 7)

		SN74LVC00A						UNIT
		T _A = 25°C		−40 TO 85°C		−40 TO 125°C		
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC} Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
	Data retention only	1.5		1.5		1.5		
V _{IH} High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65×V _{CC}		0.65×V _{CC}		0.65×V _{CC}		V
	V _{CC} = 2.3 V to 2.7 V	1.7		1.7		1.7		
	V _{CC} = 2.7 V to 3.6 V	2		2		2		
V _{IL} Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.35×V _{CC}		0.35×V _{CC}		0.35×V _{CC}	V
	V _{CC} = 2.3 V to 2.7 V		0.7		0.7		0.7	
	V _{CC} = 2.7 V to 3.6 V		0.8		0.8		0.8	
V _I Input voltage		0	5.5	0	5.5	0	5.5	V
V _O Output voltage		0	V _{CC}	0	V _{CC}	0	V _{CC}	V
I _{OH} High-level output current	V _{CC} = 1.65 V		−4		−4		−4	mA
	V _{CC} = 2.3 V		−8		−8		−8	
	V _{CC} = 2.7 V		−12		−12		−12	
	V _{CC} = 3 V		−24		−24		−24	
I _{OL} Low-level output current	V _{CC} = 1.65 V		4		4		4	mA
	V _{CC} = 2.3 V		8		8		8	
	V _{CC} = 2.7 V		12		12		12	
	V _{CC} = 3 V		24		24		24	

NOTE 7: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVC00A, SN74LVC00A

QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC00A		UNIT
			–55 TO 125°C		
			MIN	MAX	
V _{OH}	I _{OH} = –100 μA	2.7 V to 3.6 V	V _{CC} –0.2		V
	I _{OH} = –12 mA	2.7 V	2.2		
		3 V	2.4		
	I _{OH} = –24 mA	3 V	2.2		
V _{OL}	I _{OL} = 100 μA	2.7 V to 3.6 V	0.2		V
	I _{OL} = 12 mA	2.7 V	0.4		
	I _{OL} = 24 mA	3 V	0.55		
I _I	V _I = 5.5 V or GND	3.6 V	±5		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10		μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500		μA

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN74LVC00A						UNIT	
			T _A = 25°C			–40 TO 85°C		–40 TO 125°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V	V _{CC} –0.2			V _{CC} –0.2		V _{CC} –0.3		V
	I _{OH} = –4 mA	1.65 V	1.29			1.2		1.05		
	I _{OH} = –8 mA	2.3 V	1.9			1.7		1.55		
	I _{OH} = –12 mA	2.7 V	2.2			2.2		2.05		
		3 V	2.4			2.4		2.25		
	I _{OH} = –24 mA	3 V	2.3			2.2		2		
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V	0.1			0.2		0.3		V
	I _{OL} = 4 mA	1.65 V	0.24			0.45		0.6		
	I _{OL} = 8 mA	2.3 V	0.3			0.7		0.85		
	I _{OL} = 12 mA	2.7 V	0.4			0.4		0.6		
	I _{OL} = 24 mA	3 V	0.55			0.55		0.8		
I _I	V _I = 5.5 V or GND	3.6 V	±1			±5		±20		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	1			10		40		μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500		5000		μA
C _i	V _I = V _{CC} or GND	3.3 V	5							pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN54LVC00A		UNIT
				–55 TO 125°C		
				MIN	MAX	
t _{pd}	A or B	Y	2.7 V	5.1		ns
			3.3 V ± 0.3 V	1	4.3	



SN54LVC00A, SN74LVC00A QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN74LVC00A							UNIT
				T _A = 25°C			–40 TO 85°C		–40 TO 125°C		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	1.8 V ± 0.15 V	1	6	12	1	12.5	1	14	ns
			2.5 V ± 0.2 V	1	4.6	5.9	1	6.4	1	7.9	
			2.7 V	1	4.3	4.9	1	5.1	1	6.5	
			3.3 V ± 0.3 V	1	3.5	4.1	1	4.3	1	5.5	
t _{sk(o)}			3.3 V ± 0.3 V				1		1.5		ns

operating characteristics, T_A = 25°C

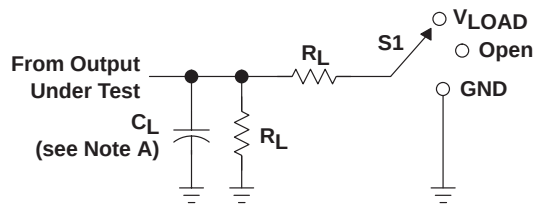
PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	f = 10 MHz	1.8 V	18	pF
			2.5 V	18	
			3.3 V	19	



SN54LVC00A, SN74LVC00A QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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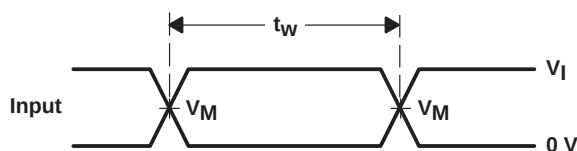
PARAMETER MEASUREMENT INFORMATION



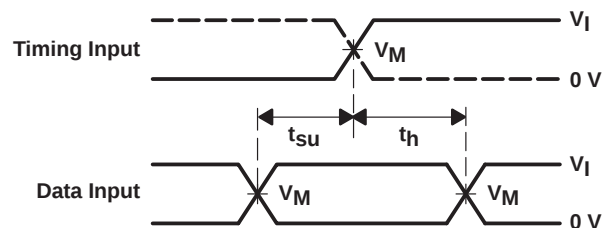
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

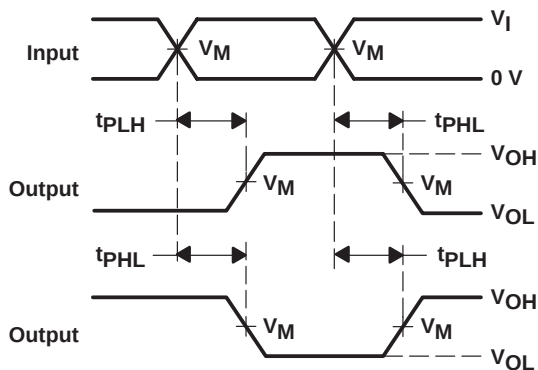
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



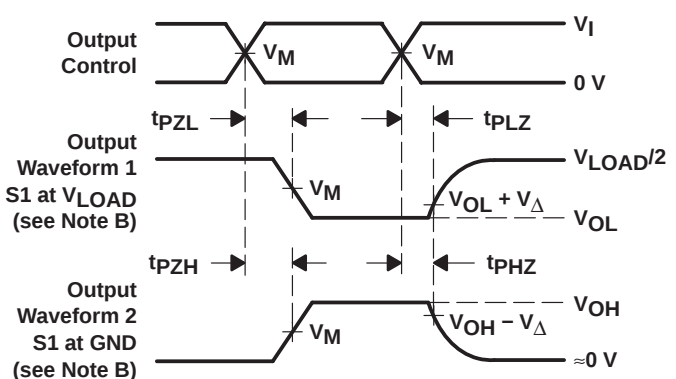
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

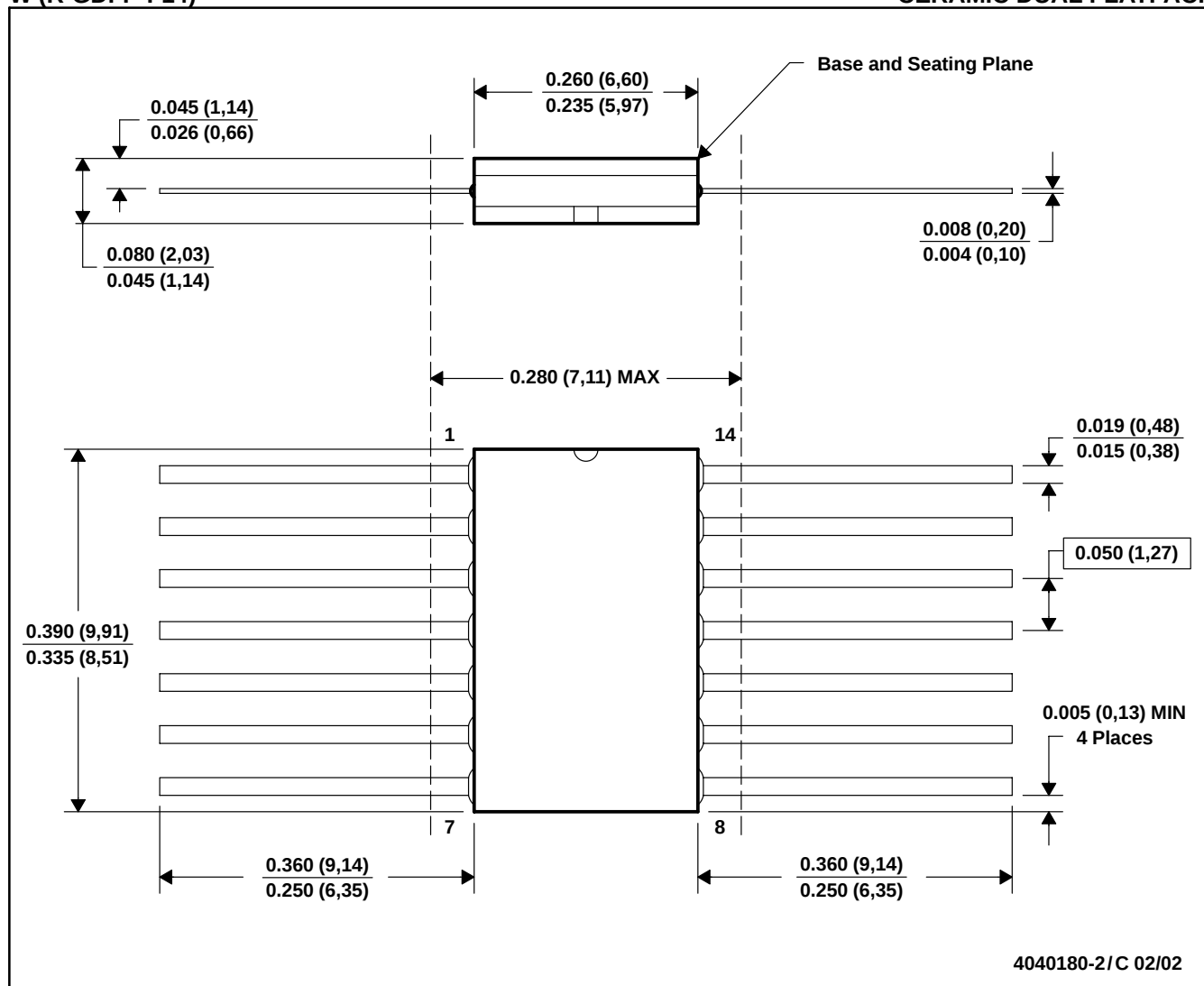


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

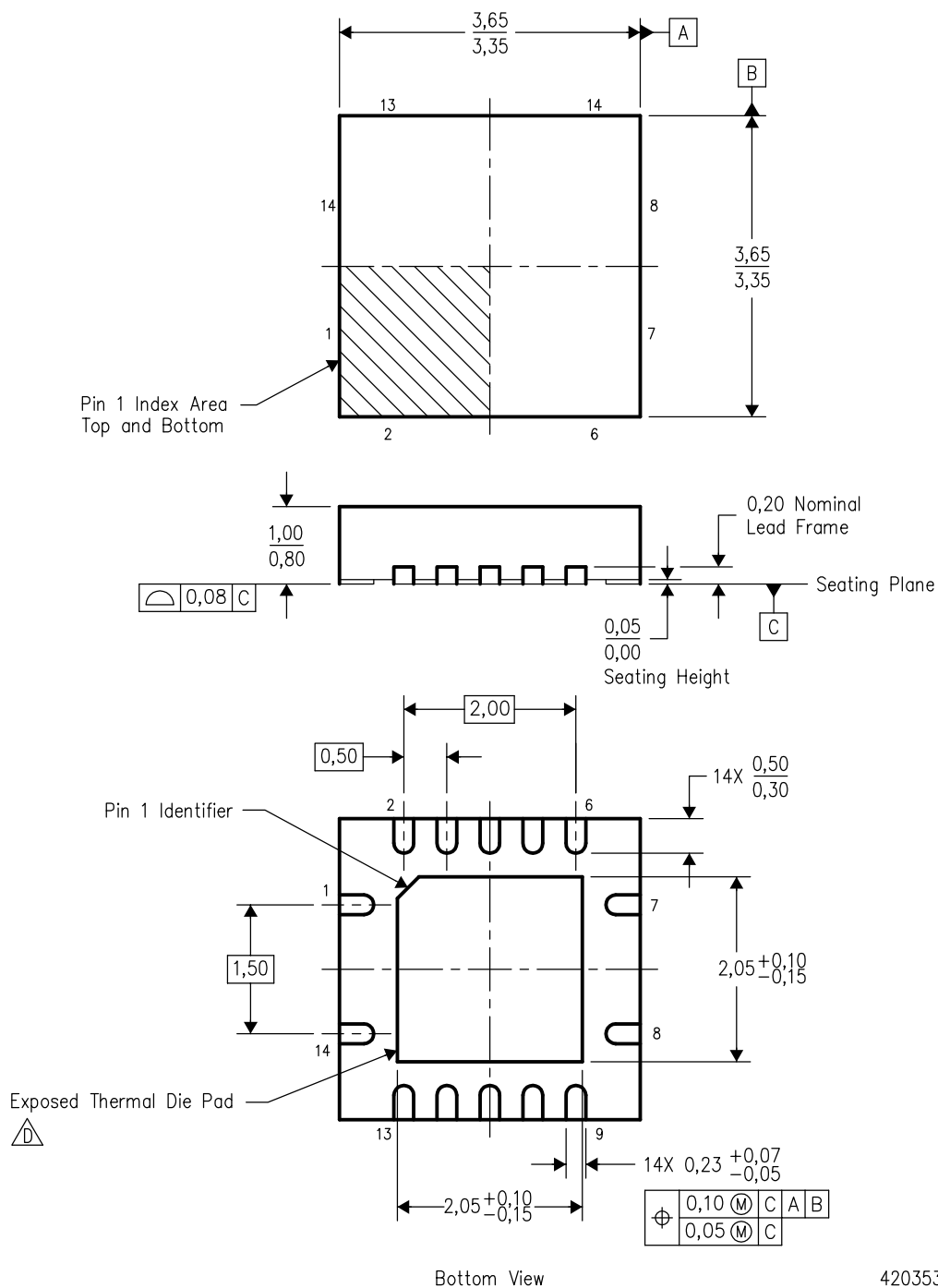
28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK

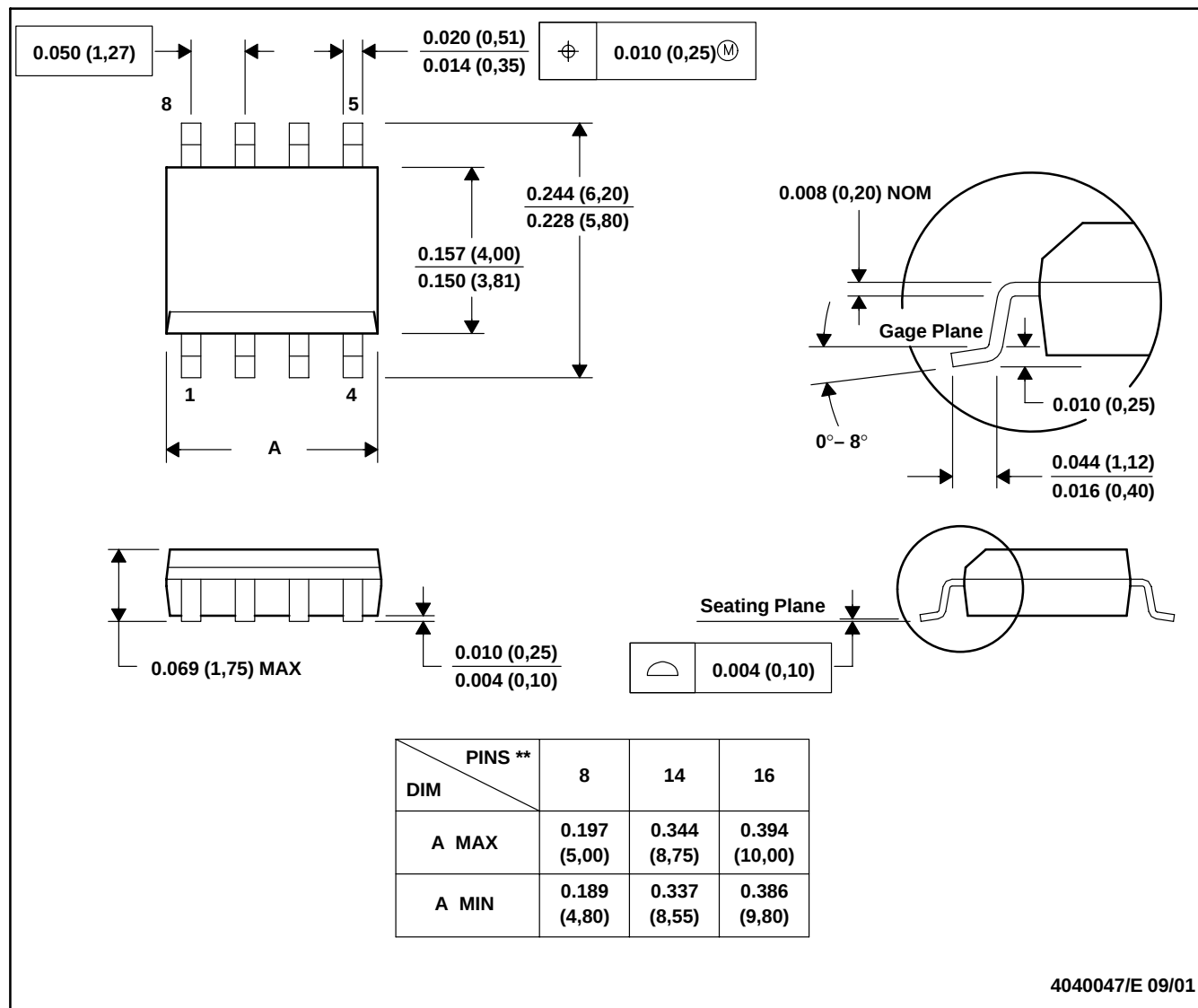


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 -  D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
 - E. Package complies to JEDEC MO-241 variation BA.

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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