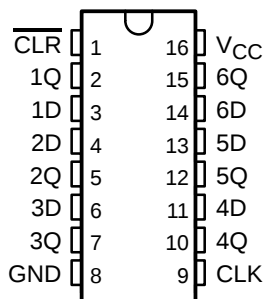


SN54ALS174, SN54ALS175, SN54AS174, SN54AS175B SN74ALS174, SN74ALS175, SN74AS174, SN74AS175B HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

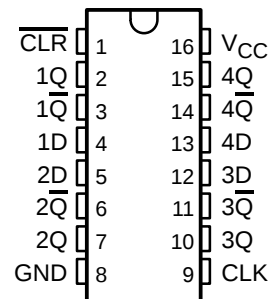
SDAS207E - APRIL 1982 - REVISED MAY 2002

- 'ALS174 and 'AS174 Contain Six Flip-Flops With Single-Rail Outputs
- 'ALS175 and 'AS175B Contain Four Flip-Flops With Double-Rail Outputs
- Buffered Clock and Direct-Clear Inputs
- Applications Include:
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators
- Fully Buffered Outputs for Maximum Isolation From External Disturbances ('AS Only)

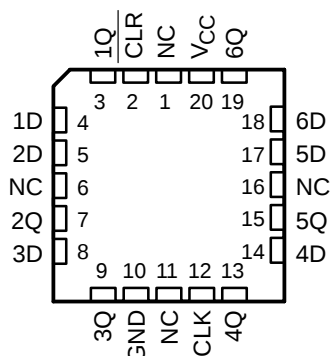
SN54ALS174 . . . J OR W PACKAGE
SN54AS174 . . . J PACKAGE
SN74ALS174, SN74AS174 . . . D, N, OR NS PACKAGE
(TOP VIEW)



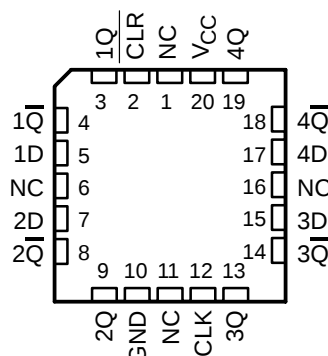
SN54ALS175 . . . J OR W PACKAGE
SN54AS175B . . . J PACKAGE
SN74ALS175, SN74AS175B . . . D, N, OR NS PACKAGE
(TOP VIEW)



SN54ALS174, SN54AS174 . . . FK PACKAGE
(TOP VIEW)



SN54ALS175 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct-clear ($\overline{\text{CLR}}$) input. The 'ALS175 and 'AS175B feature complementary outputs from each flip-flop.

Information at the data (D) inputs meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2002, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54ALS174, SN54ALS175, SN54AS174, SN54AS175B
SN74ALS174, SN74ALS175, SN74AS174, SN74AS175B
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR**

SDAS207E - APRIL 1982 - REVISED MAY 2002

ORDERING INFORMATION

T _A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74ALS174N	SN74ALS174N
			SN74AS174N	SN74AS174N
			SN74ALS175N	SN74ALS175N
			SN74AS175BN	SN74AS175BN
	SOIC – D	Tube	SN74ALS174D	ALS174
		Tape and reel	SN74ALS174DR	
		Tube	SN74AS174D	AS174
		Tape and reel	SN74AS174DR	
		Tube	SN74ALS175D	ALS175
		Tape and reel	SN74ALS175DR	
		Tube	SN74AS175BD	AS175B
		Tape and reel	SN74AS175BDR	
	SOP – NS	Tape and reel	SN74ALS174NSR	ALS174
			SN74AS174NSR	74AS174
			SN74ALS175NSR	ALS175
			SN74AS175BNSR	74AS175B
–55°C to 125°C	CDIP – J	Tube	SNJ54ALS174J	SNJ54ALS174J
			SNJ54AS174J	SNJ54AS174J
			SNJ54ALS175J	SNJ54ALS175J
			SNJ54AS175BJ	SNJ54AS175BJ
	CFP – W	Tube	SNJ54ALS174W	SNJ54ALS174W
			SNJ54ALS175W	SNJ54ALS175W
	LCCC – FK	Tube	SNJ54ALS174FK	SNJ54ALS174FK
			SNJ54ALS175FK	SNJ54ALS175FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

[‡] This orderable is not recommended for new designs.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUTS	
$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}^{\S}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q ₀	$\overline{\text{Q}}_0$

[§] 'ALS175 and 'AS175B only

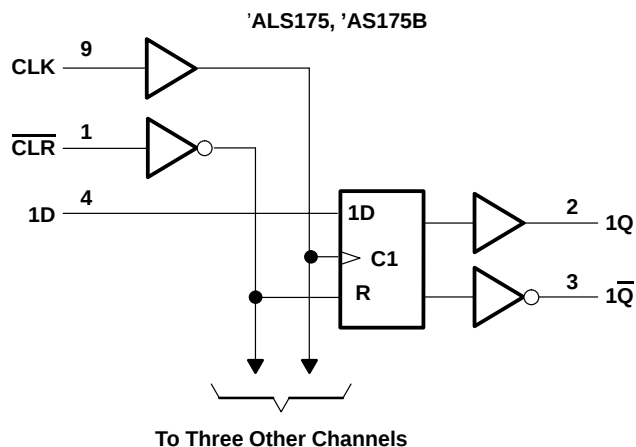
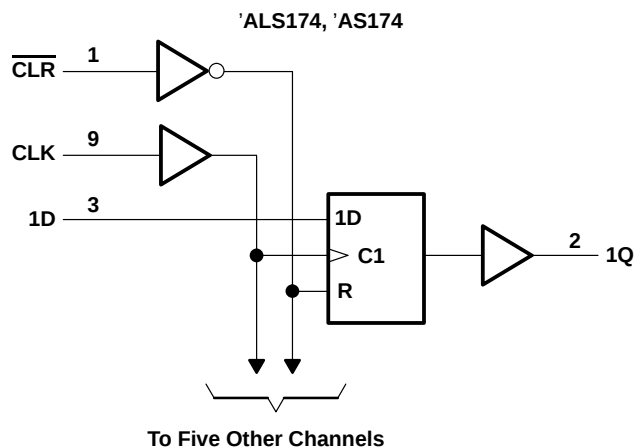


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ALS174, SN54ALS175, SN54AS174, SN54AS175B SN74ALS174, SN74ALS175, SN74AS174, SN74AS175B HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SDAS207E - APRIL 1982 - REVISED MAY 2002

logic diagrams (positive logic)



Pin numbers shown are for the D, J, N, NS, and W packages.

absolute maximum ratings over operating free-air temperature range, SN54/74ALS174, SN54/74ALS175 (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Package thermal impedance, θ_{JA} (see Note 1): D package	73°C/W
N package	67°C/W
NS package	64°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

		SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–0.4			–0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**SN54ALS174, SN54ALS175, SN54AS174, SN54AS175B
SN74ALS174, SN74ALS175, SN74AS174, SN74AS175B
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR**

SDAS207E - APRIL 1982 - REVISED MAY 2002

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA		−1.5			−1.5			V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = −0.4 mA		V _{CC} −2			V _{CC} −2			V
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 4 mA	0.25 0.4		0.25 0.4		0.35 0.5		V
			I _{OL} = 8 mA							
I _I		V _{CC} = 5.5 V, V _I = 7 V		0.1			0.1			mA
I _{IH}		V _{CC} = 5.5 V, V _I = 2.7 V		20			20			μA
I _{IL}	All others	V _{CC} = 5.5 V, V _I = 0.4 V		−0.1			−0.1			mA
	CLK			−0.15						
I _O ‡		V _{CC} = 5.5 V, V _O = 2.25 V		−20 −112		−30 −112		mA		
I _{CC}	'ALS174	V _{CC} = 5.5 V, See Note 3		11 19		11 19		mA		
	'ALS175			8 14		9 14				

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.

NOTE 3: I_{CC} is measured with D inputs and CLR grounded, and CLK at 4.5 V.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			SN54ALS174 SN54ALS175		SN74ALS174 SN74ALS175		UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		40		50		MHz
t _w	Pulse duration	CLR low	15		10		ns
		CLK high	12.5		10		
		CLK low	12.5		10		
t _{su}	Setup time before CLK↑	Data	15		10		ns
		CLR inactive	8		6		
t _h	Hold time, data after CLK↑		0		0		ns

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX [§]				UNIT
			SN54ALS174 SN54ALS175		SN74ALS174 SN74ALS175		
			MIN	MAX	MIN	MAX	
f _{max}			40		50		MHz
t _{PLH}	$\overline{\text{CLR}}$	Any Q (or $\overline{\text{Q}}$, 'ALS175)	3	20	5	18	ns
t _{PHL}			5	30	8	23	
t _{PLH}	CLK	Any Q (or $\overline{\text{Q}}$, 'ALS175)	3	20	3	15	ns
t _{PHL}			5	24	5	17	

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS174, SN54ALS175, SN54AS174, SN54AS175B SN74ALS174, SN74ALS175, SN74AS174, SN74AS175B HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SDAS207E - APRIL 1982 - REVISED MAY 2002

absolute maximum ratings over operating free-air temperature range, SN54/74AS174, SN54/74AS175B (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Package thermal impedance, θ_{JA} (see Note 1): D package	73°C/W
N package	67°C/W
NS package	64°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

		SN54AS174 SN54AS175B			SN74AS174 SN74AS175B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–2			–2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS174 SN54AS175B			SN74AS174 SN74AS175B			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2			–1.2	V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -2$ mA	$V_{CC}-2$			$V_{CC}-2$			V
V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 20$ mA	0.35	0.5		0.35	0.5		V
I_I	$V_{CC} = 5.5$ V, $V_I = 7$ V		0.1			0.1		mA
I_{IH}	$V_{CC} = 5.5$ V, $V_I = 2.7$ V		20			20		μA
I_{IL}	$V_{CC} = 5.5$ V, $V_I = 0.4$ V		–0.5			–0.5		mA
$I_{O}^{\S}$	$V_{CC} = 5.5$ V, $V_O = 2.25$ V	–30		–112	–30		–112	mA
I_{CC}	'AS174		30	45		30	45	mA
	'AS175B		22.5	34		22.5	34	

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

^{\S} The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

NOTE 4: I_{CC} is measured with D inputs, CLR, and CLK grounded.



**SN54ALS174, SN54ALS175, SN54AS174, SN54AS175B
SN74ALS174, SN74ALS175, SN74AS174, SN74AS175B
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR**

SDAS207E - APRIL 1982 - REVISED MAY 2002

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

				SN54AS174 SN54AS175B		SN74AS174 SN74AS175B		UNIT	
				MIN	MAX	MIN	MAX		
f _{clock} *	Clock frequency			100		100		MHz	
t _w *	Pulse duration		CLR low		5.5		5		ns
			CLK high		4		4		
			CLK low	'AS174	6		6		
			CLK low	'AS175B	5		5		
t _{su} *	Setup time before CLK↑		Data	'AS174	4		4		ns
				'AS175B	3		3		
			CLR inactive		6		6		
t _h *	Hold time, data after CLK↑			1		1		ns	

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data, but is not production tested.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54AS174		SN74AS174		
			MIN	MAX	MIN	MAX	
f _{max} *			100		100		MHz
t _{PHL}	$\overline{\text{CLR}}$	Any Q	5	15	5	14	ns
t _{PLH}	CLK	Any Q	3.5	9.5	3.5	8	ns
t _{PHL}			4.5	11.5	4.5	10	

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data, but is not production tested.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Figure 1)

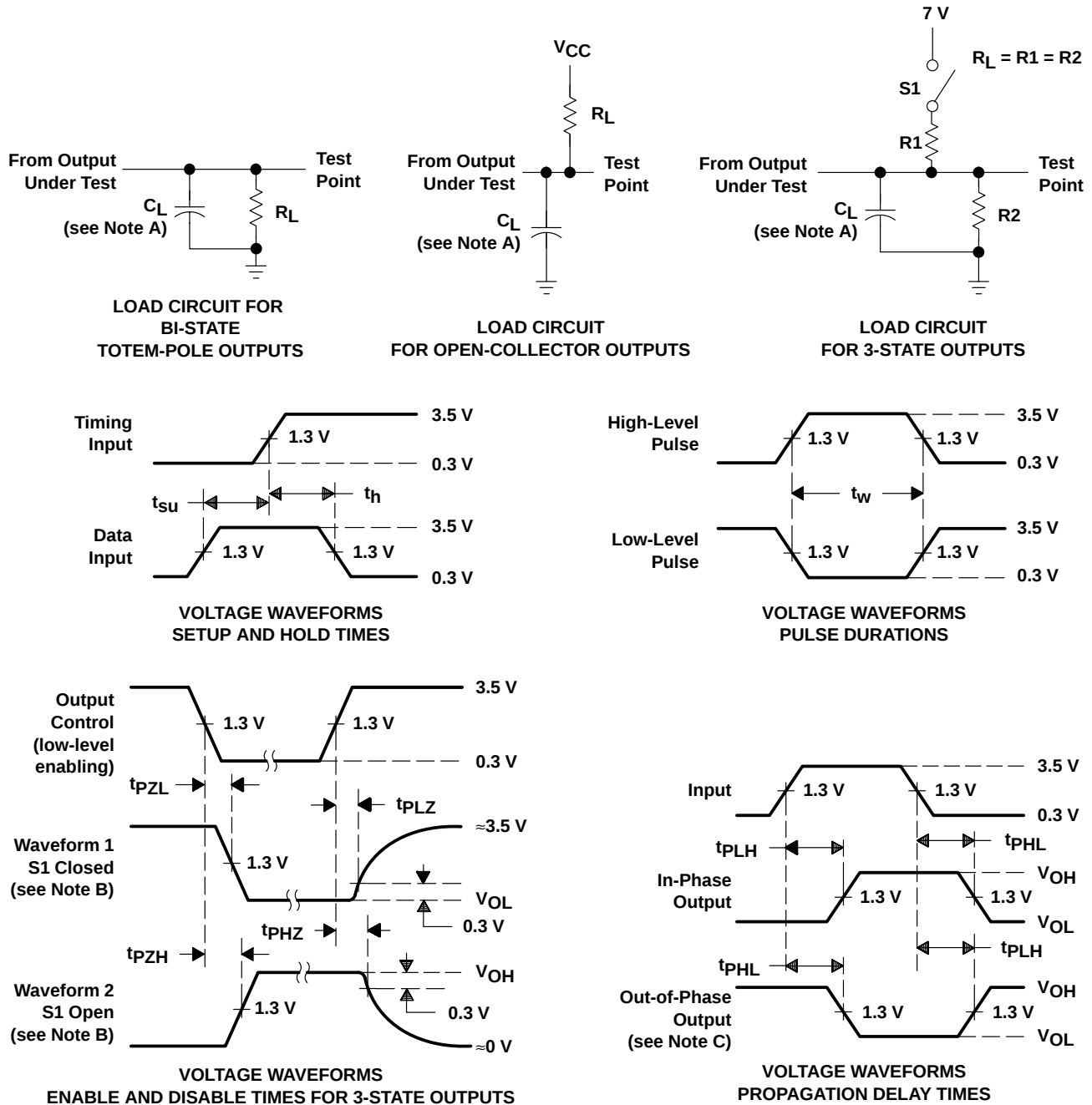
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54AS175B		SN74AS175B		
			MIN	MAX	MIN	MAX	
f _{max} *			100		100		MHz
t _{PLH}	$\overline{\text{CLR}}$	Any Q or $\overline{\text{Q}}$	4	10	4	9	ns
t _{PHL}			4.5	15	4.5	13	
t _{PLH}	CLK	Any Q or $\overline{\text{Q}}$	3	8.5	3	7.5	ns
t _{PHL}			3	11	3	10	

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data, but is not production tested.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



PARAMETER MEASUREMENT INFORMATION
 SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9553701Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9553701QEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
83019012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
8301901EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
8301901FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
83019022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
8301902EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
8301902FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
JM38510/37201B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/37201BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/37202B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/37202BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54ALS174J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54ALS175J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54AS174J	OBSOLETE	CDIP	J	16		TBD	A42 SNPB	N / A for Pkg Type
SN54AS175BJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI
SN74ALS174D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS174DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS174DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS174DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS174DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS174DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS174N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS174N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74ALS174NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS174NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS174NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS175D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS175DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS175DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS175DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS175DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
no Sb/Br)								
SN74ALS175DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS175N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS175NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS175NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS175NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS174D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74AS174DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74AS174DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74AS174DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74AS174N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS174NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS174NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS174NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS175BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS175BDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS175BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS175BDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS175BN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS175BNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS175BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS175BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ALS174FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54ALS174J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54ALS174W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54ALS175FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54ALS175J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54ALS175W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54AS174FK	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SNJ54AS174J	NRND	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54AS175BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54AS175BJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2006, Texas Instruments Incorporated