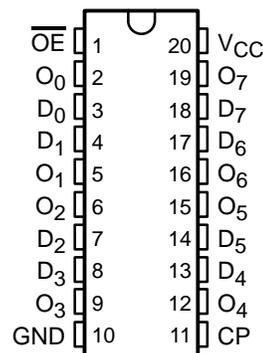


CY54FCT374T, CY74FCT374T 8-BIT REGISTERS WITH 3-STATE OUTPUTS

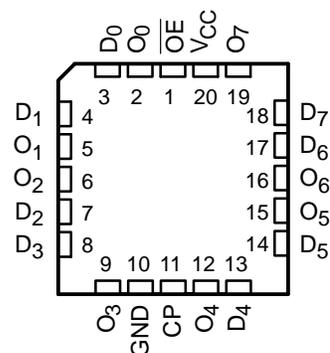
SCCS022A – MAY 1994 – REVISED OCTOBER 2001

- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Edge-Triggered D-Type Inputs
- 250-MHz Typical Switching Rate
- CY54FCT374T
 - 32-mA Output Sink Current
 - 12-mA Output Source Current
- CY74FCT374T
 - 64-mA Output Sink Current
 - 32-mA Output Source Current
- 3-State Outputs

CY54FCT374T . . . D PACKAGE
CY74FCT374T . . . P, Q, OR SO PACKAGE
(TOP VIEW)



CY54FCT374T . . . L PACKAGE
(TOP VIEW)



description

The 'FCT374T devices are high-speed, low-power, octal D-type flip-flops, featuring separate D-type inputs for each flip-flop. These devices have 3-state outputs for bus-oriented applications. A buffered clock (CP) and output-enable (\overline{OE}) inputs are common to all flip-flops. The eight flip-flops in the 'FCT374T store the state of their individual D inputs that meet the setup-time and hold-time requirements on the low-to-high CP transition. When \overline{OE} is low, the contents of the eight flip-flops are available at the outputs. When \overline{OE} is high, the outputs are in the high-impedance state. The state of \overline{OE} does not affect the state of the flip-flops.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

CY54FCT374T, CY74FCT374T
8-BIT REGISTERS
WITH 3-STATE OUTPUTS

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ORDERING INFORMATION

TA	PACKAGE†	SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
-40°C to 85°C	QSOP – Q	Tape and reel	5.2	CY74FCT374CTQCT	FCT374C
	SOIC – SO	Tube	5.2	CY74FCT374CTSOC	FCT374C
		Tape and reel	5.2	CY74FCT374CTSOCT	
	DIP – P	Tube	6.5	CY74FCT374ATPC	CY74FCT374ATPC
	QSOP – Q	Tape and reel	6.5	CY74FCT374ATQCT	FCT374A
	SOIC – SO	Tube	6.5	CY74FCT374ATSOC	FCT374A
		Tape and reel	6.5	CY74FCT374ATSOCT	
	QSOP – Q	Tape and reel	10	CY74FCT374TQCT	FCT374
SOIC – SO	Tube	10	CY74FCT374TSOC	FCT374	
	Tape and reel	10	CY74FCT374TSOCT		
-55°C to 125°C	CDIP – D	Tube	6.2	CY54FCT374CTDMB	
	LCC – L	Tube	6.2	CY54FCT374CTLMB	
	CDIP – D	Tube	7.2	CY54FCT374ATDMB	
	LCC – L	Tube	7.2	CY54FCT374ATLMB	
	CDIP – D	Tube	11	CY54FCT374TDMB	
	LCC – L	Tube	11	CY54FCT374TLMB	

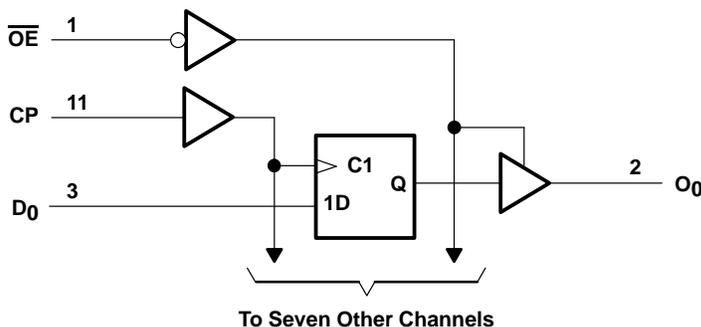
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			OUTPUT
D	CP	\overline{OE}	O
H	↑	L	H
L	↑	L	L
X	X	H	Z

H = High logic level, L = Low logic level,
X = Don't care, Z = High-impedance state,
↑ = Low-to-high clock transition

logic diagram (positive logic)



CY54FCT374T, CY74FCT374T

8-BIT REGISTERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY54FCT374T			CY74FCT374T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _{IN} = -18 mA	-0.7	-1.2					V
	V _{CC} = 4.75 V, I _{IN} = -18 mA				-0.7	-1.2		
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -12 mA	2.4	3.3					V
	V _{CC} = 4.75 V	I _{OH} = -32 mA			2			
		I _{OH} = -15 mA			2.4	3.3		
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 32 mA		0.3	0.55				V
	V _{CC} = 4.75 V, I _{OL} = 64 mA				0.3	0.55		
V _{hys}	All inputs		0.2		0.2			V
I _I	V _{CC} = 5.5 V, V _{IN} = V _{CC}			5				μA
	V _{CC} = 5.25 V, V _{IN} = V _{CC}					5		
I _{IH}	V _{CC} = 5.5 V, V _{IN} = 2.7 V			±1				μA
	V _{CC} = 5.25 V, V _{IN} = 2.7 V					±1		
I _{IL}	V _{CC} = 5.5 V, V _{IN} = 0.5 V			±1				μA
	V _{CC} = 5.25 V, V _{IN} = 0.5 V					±1		
I _{off}	V _{CC} = 0 V, V _{OUT} = 4.5 V			±1			±1	μA
I _{OS} ‡	V _{CC} = 5.5 V, V _{OUT} = 0 V	-60	-120	-225				mA
	V _{CC} = 5.25 V, V _{OUT} = 0 V				-60	-120	-225	
I _{OZH}	V _{CC} = 5.5 V, V _{IN} = 2.7 V			10				μA
	V _{CC} = 5.25 V, V _{IN} = 2.7 V					10		
I _{OZL}	V _{CC} = 5.5 V, V _{IN} = 0.5 V			-10				μA
	V _{CC} = 5.25 V, V _{IN} = 0.5 V					-10		
I _{CC}	V _{CC} = 5.5 V, V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V		0.1	0.2				mA
	V _{CC} = 5.25 V, V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V				0.1	0.2		
ΔI _{CC}	V _{CC} = 5.5 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open		0.5	2				mA
	V _{CC} = 5.25 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open				0.5	2		

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND



CY54FCT374T, CY74FCT374T
8-BIT REGISTERS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS		CY54FCT374T		CY74FCT374T		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
I_{CCD}^{\ddagger}	$V_{CC} = 5.5$ V, Outputs open, One bit switching at 50% duty cycle, $\overline{OE} = GND$, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V			0.06	0.12			mA/ MHz
	$V_{CC} = 5.25$ V, Outputs open, One bit switching at 50% duty cycle, $\overline{OE} = GND$, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V					0.06	0.12	
I_C	$V_{CC} = 5.5$ V, $f_0 = 10$ MHz, Outputs open, $\overline{OE} = GND$	One bit switching at $f_1 = 5$ MHz at 50% duty cycle	$V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V	0.7	1.4			mA
			$V_{IN} = 3.4$ V or GND	1.2	3.4			
		Eight bits switching at $f_1 = 2.5$ MHz at 50% duty cycle	$V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V	1.6	3.2			
			$V_{IN} = 3.4$ V or GND	3.9	12.2			
	$V_{CC} = 5.25$ V, $f_0 = 10$ MHz, Outputs open, $\overline{OE} = GND$	One bit switching at $f_1 = 5$ MHz at 50% duty cycle	$V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V			0.7	1.4	
			$V_{IN} = 3.4$ V or GND			1.2	3.4	
		Eight bits switching at $f_1 = 2.5$ MHz at 50% duty cycle	$V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V			1.6	3.2	
			$V_{IN} = 3.4$ V or GND			3.9	12.2	
C_i			5	10	5	10	pF	
C_o			9	12	9	12	pF	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

‡ This parameter is derived for use in total power-supply calculations.

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input ($V_{IN} = 3.4$ V)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.



CY54FCT374T, CY74FCT374T
8-BIT REGISTERS
WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		CY54FCT374T		CY54FCT374AT		CY54FCT374CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, CP high or low	7		6		6		ns
t _{su}	Setup time, data before CP↑	2		2		2		ns
t _h	Hold time, data after CP↑	1.5		1.5		1.5		ns

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		CY74FCT374T		CY74FCT374AT		CY74FCT374CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, CP high or low	7		5		5		ns
t _{su}	Setup time, data before CP↑	2		2		2		ns
t _h	Hold time, data after CP↑	1.5		1.5		1.5		ns

switching characteristics over operating free-air temperature range (see Figure 1)

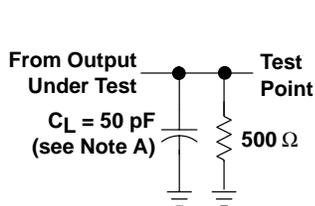
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT374T		CY54FCT374AT		CY54FCT374CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	CP	O	2	11	2	7.2	2	6.2	ns
t _{PHL}			2	11	2	7.2	2	6.2	
t _{PZH}	\overline{OE}	O	1.5	14	1.5	7.5	1.5	6.2	ns
t _{PZL}			1.5	14	1.5	7.5	1.5	6.2	
t _{PHZ}	\overline{OE}	O	1.5	8	1.5	6.5	1.5	5.7	ns
t _{PLZ}			1.5	8	1.5	6.5	1.5	5.7	

switching characteristics over operating free-air temperature range (see Figure 1)

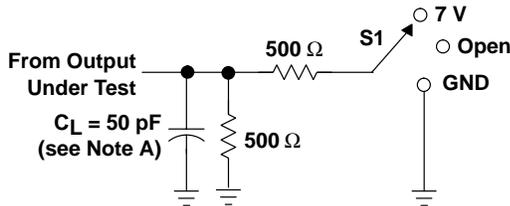
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT374T		CY74FCT374AT		CY74FCT374CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	CP	O	2	10	2	6.5	2	5.2	ns
t _{PHL}			2	10	2	6.5	2	5.2	
t _{PZH}	\overline{OE}	O	1.5	12.5	1.5	6.5	1.5	5.5	ns
t _{PZL}			1.5	12.5	1.5	6.5	1.5	5.5	
t _{PHZ}	\overline{OE}	O	1.5	8	1.5	5.5	1.5	5	ns
t _{PLZ}			1.5	8	1.5	5.5	1.5	5	



PARAMETER MEASUREMENT INFORMATION

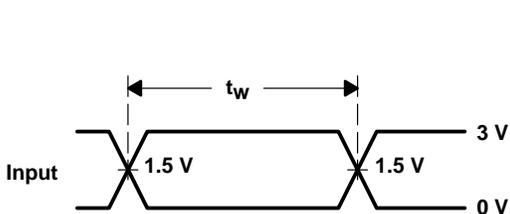


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

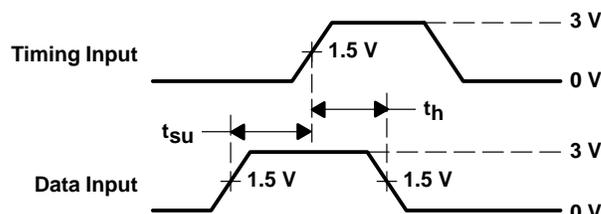


LOAD CIRCUIT FOR
3-STATE OUTPUTS

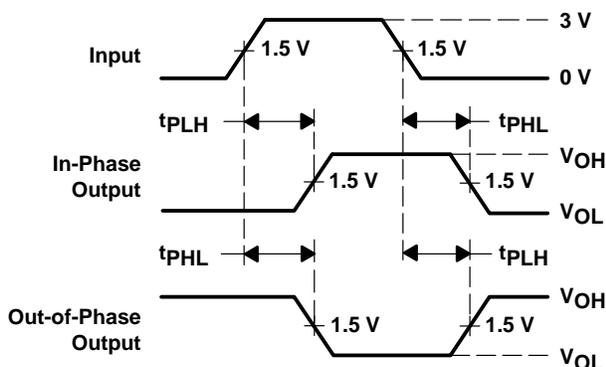
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



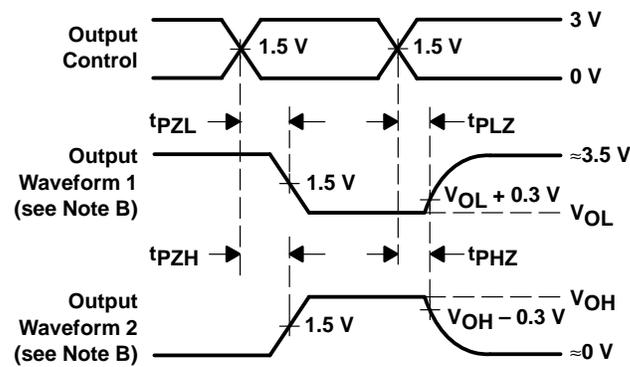
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9221802M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9221802MRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9221804MRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9221806M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9221806MRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9222203M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9222203MRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9222205MRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
CY54FCT374ATDMB	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
CY54FCT374CTLMB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
CY54FCT374TDMB	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
CY54FCT374TLMB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
CY54FCT574ATLMB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
CY74FCT374ATPC	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CY74FCT374ATPCE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CY74FCT374ATQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT374ATQCTE4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT374ATQCTG4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT374ATSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT374ATSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT374ATSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT374ATSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT374CTQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT374CTQCTE4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT374CTSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT374CTSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT374CTSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT374CTSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT374TQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT374TQCTE4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CY74FCT374TQCTG4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT374TSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT374TSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT374TSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT374TSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT574ATQCT	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT574ATQCTE4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT574ATQCTG4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT574ATSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT574ATSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT574ATSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT574ATSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT574CTQCT	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT574CTQCTE4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT574CTQCTG4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT574CTSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT574CTSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT574CTSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT574CTSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT574TQCT	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT574TQCTE4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT574TQCTG4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT574TSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT574TSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT574TSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT574TSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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