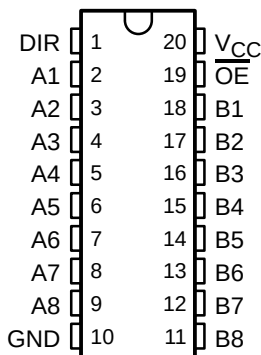


SN54LVCH245A, SN74LVCH245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

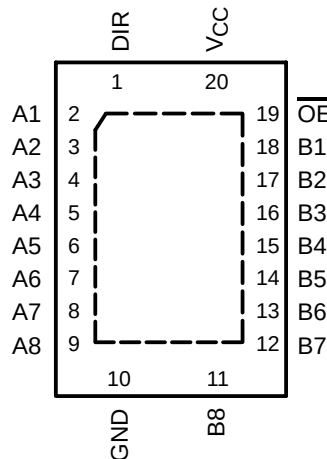
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- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 6.3 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- I_{off} Supports Partial-Power-Down Mode Operation
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

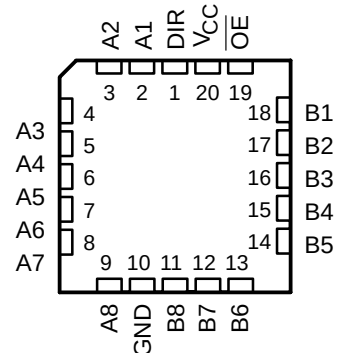
SN54LVCH245A . . . J OR W PACKAGE
SN74LVCH245A . . . DB, DGV, DW, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LVCH245A . . . RGY PACKAGE
(TOP VIEW)



SN54LVCH245A . . . FK PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74LVCH245ARGYR	LCH245A
	SOIC – DW	Tube	SN74LVCH245ADW	LVCH245A
		Tape and reel	SN74LVCH245ADWR	
	SOP – NS	Tape and reel	SN74LVCH245ANSR	LVCH245A
	SSOP – DB	Tape and reel	SN74LVCH245ADBR	LCH245A
	TSSOP – PW	Tape and reel	SN74LVCH245APWR	LCH245A
	TVSOP – DGV	Tape and reel	SN74LVCH245ADGVR	LCH245A
–55°C to 125°C	VFBGA – GQN	Tape and reel	SN74LVCH245AGQNR	LCH245A
	CDIP – J	Tube	SNJ54LVCH245AJ	SNJ54LVCH245AJ
	CFP – W	Tube	SNJ54LVCH245AW	SNJ54LVCH245AW
	LCCC – FK	Tube	SNJ54LVCH245AFK	SNJ54LVCH245AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVCH245A, SN74LVCH245A
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

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description/ordering information (continued)

The SN54LVCH245A octal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVCH245A octal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

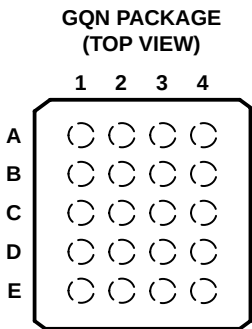
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

These devices are designed for asynchronous communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.



terminal assignments

	1	2	3	4
A	A1	DIR	V _{CC}	$\overline{OE}$
B	A3	B2	A2	B1
C	A5	A4	B4	B3
D	A7	B6	A6	B5
E	GND	A8	B8	B7

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Logic diagram for the 74147 decoder showing the internal structure for channels 18 and 19. The diagram includes inputs DIR (1) and A1 (2), and outputs 19 (OE) and 18 (B1). The logic involves two 3-input AND gates and two inverters. The outputs of the AND gates are connected to the outputs 19 and 18, and also to a common bus labeled "To Seven Other Channels".

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	70°C/W
(see Note 3): DGV package	92°C/W
(see Note 3): DW package	58°C/W
(see Note 3): GQN package	76°C/W
(see Note 3): NS package	60°C/W
(see Note 3): PW package	83°C/W
(see Note 4): RGY package	37°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

NOTES:

1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

SN54LVCH245A, SN74LVCH245A

OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 5)

		SN54LVCH245A		SN74LVCH245A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC} Supply voltage	Operating	2	3.6	1.65	3.6	V
	Data retention only	1.5		1.5		
V _{IH} High-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.65 × V _{CC}		V
	V _{CC} = 2.3 V to 2.7 V			1.7		
	V _{CC} = 2.7 V to 3.6 V	2		2		
V _{IL} Low-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.35 × V _{CC}		V
	V _{CC} = 2.3 V to 2.7 V			0.7		
	V _{CC} = 2.7 V to 3.6 V		0.8	0.8		
V _I Input voltage		0	5.5	0	5.5	V
V _O Output voltage	High or low state	0	V _{CC}	0	V _{CC}	V
	3-state	0	5.5	0	5.5	
I _{OH} High-level output current	V _{CC} = 1.65 V			–4		mA
	V _{CC} = 2.3 V			–8		
	V _{CC} = 2.7 V		–12	–12		
	V _{CC} = 3 V		–24	–24		
I _{OL} Low-level output current	V _{CC} = 1.65 V			4		mA
	V _{CC} = 2.3 V			8		
	V _{CC} = 2.7 V		12	12		
	V _{CC} = 3 V		24	24		
Δt/Δv Input transition rise or fall rate			10		10	ns/V
T _A Operating free-air temperature		–55	125	–40	85	°C

NOTE 5: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVCH245A, SN74LVCH245A

OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	SN54LVCH245A			SN74LVCH245A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V				V _{CC} –0.2			V	
		2.7 V to 3.6 V	V _{CC} –0.2							
	I _{OH} = –4 mA	1.65 V				1.2				
	I _{OH} = –8 mA	2.3 V				1.7				
	I _{OH} = –12 mA	2.7 V	2.2			2.2				
		3 V	2.4			2.4				
	I _{OH} = –24 mA	3 V	2.2			2.2				
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V				0.2			V	
		2.7 V to 3.6 V	0.2							
	I _{OL} = 4 mA	1.65 V				0.45				
	I _{OL} = 8 mA	2.3 V				0.7				
	I _{OL} = 12 mA	2.7 V	0.4			0.4				
	I _{OL} = 24 mA	3 V	0.55			0.55				
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V	±5			±5			μA
I _{off}		V _I or V _O = 5.5 V	0				±10			μA
I _I (hold)	V _I = 0.58 V	1.65 V				25			μA	
	V _I = 1.07 V		–25							
	V _I = 0.7 V	2.3 V				45				
	V _I = 1.7 V		–45							
	V _I = 0.8 V	3 V	75			75				
	V _I = 2 V		–75			–75				
	V _I = 0 to 3.6 V‡		3.6 V	±500			±500			
I _{OZ} §		V _O = 0 to 5.5 V	3.6 V	±15			±10			μA
I _{CC}	V _I = V _{CC} or GND	I _O = 0	3.6 V	10			10			μA
	3.6 V ≤ V _I ≤ 5.5 V¶			10			10			
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500			μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	4	12	4			pF	
C _{iO}	A or B ports	V _O = V _{CC} or GND	3.3 V	5.5	12	5.5			pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This is the bus-hold maximum dynamic current required to switch the input from one state to another.

[§] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[¶] This applies in the disabled state only.



SN54LVCH245A, SN74LVCH245A

OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVCH245A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	8		1	7	ns
t _{en}	$\overline{\text{OE}}$	A or B	9.5		1	8.5	ns
t _{dis}	$\overline{\text{OE}}$	A or B	8.5		1	7.5	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVCH245A								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	†	†	†	†	7.3		1.5	6.3	ns
t _{en}	$\overline{\text{OE}}$	A or B	†	†	†	†	9.5		1.5	8.5	ns
t _{dis}	$\overline{\text{OE}}$	A or B	†	†	†	†	8.5		1.7	7.5	ns
t _{sk(0)}									1		ns

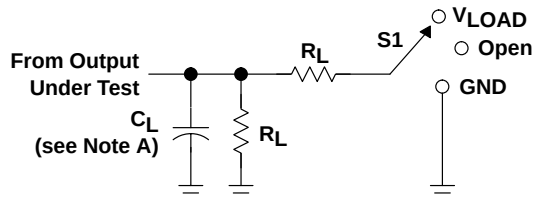
† This information was not available at the time of publication.

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per transceiver	Outputs enabled	f = 10 MHz	†	†	47	pF
		Outputs disabled		†	†	2	

† This information was not available at the time of publication.

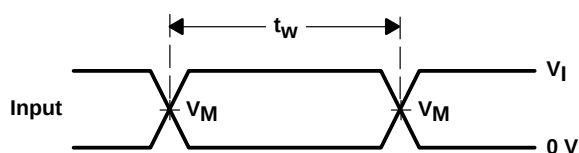
PARAMETER MEASUREMENT INFORMATION



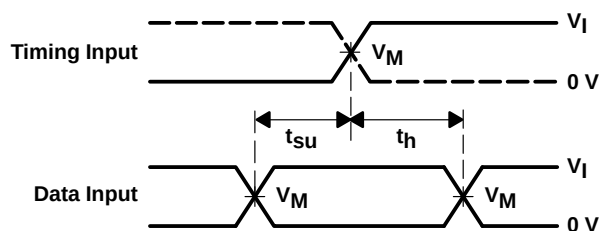
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

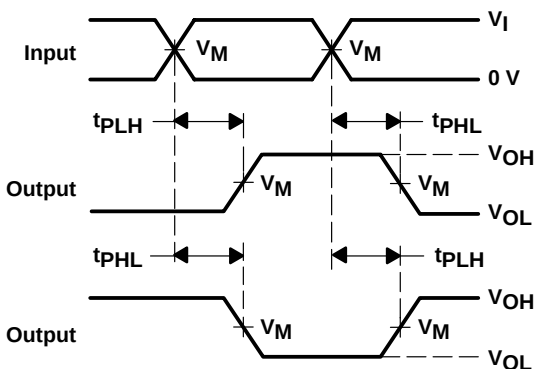
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



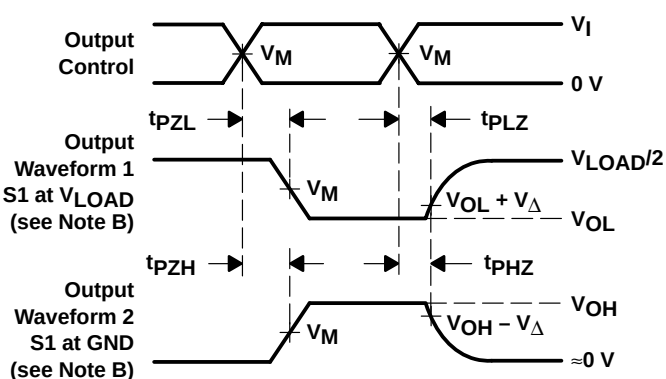
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

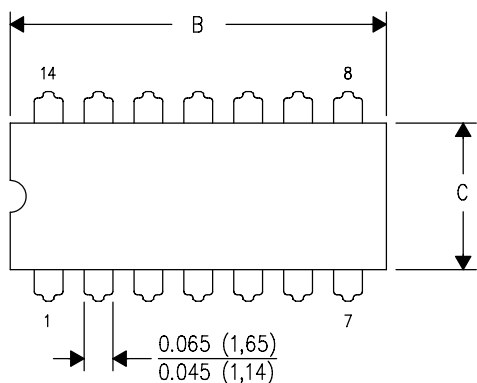
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

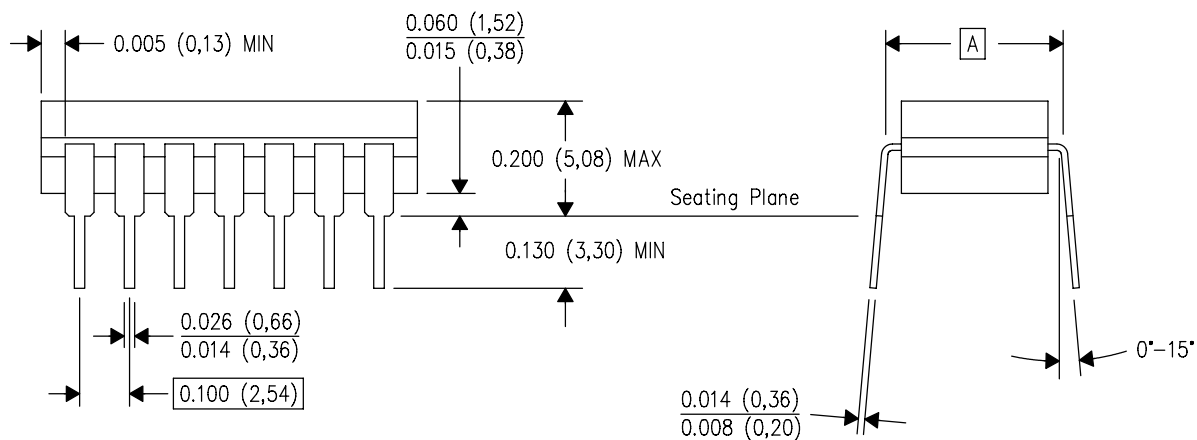
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

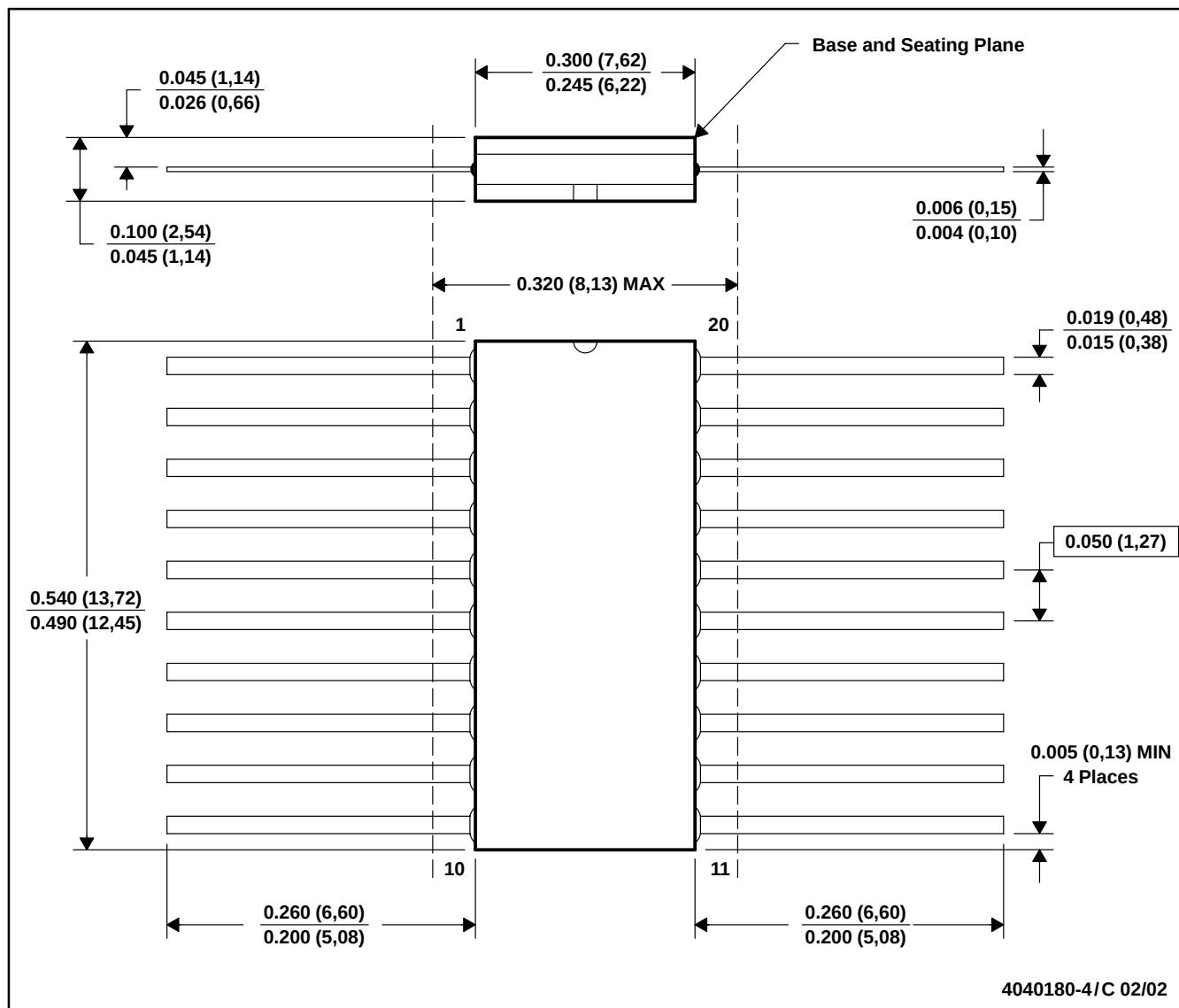


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK

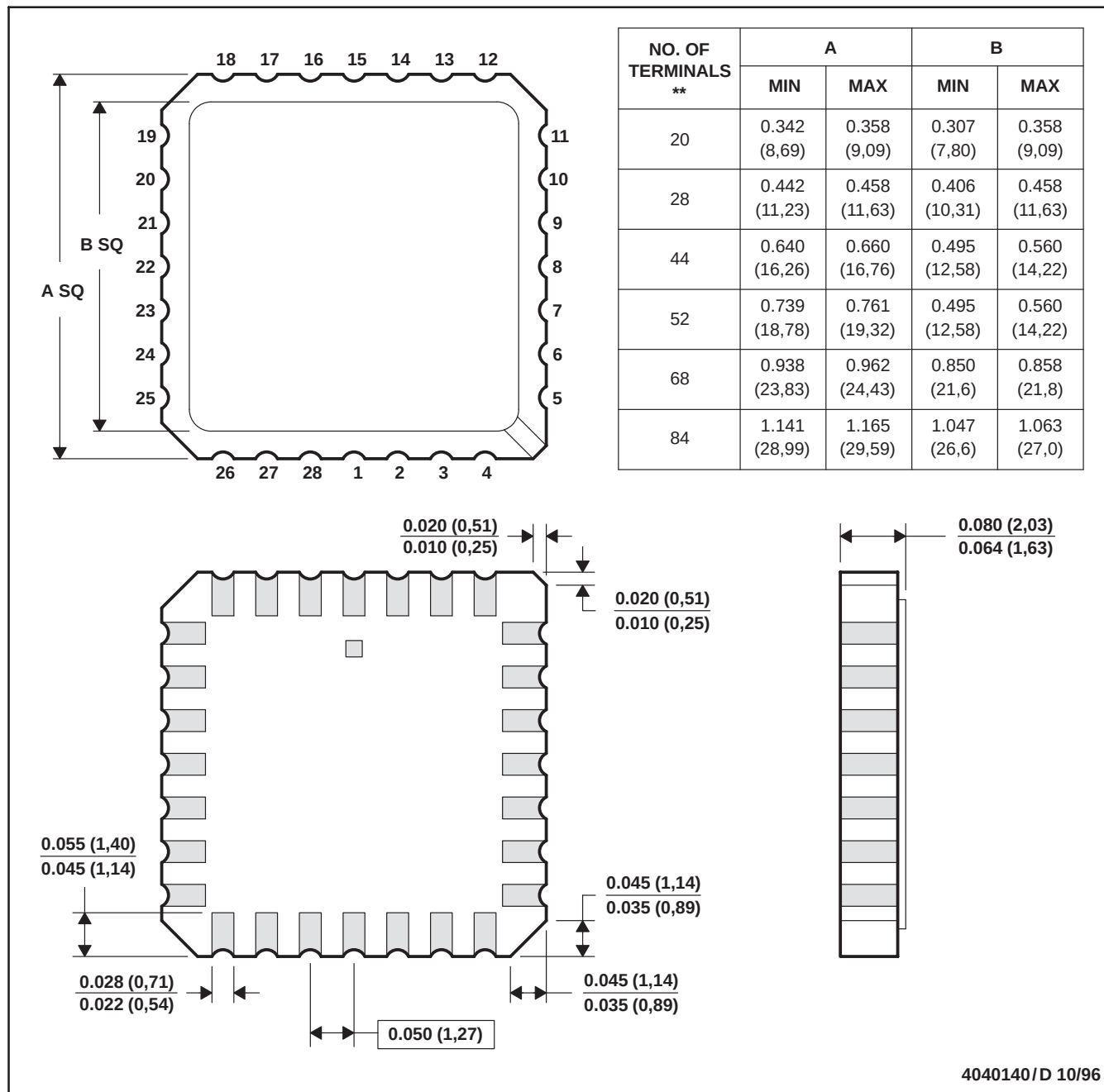


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

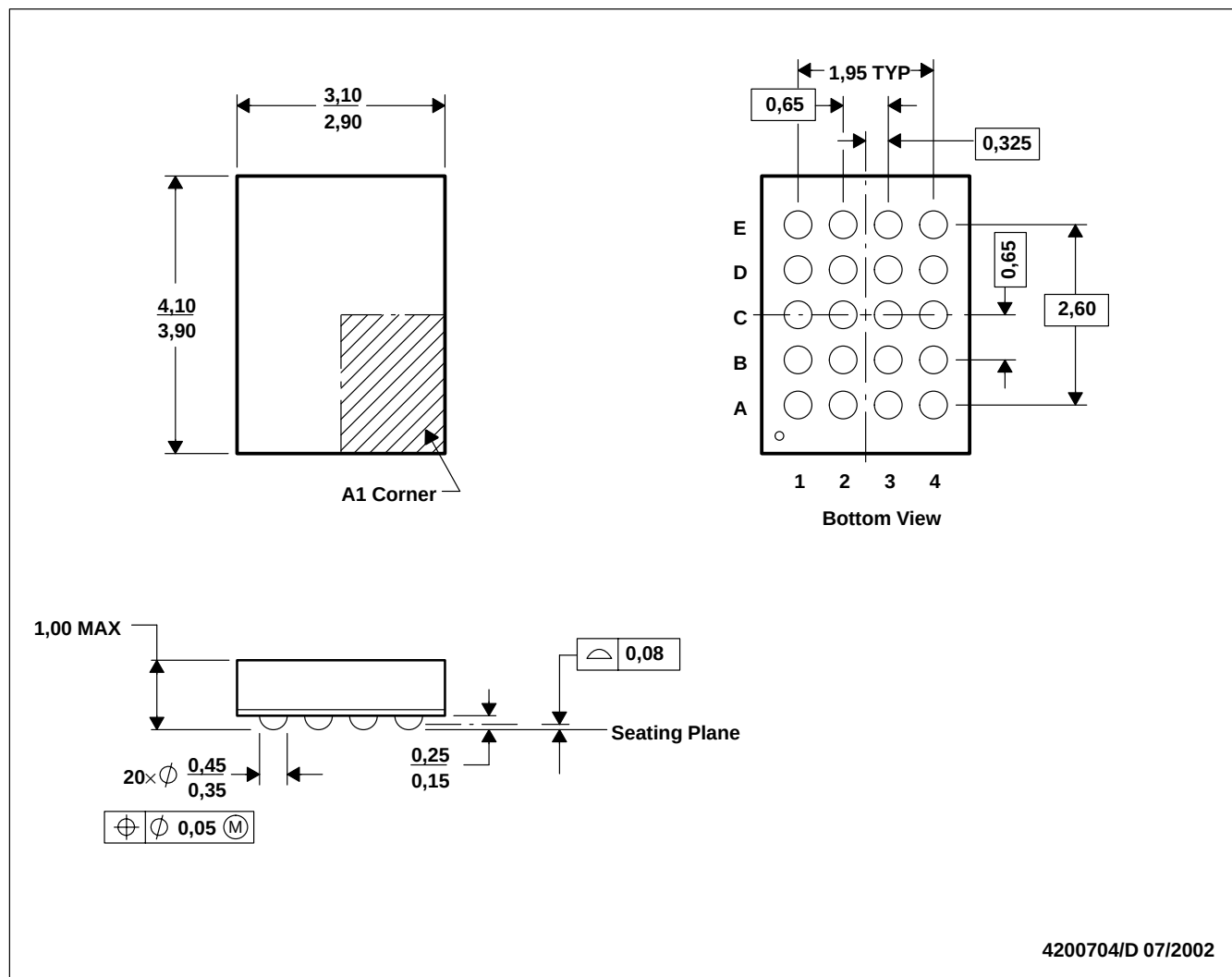
28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

GQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



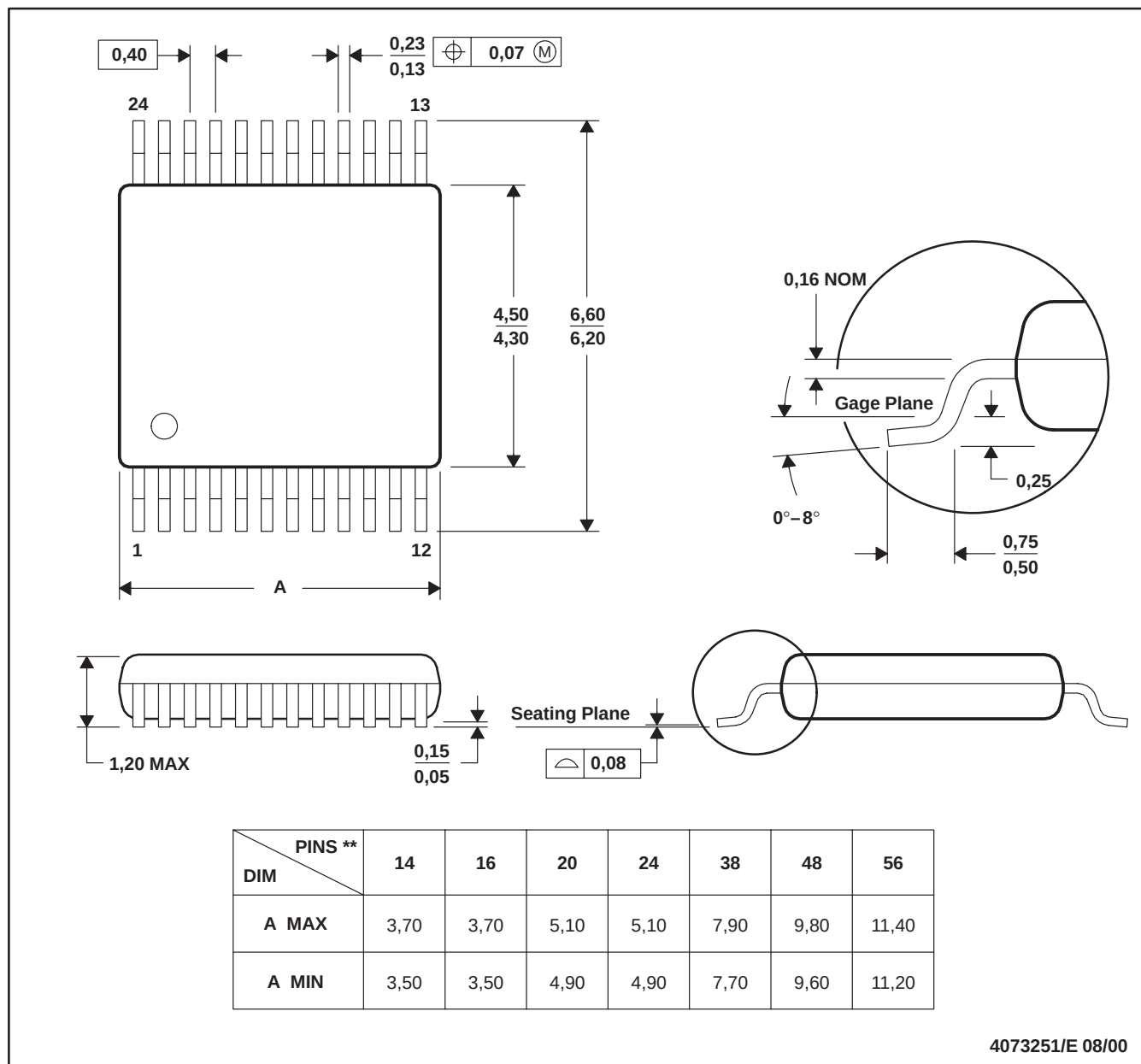
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. MicroStar Junior™ configuration
 D. Falls within JEDEC MO-225 variation BC.
 E. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

MicroStar Junior is a trademark of Texas Instruments.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

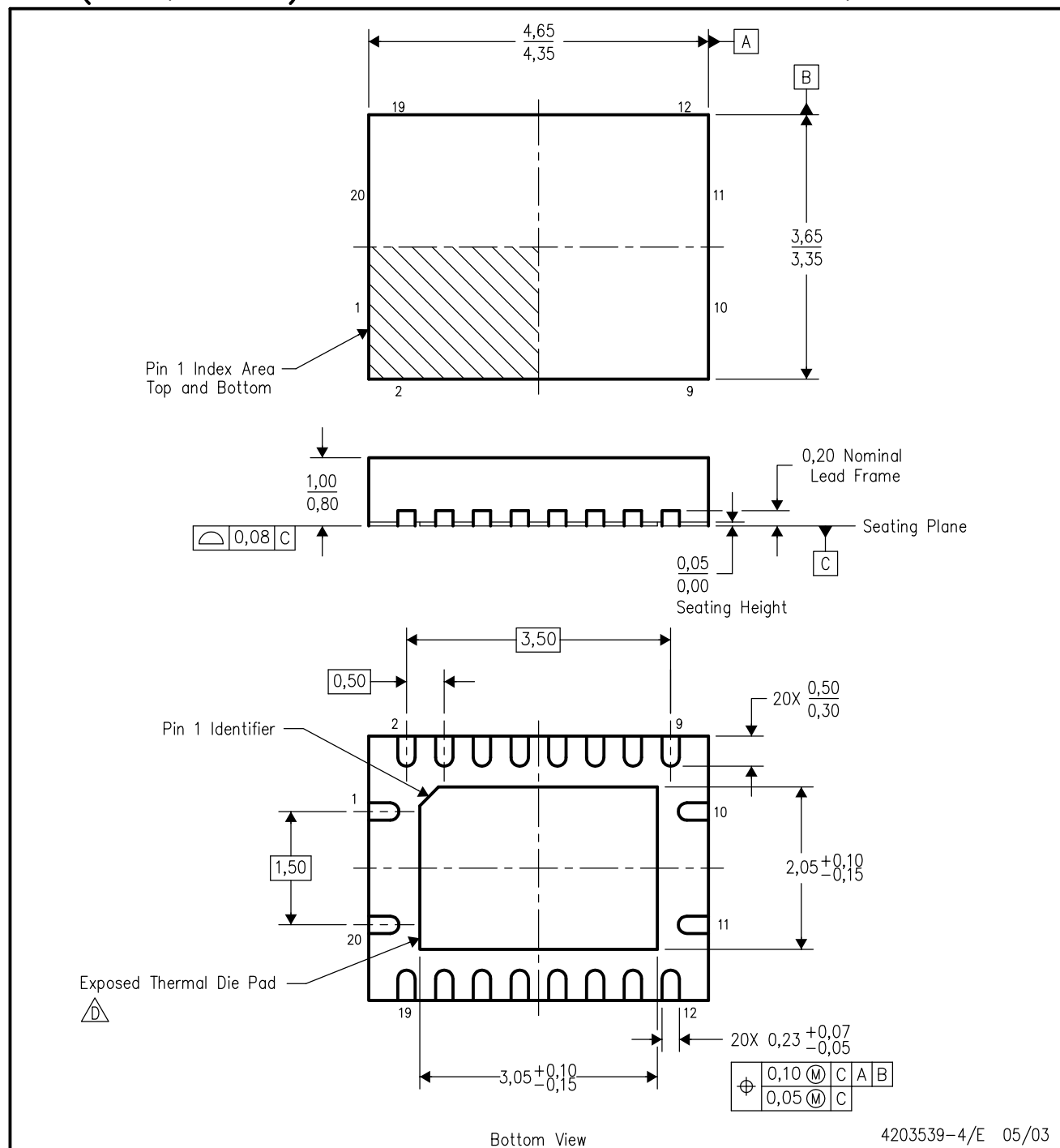
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

RGY (R-PQFP-N20)

PLASTIC QUAD FLATPACK

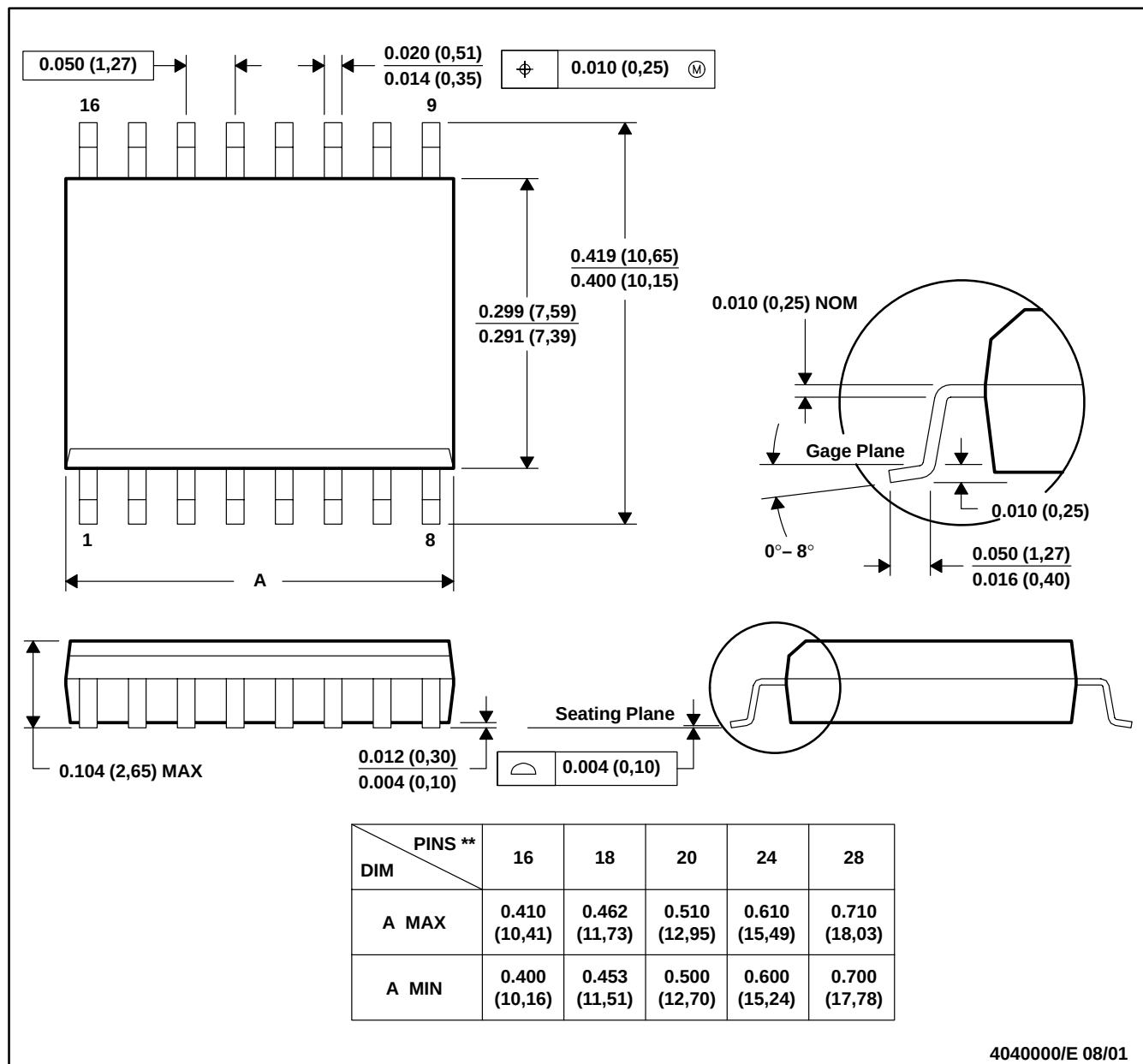


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
 - Package complies to JEDEC MO-241 variation BC.

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



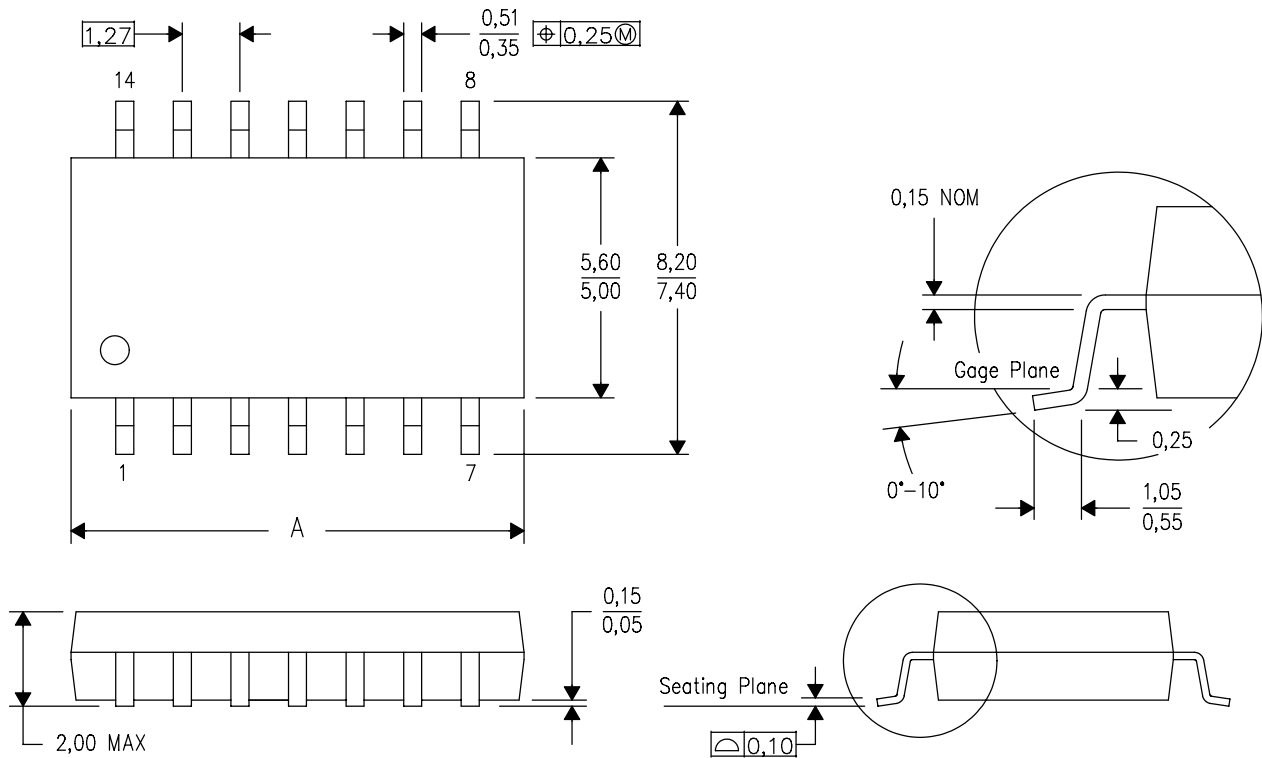
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

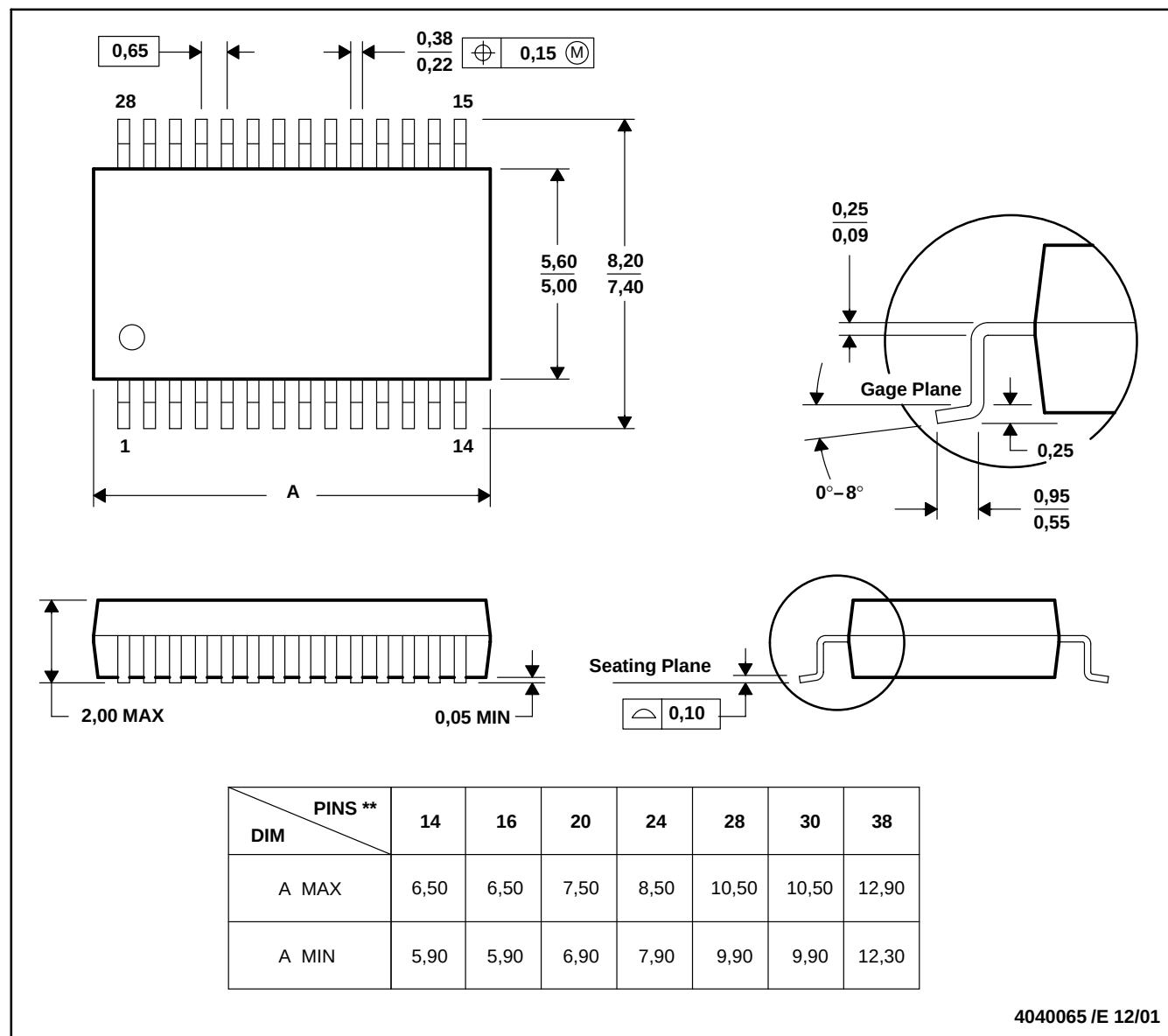
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

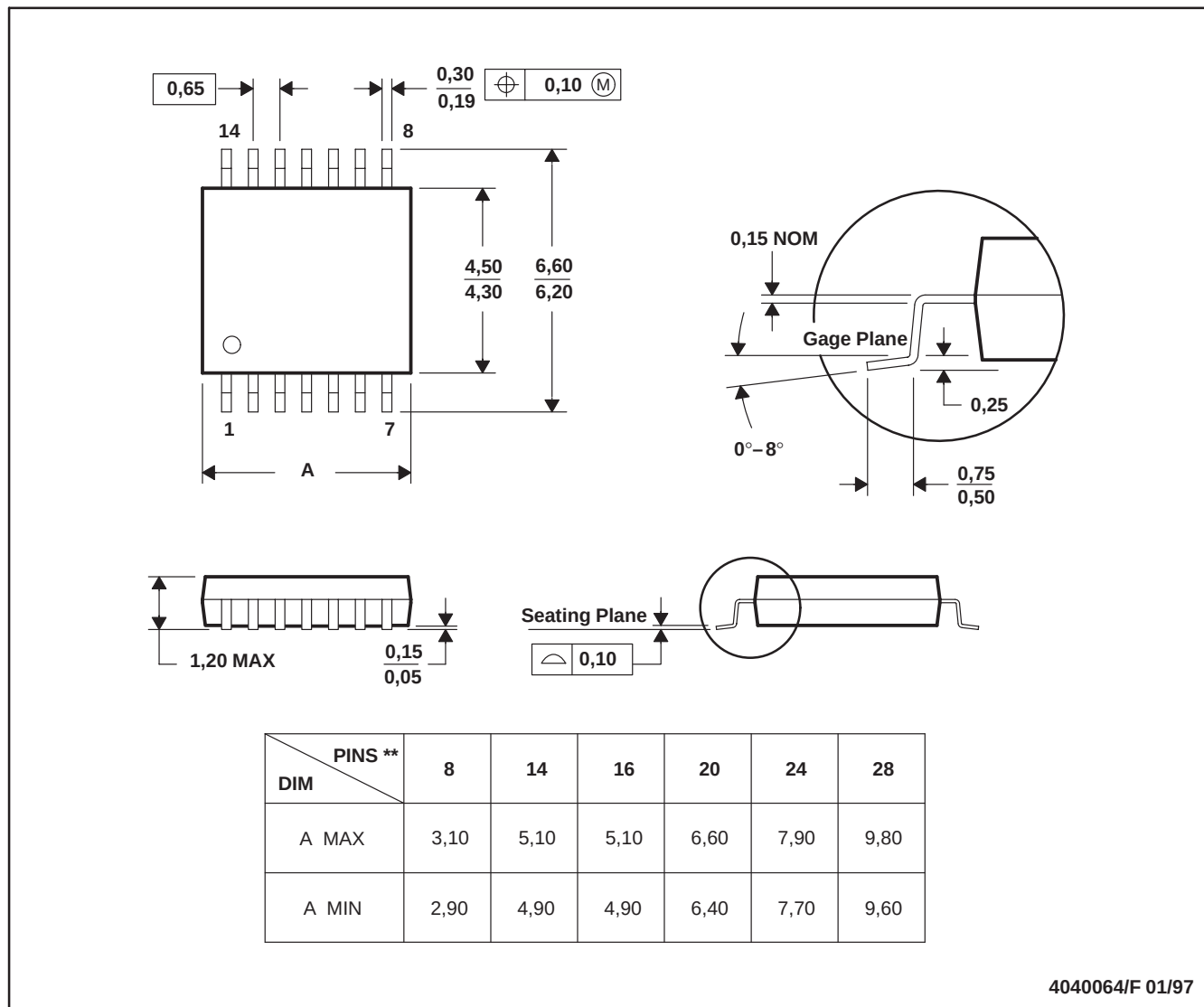


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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