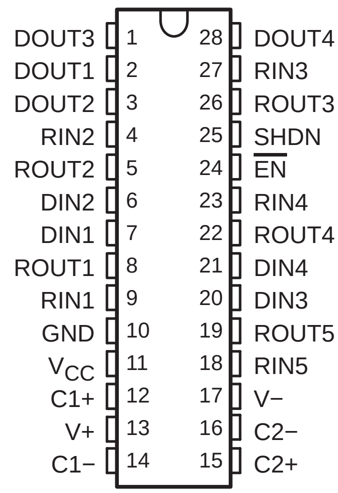
- **RS-232 Bus-Pin ESD Protection Exceeds ±15 kV Using Human-Body Model (HBM)**
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Operates at 5-V V_{CC} Supply**
- **Four Drivers and Five Receivers**
- **Operates Up To 120 kbit/s**
- **Low Supply Current in Shutdown Mode . . . 1 μA Typical**
- **External Capacitors . . . 4 × 0.1 μF**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **Applications**
  - **Battery-Powered Systems, PDAs, Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment**

DB OR DW PACKAGE
(TOP VIEW)



description/ordering information

The MAX211 device consists of four line drivers, five line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5-V supply. The devices operate at data signaling rates up to 120 kbit/s and a maximum of 30-V/μs driver output slew rate.

The MAX211 has both shutdown (SHDN) and enable control ($\overline{\text{EN}}$). In shutdown mode, the charge pumps are turned off, V+ is pulled down to V_{CC}, V− is pulled to GND, and the transmitter outputs are disabled. This reduces supply current typically to 1 μA. $\overline{\text{EN}}$ is used to put the receiver outputs into the high-impedance state to allow wired-OR connection of two RS-232 ports. It has no effect on the RS-232 drivers or the charge pumps.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC (DW)	Tube of 20	MAX211CDW	MAX211C
		Reel of 1000	MAX211CDWR	
	SSOP (DB)	Tube of 50	MAX211CDB	MAX211C
		Reel of 2000	MAX211CDBR	
−40°C to 85°C	SOIC (DW)	Tube of 20	MAX211IDW	MAX211I
		Reel of 1000	MAX211IDWR	
	SSOP (DB)	Tube of 50	MAX211IDB	MAX211I
		Reel of 2000	MAX211IDBR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

INPUTS		DRIVER	RECEIVER	DEVICE STATUS
SHDN	$\overline{EN}$			
L	L	All active	All active	Normal operation
L	H	All active	Z	Normal operation
H	X	Z	Z	Shutdown

X = don’t care, Z = high impedance

EACH DRIVER

INPUTS		OUTPUT DOUT	DRIVER STATUS
DIN	SHDN		
L	L	H	Normal operation
H	L	L	
X	H	Z	Powered off

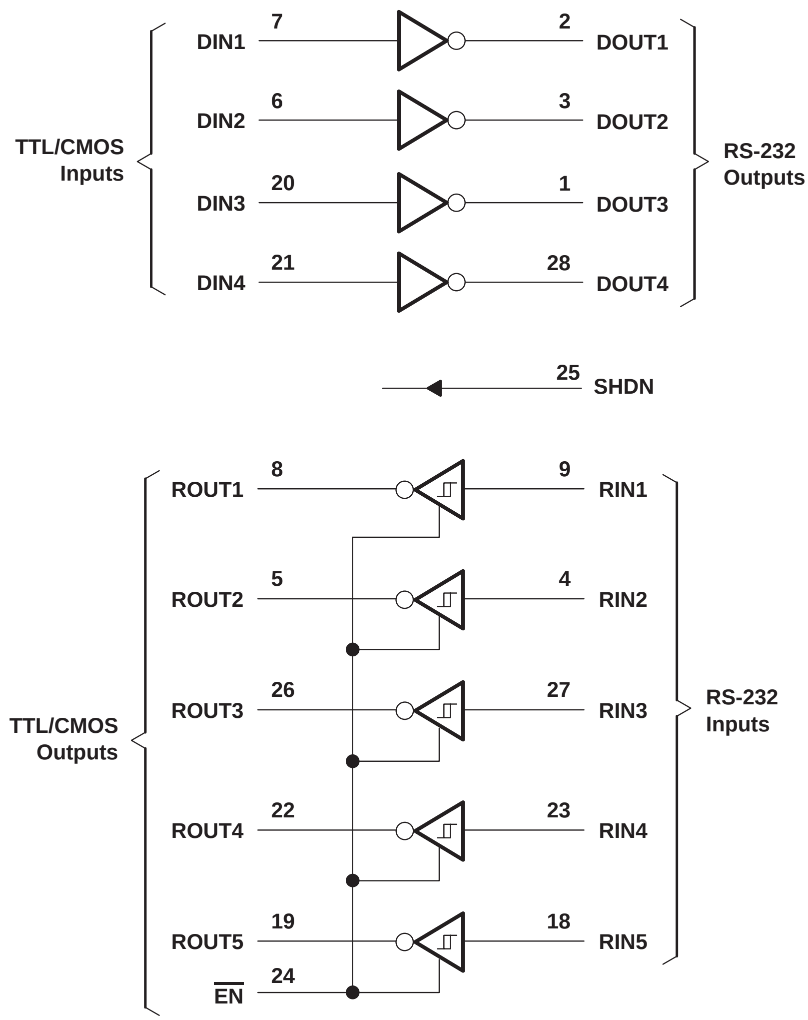
X = don’t care, Z = high impedance

EACH RECEIVER

INPUTS		OUTPUT ROUT	RECEIVER STATUS
RIN	$\overline{EN}$		
L	L	H	Normal operation
H	L	L	
X	H	Z	Powered off

X = don’t care, Z = high impedance

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 6 V
Positive charge pump voltage range, V+ (see Note 1) . . . . . V_{CC} − 0.3 V to 14 V
Negative charge pump voltage range, V− (see Note 1) . . . . . 0.3 V to −14 V
Input voltage range, V_I: Drivers . . . . . −0.3 V to V+ + 0.3 V
Receivers . . . . . ±30 V
Output voltage range, V_O: Drivers . . . . . V− − 0.3 V to V+ + 0.3 V
Receivers . . . . . −0.3 V to V_{CC} + 0.3 V
Short-circuit duration: DOUT . . . . . Continuous
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DB package . . . . . 62°C/W
DW package . . . . . 46°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4 and Figure 4)

			MIN	NOM	MAX	UNIT
	Supply voltage		4.5	5	5.5	V
V_{IH}	Driver high-level input voltage	DIN	2			V
	Control high-level input voltage	$\overline{EN}$, SHDN	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{EN}$, SHDN			0.8	V
V_I	Driver and control input voltage	DIN, $\overline{EN}$, SHDN	0		5.5	V
	Receiver input voltage		−30		30	
T_A	Operating free-air temperature	MAX211C	0		70	°C
		MAX211I	−40		85	

NOTE 4: Test conditions are C1−C4 = 0.1 μF at V_{CC} = 5 V ± 0.5 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
I_{CC}	Supply current	No load,	See Figure 6		14	20	mA
	Shutdown supply current	T_A = 25°C,	See Figure 1		1	10	μA

‡ All typical values are at V_{CC} = 5 V, and T_A = 25°C.
NOTE 4: Test conditions are C1−C4 = 0.1 μF at V_{CC} = 5 V ± 0.5 V.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND		5	9		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND		−5	−9		V
I_{IH}	Driver high-level input current	DIN = V_{CC}			15	200	μA
	Control high-level input current	$\overline{EN}$, SHDN = V_{CC}			3	10	
I_{IL}	Driver low-level input current	DIN = 0 V			−15	−200	μA
	Control low-level input current	$\overline{EN}$, SHDN = 0 V			−3	−10	
I_{OS}‡	Short-circuit output current	V_{CC} = 5.5 V,	V_O = 0 V		±10	±60	mA
r_o	Output resistance	V_{CC}, V+, and V− = 0 V,	V_O = ±2 V	300			Ω

† All typical values are at V_{CC} = 5 V, and T_A = 25°C.
‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.
NOTE 4: Test conditions are C1−C4 = 0.1 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
	Maximum data rate	C_L = 50 pF to 1000 pF, One DOUT switching,	R_L = 3 kΩ to 7 kΩ, See Figure 2	120			kbit/s
$t_{PLH (D)}$	Propagation delay time, low- to high-level output	C_L = 2500 pF, All drivers loaded,	R_L = 3 kΩ, See Figure 2		2		μs
$t_{PHL (D)}$	Propagation delay time, high- to low-level output	C_L = 2500 pF, All drivers loaded,	R_L = 3 kΩ, See Figure 2		2		μs
$t_{sk(p)}$	Pulse skew§	C_L = 150 pF to 2500 pF,	R_L = 3 kΩ to 7 kΩ, See Figure 3		300		ns
SR(tr)	Slew rate, transition region (see Figure 2)	C_L = 50 pF to 1000 pF, V_{CC} = 5 V	R_L = 3 kΩ to 7 kΩ,	3	6	30	V/μs

† All typical values are at V_{CC} = 5 V, and T_A = 25°C.
§ Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
NOTE 4: Test conditions are C1−C4 = 0.1 μF at V_{CC} = 5 V ± 0.5 V.

ESD protection

PIN	TEST CONDITIONS	TYP	UNIT
D_{OUT}, R_{IN}	Human-Body Model	±15	kV

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −1 mA		3.5	V_{CC}−0.4 V		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA				0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 5 V,	T_A = 25°C		1.7	2.4	V
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 5 V,	T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis ($V_{IT+} - V_{IT-}$)			0.2	0.5	1	V
r_i	Input resistance	V_{CC} = 5 V,	T_A = 25°C	3	5	7	kΩ
	Output leakage current	$\overline{EN}$ = V_{CC},	0 ≤ ROUT ≤ V_{CC}		±0.05	±10	μA

† All typical values are at V_{CC} = 5 V, and T_A = 25°C.
NOTE 4: Test conditions are C1−C4 = 0.1 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$t_{PLH\ (R)}$	Propagation delay time, low- to high-level output	C_L= 150 pF,	See Figure 4		0.5	10	μs
$t_{PHL\ (R)}$	Propagation delay time, high- to low-level output	C_L= 150 pF,	See Figure 4		0.5	10	μs
t_{en}	Output enable time	C_L= 150 pF, See Figure 5	R_L = 1 kΩ,		600		ns
t_{dis}	Output disable time	C_L= 150 pF, See Figure 5	R_L = 1 kΩ,		200		ns
$t_{sk(p)}$	Pulse skew‡	See Figure 3			300		ns

† All typical values are at V_{CC} = 5 V, and T_A = 25°C.
‡ Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
NOTE 4: Test conditions are C1−C4 = 0.1 μF, at V_{CC} = 5 V ± 0.5 V.

PARAMETER MEASUREMENT INFORMATION

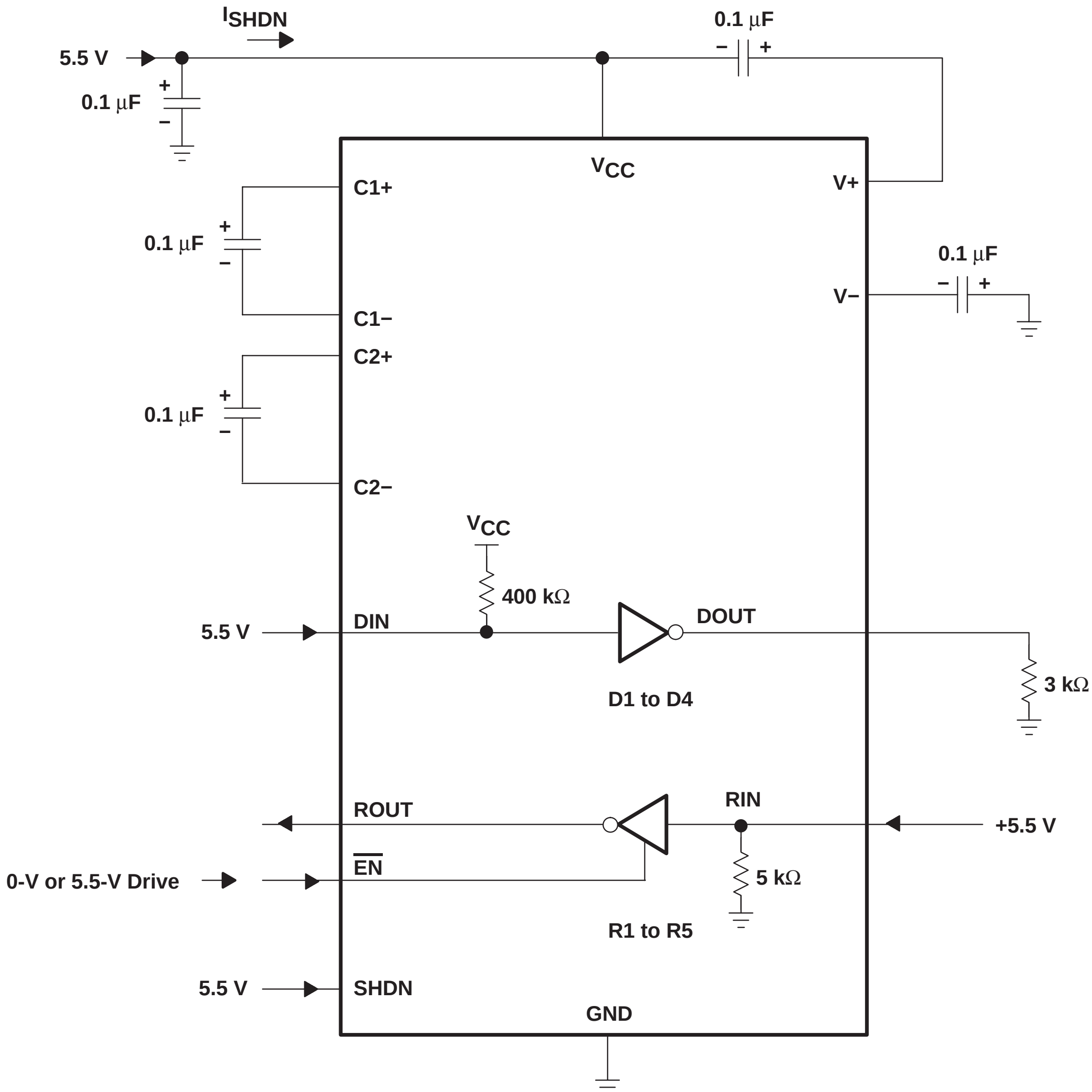
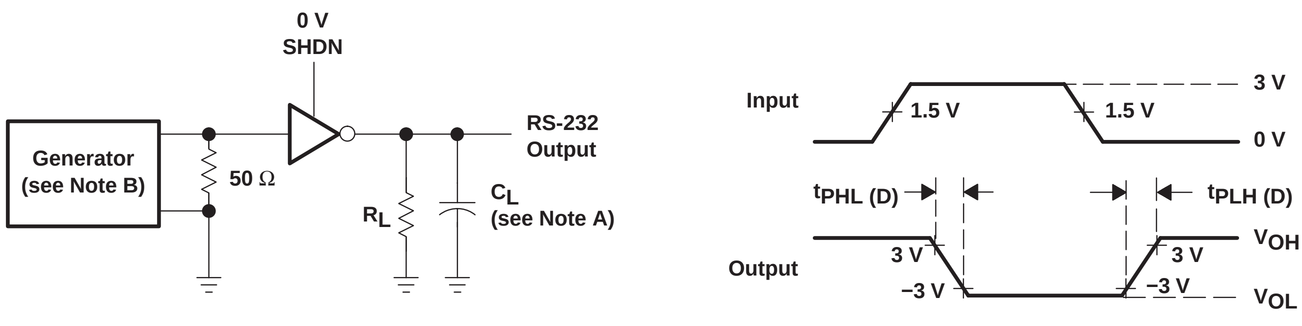


Figure 1. Shutdown Current Test Circuit

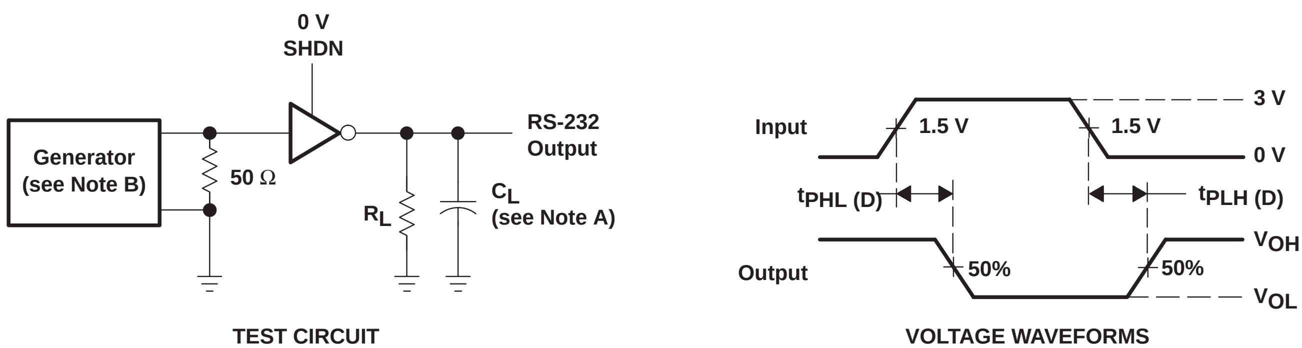
PARAMETER MEASUREMENT INFORMATION



$$SR(tr) = \frac{6\ V}{t_{PHL\ (D)}\ \text{or}\ t_{PLH\ (D)}}$$

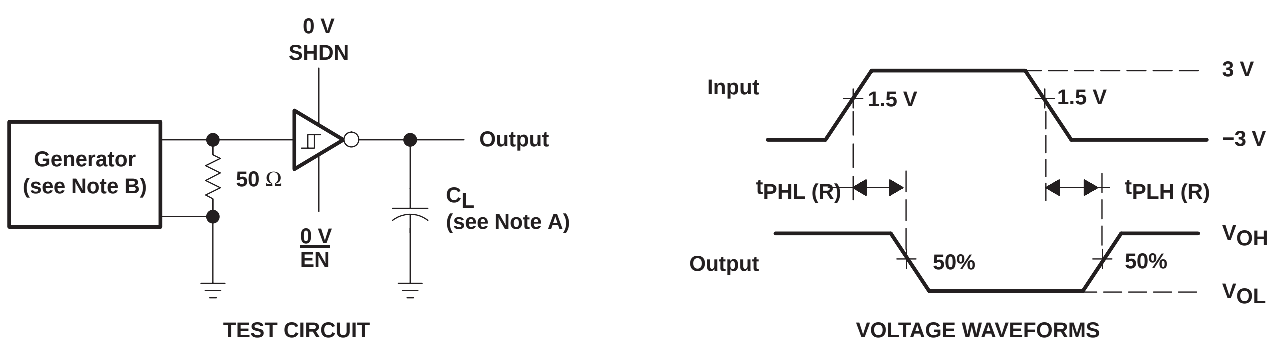
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 120 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 2. Driver Slew Rate and Propagation Delay Times



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 120 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

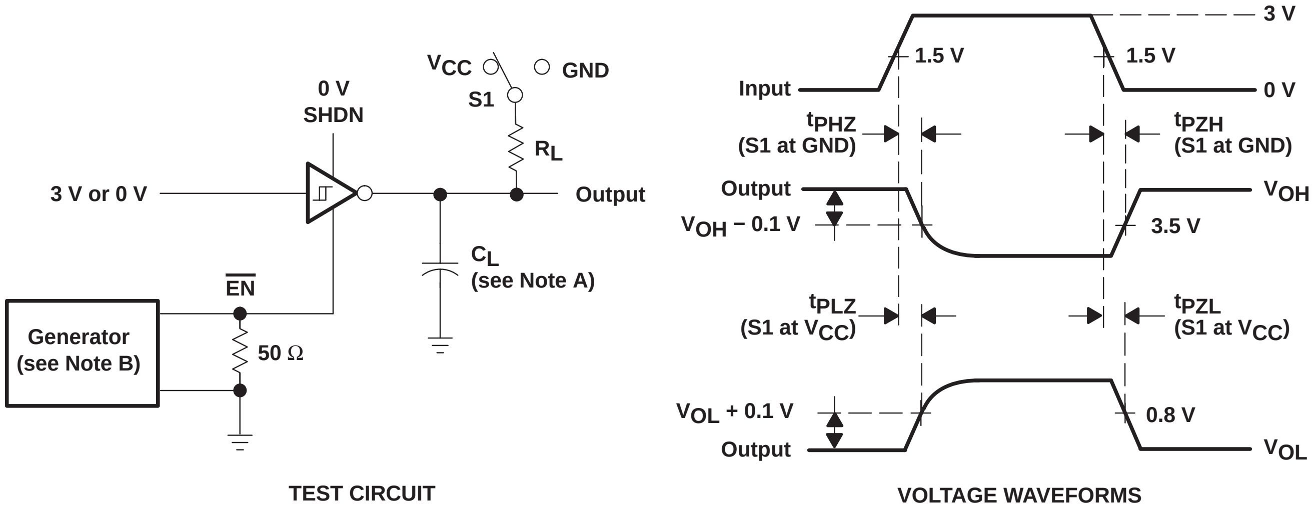
Figure 3. Driver Pulse Skew



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 4. Receiver Propagation Delay Times

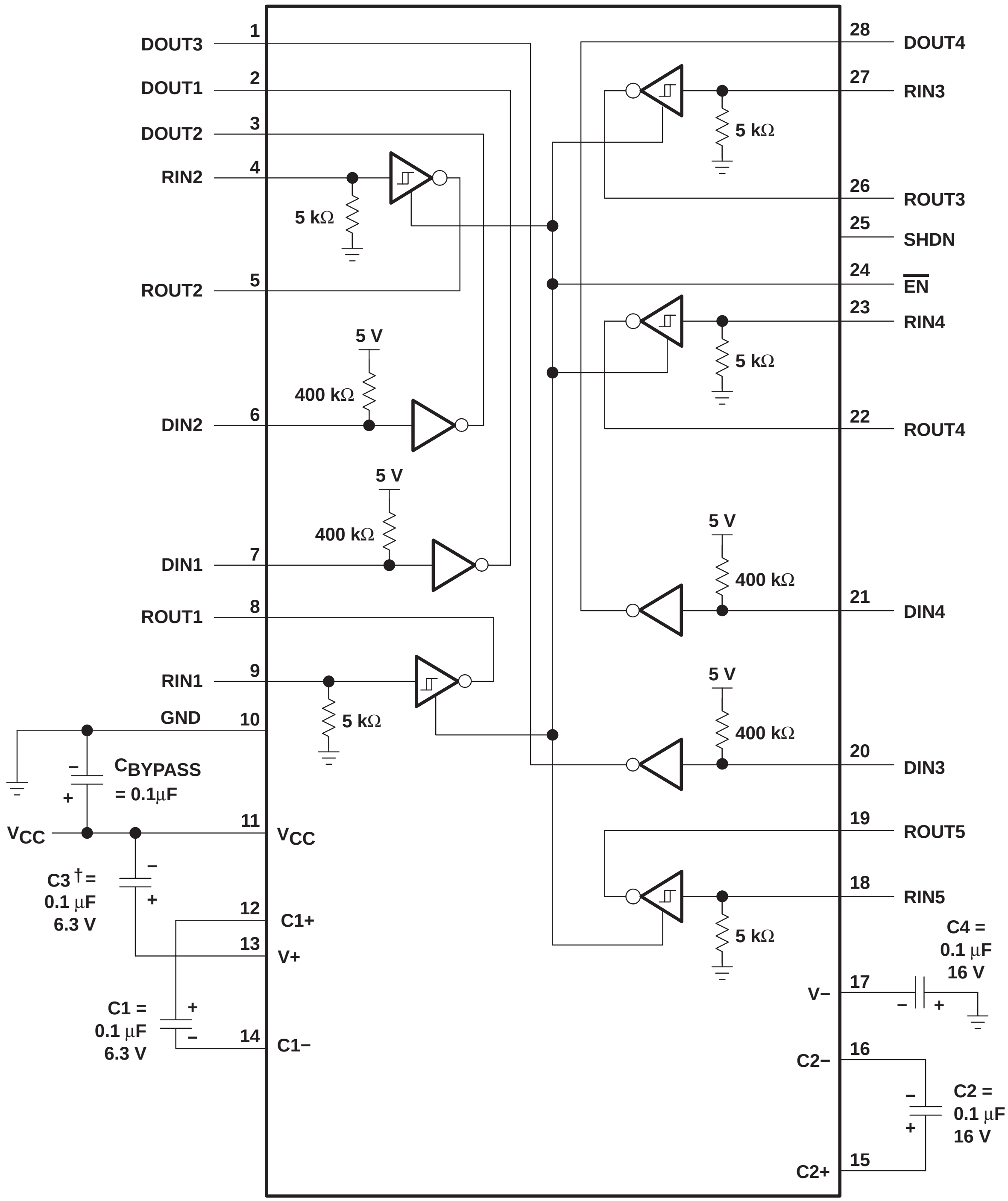
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
D. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 5. Receiver Enable and Disable Times

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 6. Typical Operating Circuit and Capacitor Values

APPLICATION INFORMATION

capacitor selection

The capacitor type used for C1−C4 is not critical for proper operation. The MAX211 requires 0.1-µF capacitors, although capacitors up to 10 µF can be used without harm. Ceramic dielectrics are suggested for the 0.1-µF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2×) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V−.

Use larger capacitors (up to 10 µF) to reduce the output impedance at V+ and V−.

Bypass V_{CC} to ground with at least 0.1 µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1−C4).

electrostatic discharge (ESD) protection

Texas Instruments MAX211 devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15 kV when powered down.

ESD test conditions

ESD testing is stringently performed by TI, based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

Human-Body Model

The Human-Body Model (HBM) of ESD testing is shown in Figure 7. Figure 8 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor charged to the ESD voltage of concern and subsequently discharged into the DUT through a 1.5-kΩ resistor.

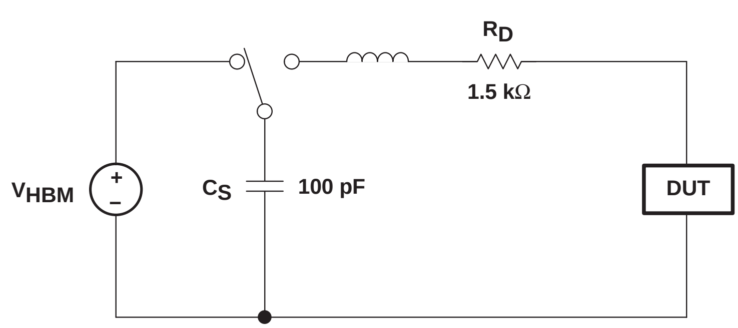


Figure 7. HBM ESD Test Circuit

APPLICATION INFORMATION

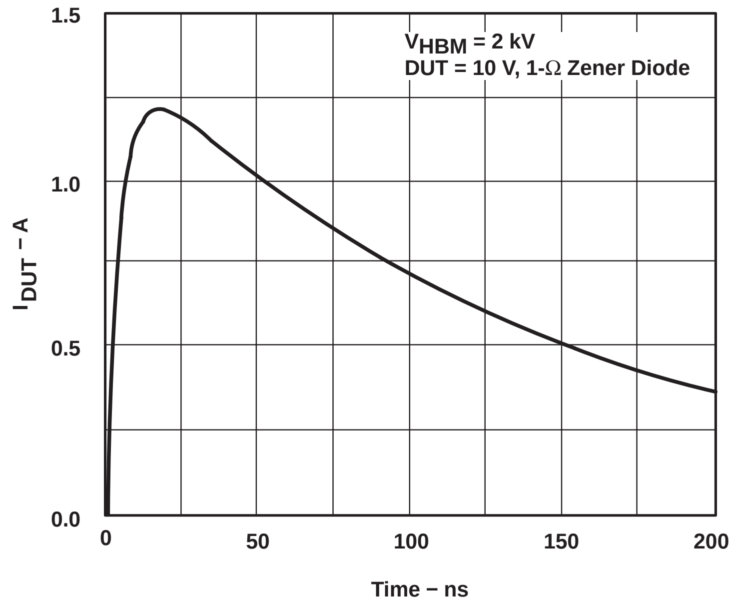


Figure 8. Typical HBM Current Waveform

Machine Model

The Machine Model (MM) ESD test applies to all pins, using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test no longer is as pertinent to the RS-232 pins.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
MAX211CDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211CDBE4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211CDBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211CDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211CDBRE4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211CDBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211CDW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211CDWE4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211CDWG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211CDWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211CDWRE4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211CDWRG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211IDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211IDBE4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211IDBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211IDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211IDBRE4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211IDBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211IDW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211IDWE4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211IDWG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211IDWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211IDWRE4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX211IDWRG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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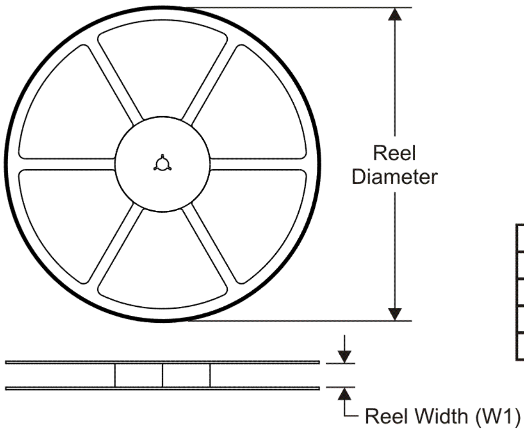
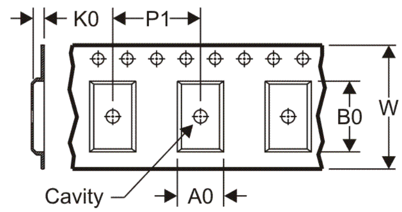
TAPE AND REEL INFORMATION

REEL DIMENSIONS

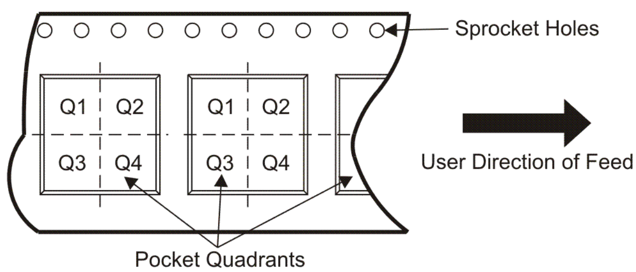


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

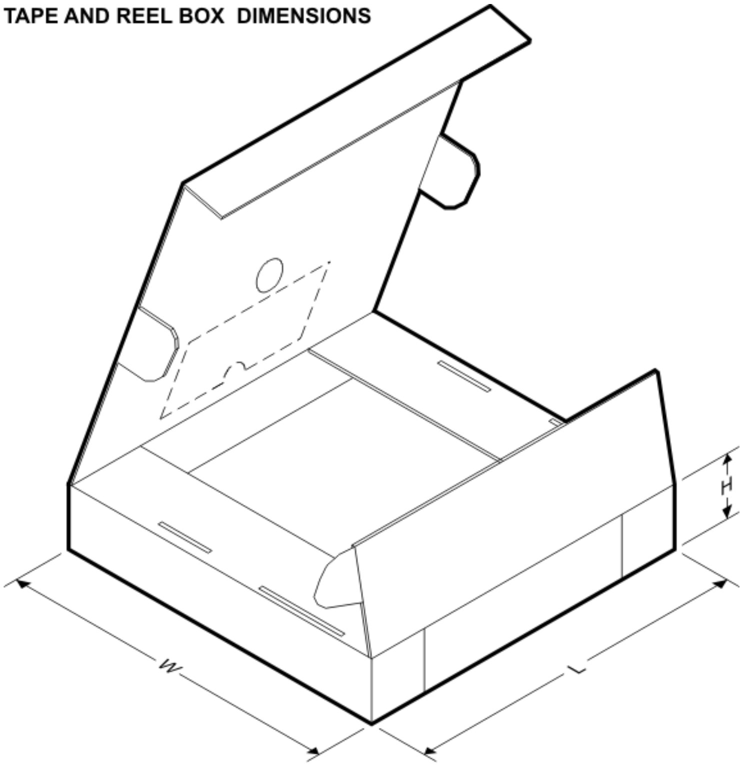
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX211CDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
MAX211CDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
MAX211IDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
MAX211IDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

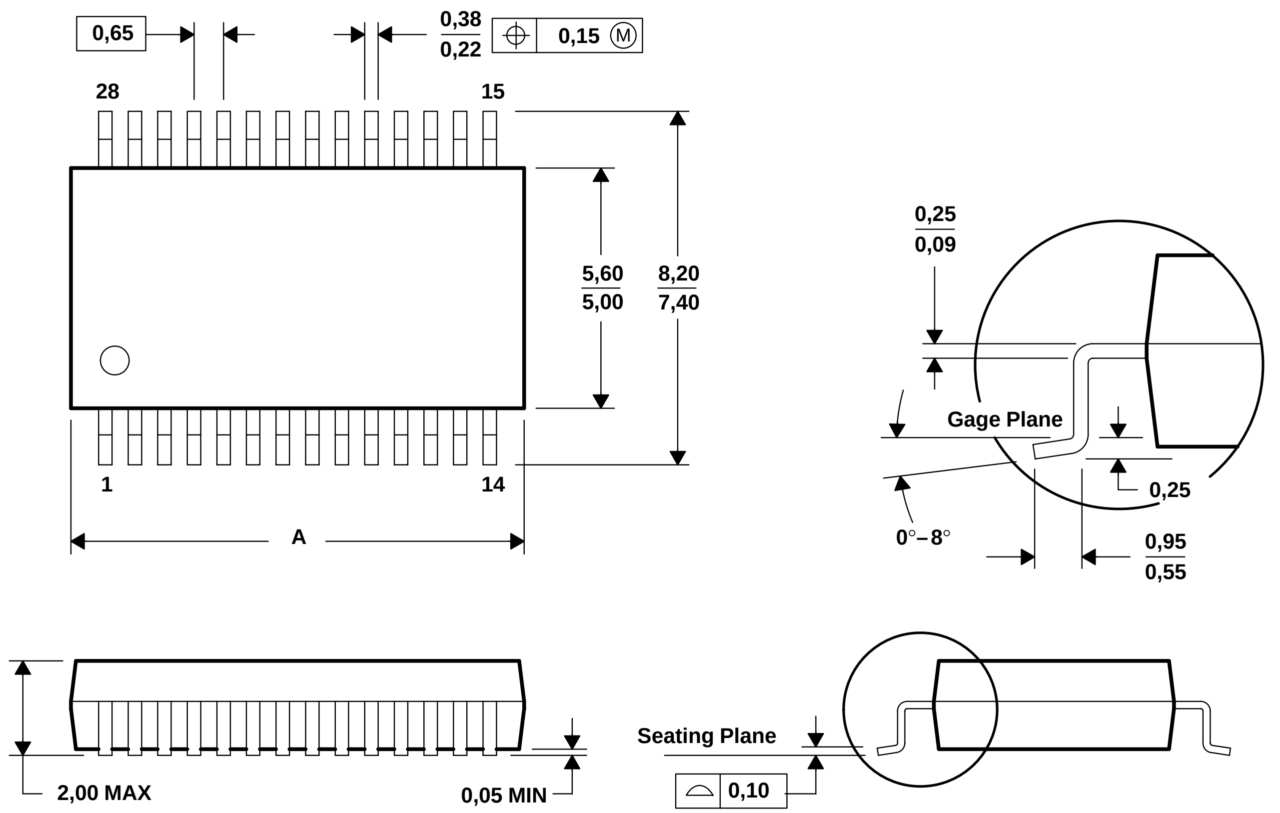


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX211CDBR	SSOP	DB	28	2000	346.0	346.0	33.0
MAX211CDWR	SOIC	DW	28	1000	346.0	346.0	49.0
MAX211IDBR	SSOP	DB	28	2000	346.0	346.0	33.0
MAX211IDWR	SOIC	DW	28	1000	346.0	346.0	49.0

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

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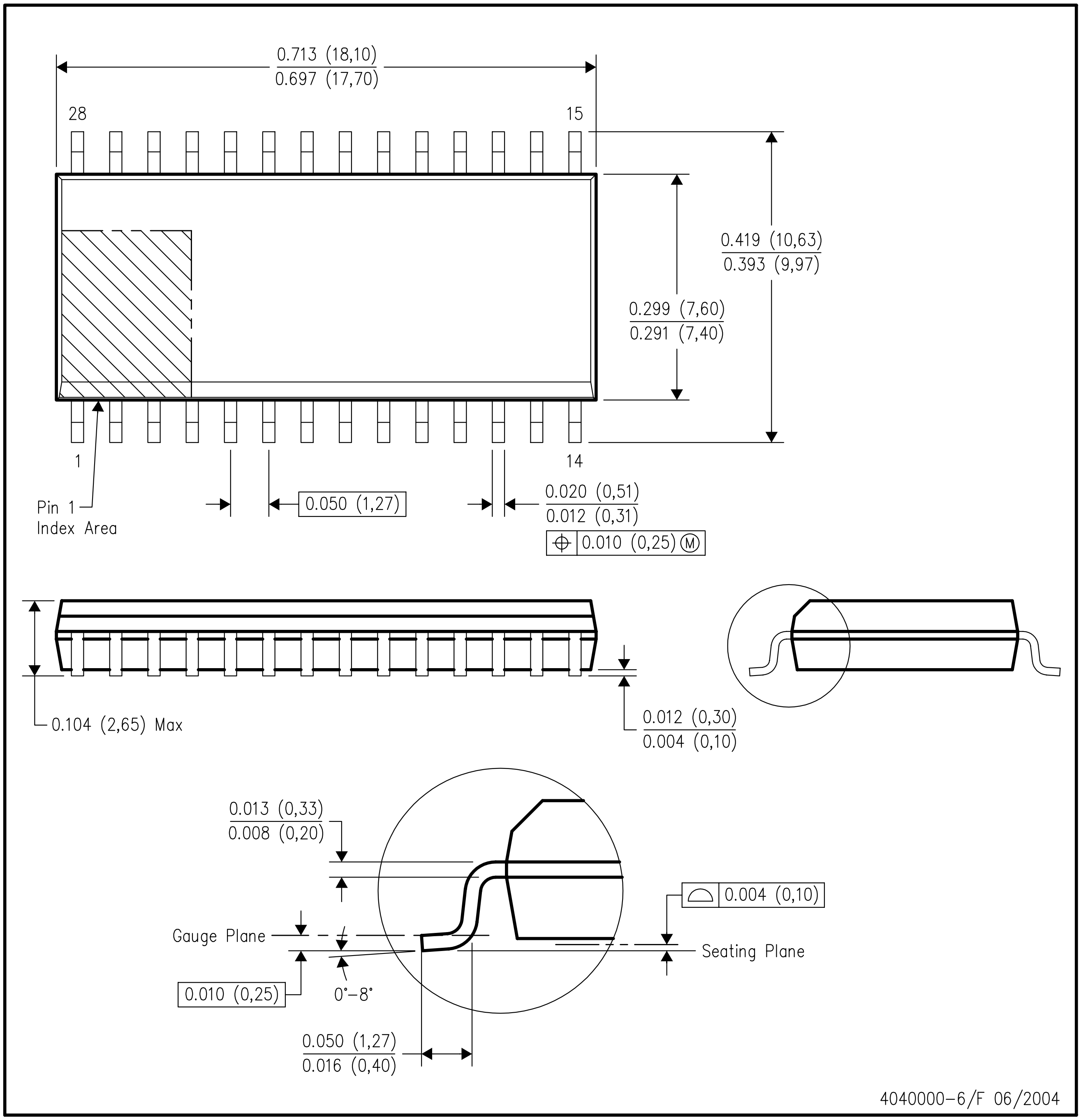
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

DW (R-PDSO-G28) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AE.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

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Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
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Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
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