REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																		
SHEET																		
REV																		
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28				

REV STATUS OF SHEETS	REV													
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Doug L. Gross

CHECKED BY
Ray Monnin

APPROVED BY

DRAWING APPROVAL DATE
92-08-31

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS
128K X 8 BIT FLASH EEPROM,
MONOLITHIC SILICON

SIZE	CAGE CODE	5962-90899
A	67268	

SHEET 1 OF 28

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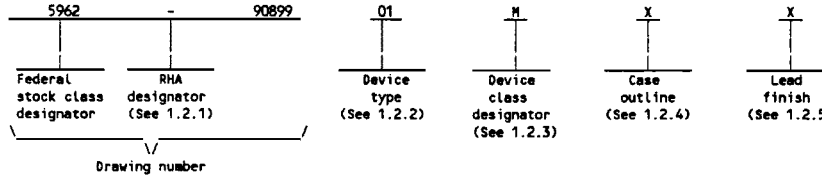
5962-E118

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V shall meet or exceed the electrical performance characteristics specified in table I herein after exposure to the specified irradiation levels specified in the absolute maximum ratings herein and the RHA marked devices shall be marked in accordance with MIL-I-38535. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time	Endurance
01	28F010	(128 K x 8) CMOS flash EEPROM	250 ns	10000 cycles
02	28F010	(128 K x 8) CMOS flash EEPROM	200 ns	10000 cycles
03	28F010	(128 K x 8) CMOS flash EEPROM	150 ns	10000 cycles
04	28F010	(128 K x 8) CMOS flash EEPROM	120 ns	10000 cycles
05	28F010	(128 K x 8) CMOS flash EEPROM	250 ns	1000 cycles
06	28F010	(128 K x 8) CMOS flash EEPROM	200 ns	1000 cycles
07	28F010	(128 K x 8) CMOS flash EEPROM	150 ns	1000 cycles
08	28F010	(128 K x 8) CMOS flash EEPROM	120 ns	1000 cycles

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
T	See figure 1	32	"J" lead chip carrier
U	See figure 1	32	Flat pack
X	GDIP1-T32 or CDIP2-T32	32	Dual-in-line
Y	CQCC1-N32	32	Rectangular leadless chip carrier
Z	See figure 1	32	Gullwing lead chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Endurance:	
Device types 01-04	10000 cycles/byte, minimum
Device types 05-08	1000 cycles/byte, minimum
Supply voltage range (V_{CC}) 2/	-2.0 V dc to +7.0 V dc
Storage temperature range (T_{stg})	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J) 3/	+150°C
Thermal resistance, junction-to-case (Θ_{JC}) (case outline X, Y)	See MIL-STD-1835
Thermal resistance, junction-to-case (Θ_{JC}) (case outlines T, Z)	13°C/W
Thermal resistance, junction-to-case (Θ_{JC}) (case outline U)	27°C/W
Voltage on any pin with respect to ground 2/	-2.0 V dc to +7.0 V dc
Voltage on pin A9 with respect to ground 4/	-2.0 V dc to +13.5 V dc
V_{pp} supply voltage with respect to ground 4/	-2.0 V dc to +14.0 V dc
V_{CC} supply voltage with respect to ground 2/	-2.0 V dc to +7.0 V dc
Output short circuit current 5/	200 mA
Data retention	10 years minimum

1.4 Recommended operating conditions. 6/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Operating temperature range (T_{case})	-55°C to +125°C
Low level input voltage range (V_{IL})	-0.5 V dc to +0.8 V dc
High level input voltage range (V_{IH})	+2.0 V dc to V_{CC} +0.5 V dc
High level input voltage range, CMOS (V_{IH})	V_{CC} -0.5 V dc to V_{CC} +0.5 V dc
Chip clear (V_P)	11.4 V dc to 12.6 V dc

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	xx percent 7/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Minimum dc voltage on input or V_O pins is -0.5 V. During voltage transitions, inputs may overshoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum dc voltage on output and V_O pins is V_{CC} +0.5 V. During voltage transitions outputs may overshoot to V_{CC} +2.0 V for periods up to 20 ns.
3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
4/ Minimum dc input voltage on A9 or V_{pp} may overshoot to +14.0 V for periods less than 20 ns.
5/ No more than one output shorted at a time. Duration of short circuit should not be greater than 1 second.
6/ All voltages are referenced to V_{SS} (ground).
7/ When QML source exists a value shall be provided.

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of LATCH-UP in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronic Industries Association, 2001 Pennsylvania Avenue, N.W., Washington, DC 20006.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pennsylvania 19103).

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth tables. The truth tables shall be as specified on figure 3.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 3 herein. When required, in screening (see 4.2 herein), or quality conformance inspection groups A, B, C, or D (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test in a checkerboard or similar pattern (a minimum of 50 percent of the total number of bits programmed).

3.2.3.2 Programmed devices. The requirements for supplying programmed devices are not part of this document.

3.2.3.3 Command definitions. The command definitions table shall be as specified on figure 3.

3.2.4 Block diagram. The block diagram shall be as specified on figure 4.

3.2.5 Switching test circuits and waveforms. The switching test circuits and waveforms shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECS of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Device type	Limits		Units
					Min	Max	
DC CHARACTERISTICS							
Input leakage current	I_{LI}	$V_{CC} = V_{CC}$ max, $V_{IN} = V_{CC}$ max or V_{SS}	1, 2, 3	All		±1.0	µA
Output leakage current	I_{LO}	$V_{CC} = V_{CC}$ max, $V_{OUT} = V_{CC}$ max or V_{SS}	1, 2, 3	All		±10	µA
V_{CC} standby current (TTL)	I_{CCS1}	$V_{CC} = V_{CC}$ max, $\overline{CE} = V_{IH}$	1, 2, 3	All		1.0	mA
V_{CC} standby current (CMOS)	I_{CCS2}	$V_{CC} = V_{CC}$ max, $\overline{CE} = V_{CC}$ ±0.2 V	1, 2, 3	All		100	µA
V_{CC} active read current	I_{CC1}	$V_{CC} = V_{CC}$ max, $\overline{CE} = V_{IL}$, $I_{OUT} = 0$ mA, f = 6.0 MHz, $\overline{OE} = V_{IH}$	1, 2, 3	All		30	mA
V_{CC} programming current	I_{CC2}	$\overline{CE} = V_{IL}$, programming in progress	1, 2, 3	All		30 2/	mA
V_{CC} erase current	I_{CC3}	$\overline{CE} = V_{IL}$, erasure in progress	1, 2, 3	All		30 2/	mA
V_{PP} standby current	I_{PPS}	$V_{PP} = V_{PPL}$	1, 2, 3	All		±10	µA
V_{PP} read current	I_{PP1}	$V_{PP} = V_{PPH}$	1, 2, 3	All		200	µA
		$V_{PP} = V_{PPL}$				±10	
V_{PP} programming current	I_{PP2}	$V_{PP} = V_{PPH}$, programming in progress	1, 2, 3	All		30 2/	mA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Device type	Limits		Units
					Min	Max	
DC CHARACTERISTICS - Continued							
V_{PP} erase current	I_{PP3}	$V_{PP} = V_{PPH}$ erasure in progress	1, 2, 3	All		30 2/	mA
Low level input voltage	V_{IL}		1, 2, 3	All	-0.5 2/	0.8	V
High level input voltage (TTL)	V_{IH1}		1, 2, 3	All	2.0	V_{CC}+ 0.5 2/	V
High level input voltage (CMOS)	V_{IH2}		1, 2, 3	All	0.7 V_{CC}	V_{CC}+ 0.5 2/	V
Low level output voltage	V_{OL}	$I_{OL} = 2.1$ mA, $V_{CC} = V_{CC}$ min	1, 2, 3	All		0.45	V
High level output voltage (TTL)	V_{OH1}	$I_{OH} = -2.5$ mA, $V_{CC} = V_{CC}$ min	1, 2, 3	All	2.4		V
High level output voltage (CMOS)	V_{OH2}	$I_{OH} = -2.5$ mA, $V_{CC} = V_{CC}$ min	1, 2, 3	All	0.85 V_{CC}		V
	V_{OH3}	$I_{OH} = -100\ \mu A$, $V_{CC} = V_{CC}$ min			V_{CC}- 0.4 2/		V
A9 auto select voltage	V_{ID}	A9 = V_{ID}	1, 2, 3	All	11.5	13.0	V
A9 auto select current	I_{ID}	A9 = V_{ID} max, $V_{CC} = V_{CC}$ max	1, 2, 3	All		500 2/	µA
V_{PP} during read only operations	V_{PPL}	NOTE: erase/program are inhibited when $V_{PP} = V_{PPL}$	1, 2, 3	All	0	V_{CC}+ 2.0 2/	V
V_{PP} during read/write operations	V_{PPH}		1, 2, 3	All	11.4	12.6	V
Functional tests		See 4.4.1d	7, 8A, 8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Device type	Limits		Units
					Min	Max	
CAPACITANCE 2/							
Input capacitance	C_{IN1}	$V_{IN} = 0\ V$, $T_A = 25°C$, $f = 1.0\ MHz$	4	All		10	pF
Output capacitance	C_{OUT}	$V_{OUT} = 0\ V$, $T_A = 25°C$, $f = 1.0\ MHz$	4	All		12	pF
V_{pp} input capacitance	C_{IN2}	$V_{IN} = 0\ V$, $T_A = 25°C$, $f = 1.0\ MHz$	4	All		12	pF
AC CHARACTERISTICS - READ ONLY OPERATIONS (See figure 5 as applicable.)							
Read cycle time	t_{AVAV1} (t_{RC})	2/	9, 10, 11	01,05 02,06 03,07 04,08	250 200 150 120		ns
Chip enable access time	t_{ELQV} (t_{CE})		9, 10, 11	01,05 02,06 03,07 04,08		250 200 150 120	ns
Address access time	t_{AVQV} (t_{ACC})		9, 10, 11	01,05 02,06 03,07 04,08		250 200 150 120	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Device type	Limits		Units
					Min	Max	
AC CHARACTERISTICS - READ ONLY OPERATIONS - Continued. (See figure 5 as applicable.)							
Output enable access time	t_{GLQV} (t_{OE})		9, 10, 11	01,05 02,06 03,07 04,08		65 60 55 50	ns
Chip enable to output in low Z	t_{ELQX} (t_{LZ})		9, 10, 11	All	0 2/		ns
Chip disable to output in high Z	t_{EHQZ} (t_{DF1})	2/	9, 10, 11	All		55	ns
Output enable to output in low Z	t_{GLQX} (t_{OLZ})		9, 10, 11	All	0 2/		ns
Output disable to output in high Z	t_{GHQZ} (t_{DF2})	2/	9, 10, 11	01,05 02,06 03,07 04,08		60 45 35 30	ns
Output hold from address, CE, or OE change	t_{AXQX} (t_{OH})	3/	9, 10, 11	All	0 2/		ns
Write recovery time before read	t_{WHGL}		9, 10, 11	All	6.0		µs
ERASE AND PROGRAMMING PERFORMANCE							
Chip erase		Excludes 00H programming	9, 10, 11	All		60	s
Chip program		Excludes system overhead 4/		All		24	s

1/ Case temperatures are instant on.
2/ Parameters shall be tested as part of device initial characterization and after design and process change. Parameter shall be guaranteed to the limits specified in table I for all lots not specifically tested.
3/ Whichever occurs first.
4/ Minimum byte programming time excluding system overhead is 16 µs (10 µs programming +6.0 µs write recovery), while maximum is 400 µs/byte (16 µs x 25 loops allowed by algorithm). Maximum chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 42 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

3.12 Processing of EEPROMs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

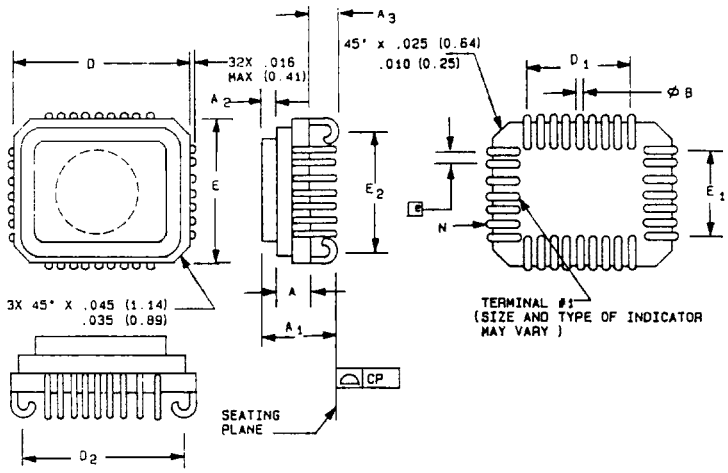
3.12.1 Conditions of the supplied devices. Devices will be supplied in an unprogrammed or clear state. No provision will be made for supplying programmed devices.

3.12.2 Erasure of EEPROMs. When specified, devices shall be erased in accordance with procedures and characteristics specified in 4.5.1.

3.12.3 Programming of EEPROMs. When specified, devices shall be programmed in accordance with procedures and characteristics specified in 4.5.2.

3.12.4 Verification of state of EEPROMs. When specified, devices shall be verified as either written to the specified pattern or cleared. As a minimum, verification shall consist of performing a read of the entire array to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and the device shall be removed from the lot or sample.

Case T



NOTE: Metric equivalents are given in parenthesis.

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.057	.080	1.45	2.03	
A_1	.122	.159	3.10	4.04	Solid lid
A_2	.010	.014	0.25	0.36	Solid lid
A_3	.055	.065	1.38	1.65	
ϕB	.014	.018	0.36	0.46	
CP	.000	.004	0.00	0.10	
D	.540	.565	13.72	14.35	
D_1	.400		10.16		Reference
D_2	.500		12.70		
E	.440	.464	11.17	11.79	
E_1	.300		7.62		Reference
E_2	.400		10.16		
e	.043	.057	1.09	1.45	Typical
N	32				

FIGURE 1. Case outlines.

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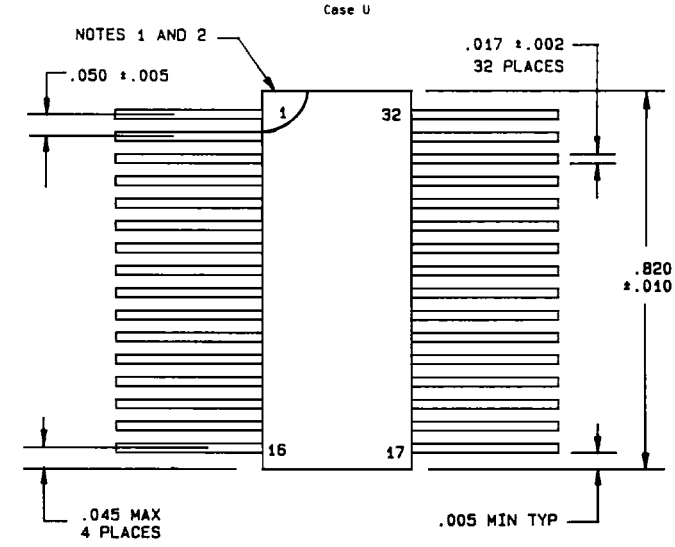
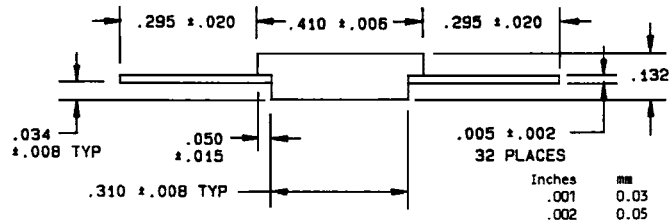
Case U





Inches	mm	Inches	mm
.001	0.03	.040	1.02
.002	0.05	.045	1.15
.005	0.13	.050	1.27
.006	0.15	.132	3.35
.008	0.20	.295	7.49
.017	0.43	.310	7.87
.020	0.51	.410	10.41
.034	0.86	.820	20.83

NOTES:
1. Terminal one shall be identified by a mechanical index on the lead or body, or a mark on the top surface within the region shown.
2. Terminal identification numbers need not appear on the package.
3. Weight: 1.5 g maximum.
4. Dimensions are in inches.
5. Metric equivalents are given for general information only.

FIGURE 1. Case outlines - Continued.

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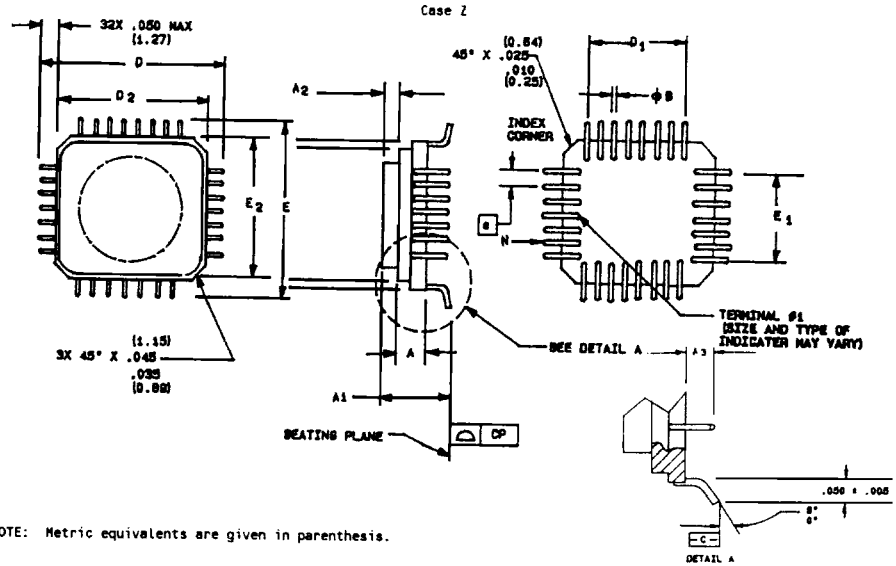

NOTE: Metric equivalents are given in parenthesis.

Family: Ceramic leadless chip carrier					
Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.057	.080	1.45	2.03	
A_1	.122	.159	3.10	4.04	Solid lid
A_2	.010	.014	0.25	0.36	Solid lid
A_3	.055	.065	1.40	1.65	
B	.014	.018	0.36	0.46	
CP	.000	.004	0.00	0.10	
D		.670		17.01	
D_1	.400		10.16		Reference
D_2	.540	.560	13.71	14.22	
E		.570		14.49	
E_1	.300		7.62		Reference
E_2	.440	.460	11.18	11.68	
$\lvert e \rvert$	.043	.057	1.09	1.45	Typical
N	32				

FIGURE 1. Case outlines - Continued.

Device types	All
Case outlines	T, U, X, Y, Z
Terminal number	Terminal symbol
1	V_{PP}
2	A16
3	A15
4	A12
5	A7
6	A6
7	A5
8	A4
9	A3
10	A2
11	A1
12	A0
13	DQ0
14	DQ1
15	DQ2
16	V_{SS}
17	DQ3
18	DQ4
19	DQ5
20	DQ6
21	DQ7
22	$\overline{CE}$
23	A10
24	$\overline{OE}$
25	A11
26	A9
27	A8
28	A13
29	A14
30	NC
31	$\overline{WE}$
32	V_{CC}

FIGURE 2. Terminal connections.

Pins		V_{PP} 1/	A_0	A_9	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$DQ_0 - DQ_7$
Read only	Operation							
	Read	V_{PPL}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data out
	Output disable	V_{PPL}	X 2/	X 2/	V_{IL}	V_{IH}	V_{IH}	3-state
	Standby	V_{PPL}	X 2/	X 2/	V_{IH}	X 2/	X 2/	3-state
	Auto-select manufacturer code 3/	V_{PPL}	V_{IL}	V_{ID} 4/	V_{IL}	V_{IL}	V_{IH}	5/
	Auto-select device code 3/	V_{PPL}	V_{IH}	V_{ID} 4/	V_{IL}	V_{IL}	V_{IH}	6/
Read/write	Read	V_{PPH}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data out 7/
	Output disable	V_{PPH}	X 2/	X 2/	V_{IL}	V_{IH}	V_{IH}	3-state
	Standby 8/	V_{PPH}	X 2/	X 2/	V_{IH}	X 2/	X 2/	3-state
	Write	V_{PPH}	A_0	A_9	V_{IL}	V_{IH}	V_{IL}	Data in 9/

1/ Refer to dc characteristics. When $V_{PP} = V_{PPL}$ memory contents can be read but not written or erased.
2/ X can be V_{IL} or V_{IH}.
3/ Manufacture and device code may also be accessed via a command register write sequence.
4/ V_{ID} is the auto select high voltage. Refer to dc characteristics.
5/ The output for $DQ_0 - DQ_7$ shall be as follows:

$DQ_0 - DQ_7$
DATA = 89H
DATA = 01H

6/ The output for $DQ_0 - DQ_7$ shall be as follows:

$DQ_0 - DQ_7$
DATA = B4H
DATA = A7H

7/ Read operations with $V_{PP} = V_{PPH}$ may access array data or the auto select codes.
8/ With V_{PP} at high voltage, the standby current equals $I_{CC} + I_{PP}$ (standby).
9/ Refer to command definitions for valid Data-In during a write operation.

Bus operations

FIGURE 3. Truth tables.

Command	BUS cycles required	First BUS cycle			Second BUS cycle		
		Operation 1/	Address 2/	Data 3/	Operation 1/	Address 2/	Data 3/
Read memory	1	Write	X	00H	Read	RA	RD
Read auto select codes 4/	2	Write	X	90H	Read	IA	ID
Setup erase/erase	2	Write	X	20H	Write	X	20H
Erase verify	2	Write	EA	A0H	Read	X	EVD
Setup program/program	2	Write	X	40H	Write	PA	PD
Program verify	2	Write	X	C0H	Read	X	PVD
Reset 5/	2	Write	X	FFH	Write	X	FFH

1/ Refer to BUS operations for definitions.
2/ RA = Address of the memory location to be read.
IA = Identifier address: 00H for manufacturer code, 01H for device code.
EA = Address of memory location to be read during erase verify.
PA = Address of memory location to be programmed.
Address are latched on the falling edge of the write-enable pulse.
3/ RD = Data read from location RA during read operation.
ID = Data read from location IA during device identification.
EVD = Data read from location EA during erase verify.
PD = Data to be programmed at location PA. Data is latched on the rising edge of write-enable.
PVD = Data read from location PA during program verify. PA is latched on the program command.
4/ Following the read Auto Select code ID command, two read operations access manufacturer and device codes.
5/ The second bus cycle must be followed by the desired command register write.

Command definitions

FIGURE 3. Truth tables - Continued.

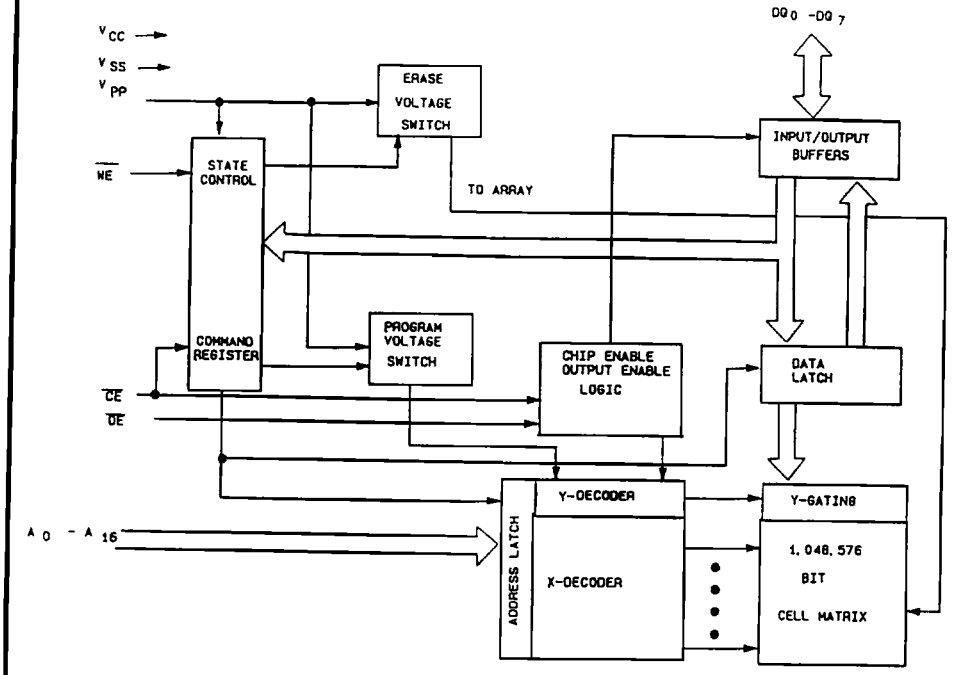

FIGURE 4. Block diagram.

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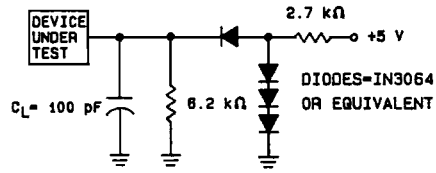
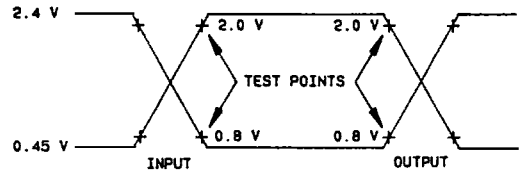


SWITCHING TEST CIRCUIT (OR EQUIVALENT)

C_L includes jig capacitance



AC testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.

FIGURE 5. Switching test circuits and waveforms.

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		REVISION LEVEL	SHEET 18

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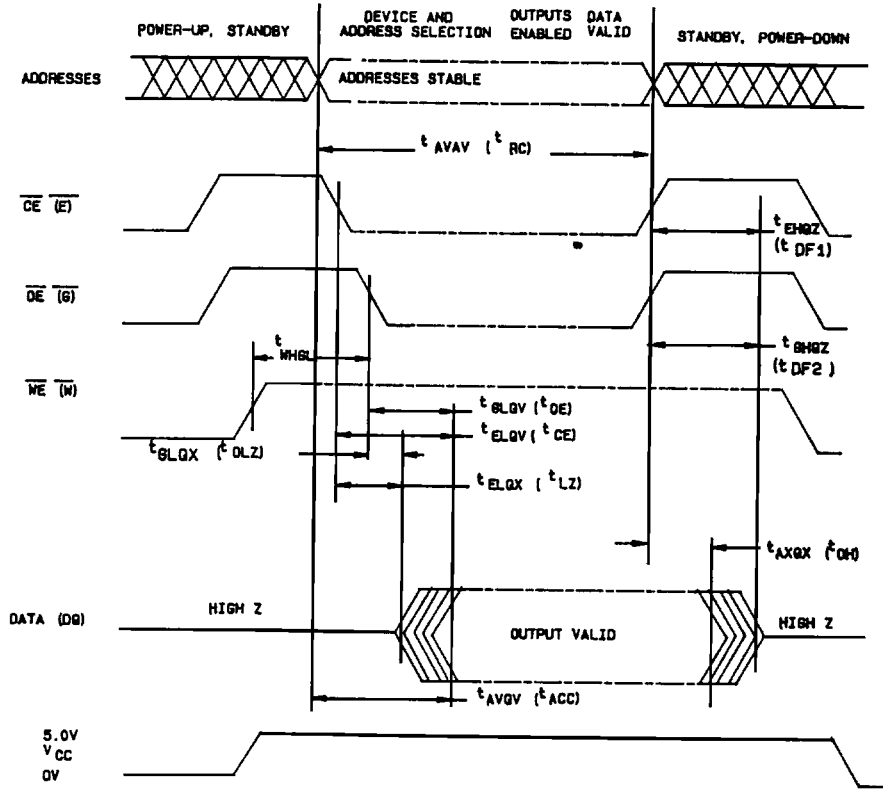

AC waveforms for read operations

FIGURE 5. Switching test circuits and waveforms - Continued.

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		REVISION LEVEL	SHEET 19

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. Prior to burn-in, the devices shall be programmed (see 4.5.2 herein) with a checkerboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the PDA calculation and shall be removed from the lot (see 4.2.3 herein).

c. For device class M, the burn-in test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device classes B and S, the burn-in test circuit shall be submitted to the qualifying activity. For device classes Q and V, the burn-in test circuit shall be submitted to DESC-ECS with the certificate of compliance and under the control of the device manufacturer's Technical Review Board (TRB) in accordance with MIL-I-38535.

(1) Static burn-in for device classes S and V (method 1015 of MIL-STD-883, test condition A).

(a) All inputs shall be connected to GND. Outputs may be open or connected to 4.5 V minimum. Resistors R1 are optional on both inputs and outputs, and required on outputs connected to V_{CC} ±0.5 V. R1 = 220 ohms to 47 kilohms. For static II burn-in, reverse all input connections (i.e., V_{SS} to V_{CC}).

(b) V_{CC} = 4.5 V minimum.

(c) Ambient temperature (T_A) shall be +125°C minimum.

(d) Test duration for the static test shall be 48 hours minimum. The 48-hour burn-in shall be broken into two sequences of 24 hours each (static I and static II) followed by interim electrical measurements.

(2) Dynamic burn-in for device classes M, B, S, Q, and V (method 1015 of MIL-STD-883, test condition D) using the circuit submitted (see 4.2.1c herein).

d. Interim and final electrical parameters shall be as specified in table IIA herein.

e. For classes S and B devices, post dynamic burn-in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

f. A data retention stress and margin test shall be included and shall consist of the following steps:

(1) All devices shall be written with a charge opposite the state that the cell would read in its equilibrium state (e.g. worst case pattern). Verify margin to be > 6.0 volts.

(2) After writing, perform a high temperature unbiased storage for 48 hours at 150°C minimum. The storage time may be accelerated by using a higher temperature in accordance with the Arrhenius relationship and with an apparent activation energy of .6 ev. The maximum storage temperature shall not exceed 200°C for assembled devices and 300°C for unassembled devices.

(3) Read the data retention pattern and test using subgroups 1, 7, and 9 minimum, (e.g. high temperature equivalent subgroups 2, 8A and 10 may be used) after bake, prior to burn-in. Devices having bits not in the proper state after storage shall constitute a device failure. Verify margin to be > 5.75 volts.

g. After the completion of all screening, the device shall be erased and verified prior to delivery.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.2.3 Percent defective allowable (PDA).

a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. The PDA for class B devices shall be in accordance with MIL-M-38510 for dynamic burn-in.

c. Static burn-in I and II failures shall be cumulative for determining PDA.

d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table I, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

e. The PDA for device classes Q and V shall be in accordance with MIL-I-38535 for dynamic burn-in.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Qualification data for subgroups 7, 8A, and 8B shall be attributes only.

4.3.1.1 Qualification extension inspection for device classes B and S. When authorized by the qualifying activity, if a manufacturer qualifies one device type which is identical (i.e., same die), to other device types on this specification, the slower device types may be part I qualified, upon the request of the manufacturer, without any further testing. The faster device types may be part I qualified by performing only group A qualification data testing.

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

TABLE IIA. Elecrtical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
		Device class M	Device class B	Device class S	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9 or 2,8A,10	1,7,9 or 2,8A,10	1,7,9 or 2,8A,10	1,7,9 or 2,8A,10
2	Static burn-in I method 1015	Not required	Not required	Required	Not required	Not required
3	Same as line 1			1*,7* Δ		1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required	Required	Required
5	Same as line 1			1*,7* Δ		1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group B end-point electrical parameters			1,2,3,7, 8A,8B,9,10, 11 Δ		
9	Group C end-point electrical parameters	2,8A,10	1,2,3,7, 8A,8B Δ		1,2,3,7 8A,8B Δ	1,2,3,7, 8A,8B,9,10, 11 Δ
10	Group D end-point electrical parameters	2,8A,10	2,3,7 8A,8B	2,3,7 8A,8B	2,3,7 8A,8B	2,3,7 8A,8B
11	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate test are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * Indicates PDA applies to subgroups 1 and 7.
5/ ** See 4.4.1c.
6/ Δ Indicates delta limit (see table IIC) shall be required where specified, and the delta values shall be computed with reference to the previous electrical parameters (see table IIC).
7/ See 4.4.1e.

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures and all input and output terminals tested.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

e. O/V (latchup) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. Procedures and circuits shall be submitted to DESC-ECS for class M device. For classes B or S the procedures and circuits shall be submitted to the qualifying activity. For classes Q or V the procedures and circuits shall be submitted to DESC-ECS and will be under the control of the device manufacturer's TRB. Testing shall be on all pins, on 5 devices with zero failures. Latchup test shall be considered destructive. JEDEC standard no. 17 may be used as a guideline for latchup testing.

f. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified, (except devices submitted for groups B, C, and D testing).

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

a. For device class S, steady-state life test circuits shall be conducted using test condition D and the circuit described in 4.2.1c herein, or equivalents approved by the qualifying activity.

b. For device class S only, end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 5 of group B inspections and shall consist of tests specified in table IIC herein.

c. All devices selected for class S electrical testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted to groups C and D).

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C and shall consist of test specified in table IIC herein.

4.4.3.1 Additional criteria for device classes M and B.

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) The device selected for testing shall be programmed with a checkerboard pattern. After completion of all testing, the devices shall be erased and verified (except devices submitted for group D testing).

(2) Test condition D or E. For device class M, the test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

(3) T_A = +125°C, minimum.

(4) Test duration: 1,000 hours, except as specified in method 1005 of MIL-STD-883.

b. All devices requiring end-point electrical testing shall be programmed with a checkerboard or equivalent alternating bit pattern.

c. An endurance test, per method 1033 of MIL-STD-883, shall be added to group C1 inspection prior to performing the steady state life test (see 4.4.3.1a) and extended data retention (see 4.4.3.1d). Cycling will be on the bulk chip basis from devices passing group A after the completion of the requirements of 4.2 herein. Initially, two (2) groups of devices shall be formed, cell 1 and cell 2. The following conditions shall be met:

(1) Cell 1 shall be cycled at -55°C and cell 2 shall be cycled at +125°C for a minimum of 10,000 cycles for device types 01, 02, 03, and 04 and 1,000 cycles for device types 05, 06, 07, and 08.

(2) Perform group A subgroups 1, 7, and 9 after cycling. Form two (2) new cells (cells 3 and 4) for steady-state life test consist of one-half of devices from cell 1 and one-half of the devices from cell 2. Cell 4 for extended data retention consists of the remaining devices from cells 1 and 2.

(3) The sample plans for cell 1, cell 2, cell 3, and cell 4 shall individually be the same as for group C1, as specified in method 5005 of MIL-STD-883.

d. Extended data retention test shall consist of the following:

(1) All devices shall be programmed with a charge on all memory cells in each device such that the cell will read opposite the state that the cell would read in its equilibrium state (e.g., worst case pattern).

(2) Unbiased bake for 1000 hours (minimum) at +150°C (minimum). The unbiased bake time may be accelerated by using higher temperature in accordance with the Arrhenius Relationship.

$$A_F = e^{-\frac{EA}{K}\left[\frac{1}{T_1} - \frac{1}{T_2}\right]}$$

A_F = acceleration factor (unitless quantity) = t_1/t_2.
T = Temperature in Kelvin (i.e., t_1 +273 = °K).
t_1 = time (hrs) at temperature T_1.
t_2 = time (hrs) at temperature T_2.
K = Boltzmanns constant = 8.62×10^{-5} eV/°K using an apparent activation energy (E_A) of 0.6 V.
(E_A) of 0.6 V.

(3) Read the pattern after bake and perform end-point electrical tests for table IIA herein for group C.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein. The devices selected for testing shall be programmed with a checkerboard pattern. After completion of all testing, the devices shall be erased and verified.

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hours at +125°C	100%
Radiographic	2012	100%

TABLE IIC. Delta limits at 25°C.

Test 1/	Device types
	All
I_{CCS} standby	±10 percent of specified value in table I.
I_{LI}	±10 percent of specified value in table I.
I_{LO}	±10 percent of specified value in table I.

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine delta.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). The group E inspection end-point electrical parameters shall be as specified in table IIA herein. RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document or to a higher qualified level. RHA tests for device classes Q and V shall be performed in accordance with MIL-I-38535 and 1.2.1 herein.

a. RHA tests for device classes B, S, Q, and V for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table I herein. RHA samples need not be tested at -55°C or +125 prior to total dose irradiation.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. The samples shall pass the specified group A electrical parameters for subgroups specified in table IIA herein. Additionally classes Q and V, for quality conformance inspection may be at wafer level.

d. The device shall be subjected to radiation hardness assurance tests as specified in MIL-M-38510, (device classes M, B, and S) and MIL-I-38535, (device classes Q and V) for the RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = 25°C ±5°C, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition established during characterization.

f. SEP testing, shall be performed on all class S and V devices. SEP testing shall be performed at initial qualification and after any design or process changes which may affect the upset or latchup characteristics of the device. Test four devices with zero failures. ASTM standard F1192-88 may be used as a guideline when performing SEP testing. For device class V, the device parametrics that influence single event upset immunity shall be monitored at the wafer level as part of a TRB approved wafer level hardness plan. The test conditions for SEP are as follows:

(1) The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e., 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

(2) The fluence shall be greater than 100 errors or ≥ 10^7 ions/cm^2.

(3) The flux shall be between 10^2 and 10^5 ion/cm^2/s. The cross section shall be verified to be flux independent by measuring the cross section to two flux rates which differ by at least on order of magnitude.

(4) The particle range shall be ≥ 20 microns in silicon.

(5) The test temperatures shall be +25°C and also the maximum rated operating temperature ±10°C.

(6) Bias conditions shall be V_{CC} = 4.5 V dc for the upset measurements and V_{CC} = 5.5 V dc for the latchup measurements.

g. For device classes M, B, and S, subgroups 1 and 2 of table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

h. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-I-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-I-38535.

i. Transient dose rate survivability testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-I-38535. Device parametric parameters that influence latchup and device burn-out shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-I-38535.

j. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

(1) RHA delta limits.

(2) RHA upset levels.

(3) Test conditions (SEP).

(4) Number of upset (SEP).

(5) Number of transients.

(6) Occurrence of latchup.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate figures and tables as follows.

4.5.1 Erasing procedures. The erasing procedures shall be as specified by the device manufacturer and shall be available upon request.

4.5.2 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.6 Delta measurements for device classes B, S, Q, and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIC.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6047.

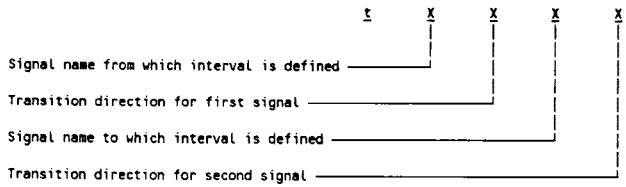
6.4 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

C_{IN}, C_{OUT}	Input and bidirectional output, terminal-to-GND capacitance.
GND	Ground zero voltage potential.
I_{CC}	Supply current.
I_{IL}	Input current low.
I_{IH}	Input current high.
T_C	Case temperature.
T_A	Ambient temperature.
V_{CC}	Positive supply voltage.
V_H	Output enable and Write enable voltage during chip erase.
O/V	Latchup over-voltage.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case subscripts. The initial character is always "t" and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transition. Thus the format is:



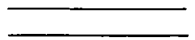
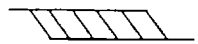
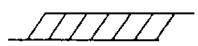
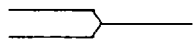
a. Signal definitions:

A = Address
D = Data in
Q = Data out
W = Write enable
E = Chip enable
O = Output enable

b. Transition definitions:

H = Transition to high
L = Transition to low
V = Transition to valid
X = Transition to invalid or don't care
Z = Transition to off (high impedance)

6.5.3 Waveforms.

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECS and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 92-08-31

Approved sources of supply for SMD 5962-90899 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECS. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9089901MXX	34335	AM28F010-250/BXA
	34649	MD28F010-25/B
5962-9089901MYX	34335	AM28F010-250/BUA
	34649	MR28F010-25/B
5962-9089901MTX	34649	MT28F010-25/B
5962-9089901MZX	34649	MZ28F010-25/B
5962-9089901MUX	34649	MF28F010-25/B
5962-9089902MXX	34335	AM28F010-200/BXA
	34649	MD28F010-20/B
5962-9089902MYX	34335	AM28F010-200/BUA
	34649	MR28F010-20/B
5962-9089902MTX	34649	MT28F010-20/B
5962-9089902MZX	34649	MZ28F010-20/B
5962-9089902MUX	34649	MF28F010-20/B
5962-9089903MXX	34335	AM28F010-150/BXA
	34649	MD28F010-15/B
5962-9089903MYX	34335	AM28F010-150/BUA
	34649	MR28F010-15/B
5962-9089903MTX	34649	MT28F010-15/B
5962-9089903MZX	34649	MZ28F010-15/B
5962-9089903MUX	34649	MF28F010-15/B
5962-9089904MXX	34335	AM28F010-120/BXA
	34649	MD28F010-12/B
5962-9089904MYX	34335	AM28F010-120/BUA
	34649	MR28F010-12/B
5962-9089904MTX	34649	MT28F010-12/B
5962-9089904MZX	34649	MZ28F010-12/B
5962-9089904MUX	34649	MF28F010-12/B
5962-9089905MXX	34335	AM28F010-250C3/BXA
	34649	MD28F010-25/B
5962-9089905MYX	34335	AM28F010-250C3/BUA
	34649	MR28F010-25/B
5962-9089905MTX	34649	MT28F010-25/B
5962-9089905MZX	34649	MZ28F010-25/B
5962-9089905MUX	34649	MF28F010-25/B

See footnote at end of table

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9089906MXX	34335	AM28F010-200C3/BXA
	34649	MD28F010-20/B
5962-9089906MYX	34335	AM28F010-200C3/BUA
	34649	MR28F010-20/B
5962-9089906MTX	34649	MT28F010-20/B
5962-9089906MZX	34649	MZ28F010-20/B
5962-9089906MUX	34649	MF28F010-20/B
5962-9089907MXX	34335	AM28F010-150C3/BXA
	34649	MD28F010-15/B
5962-9089907MYX	34335	AM28F010-150C3/BUA
	34649	MR28F010-15/B
5962-9089907MTX	34649	MT28F010-15/B
5962-9089907MZX	34649	MZ28F010-15/B
5962-9089907MUX	34649	MF28F010-15/B
5962-9089908MXX	34335	AM28F010-120C3/BXA
	34649	MD28F010-12/B
5962-9089908MYX	34335	AM28F010-120C3/BUA
	34649	MR28F010-12/B
5962-9089908MTX	34649	MT28F010-12/B
5962-9089908MZX	34649	MZ28F010-12/B
5962-9089908MUX	34649	MF28F010-12/B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address	Manufacturer code	Device code
34335	Advanced Micro Devices, Incorporated 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088	01H	A7H
34649	Intel Corporation 5000 West Chandler Blvd. Chandler, AZ 85226	89H	B4H

The cross-reference information below is presented for the convenience of users. Microcircuits covered by SMD 5962-90899 will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges, postirradiation performance, or reliability factors equivalent to the listed SMD device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for SMD types or as a waiver of any of the provisions of the applicable general specification.

Standardized military drawing PIN	Generic industry PIN 1/
5962-9089901MXX	28F010-250
5962-9089901MYX	28F010-250
5962-9089901MTX	28F010-250
5962-9089901MZX	28F010-250
5962-9089901MUX	28F010-250
5962-9089902MXX	28F010-200
5962-9089902MYX	28F010-200
5962-9089902MTX	28F010-200
5962-9089902MZX	28F010-200
5962-9089902MUX	28F010-200
5962-9089903MXX	28F010-150
5962-9089903MYX	28F010-150
5962-9089903MTX	28F010-150
5962-9089903MZX	28F010-150
5962-9089903MUX	28F010-150
5962-9089904MXX	28F010-120
5962-9089904MYX	28F010-120
5962-9089904MTX	28F010-120
5962-9089904MZX	28F010-120
5962-9089904MUX	28F010-120
5962-9089905MXX	28F010-250
5962-9089905MYX	28F010-250
5962-9089905MTX	28F010-250
5962-9089905MZX	28F010-250
5962-9089905MUX	28F010-250
5962-9089906MXX	28F010-200
5962-9089906MYX	28F010-200
5962-9089906MTX	28F010-200
5962-9089906MZX	28F010-200
5962-9089906MUX	28F010-200
5962-9089907MXX	28F010-150
5962-9089907MYX	28F010-150
5962-9089907MTX	28F010-150
5962-9089907MZX	28F010-150
5962-9089907MUX	28F010-150
5962-9089908MXX	28F010-120
5962-9089908MYX	28F010-120
5962-9089908MTX	28F010-120
5962-9089908MZX	28F010-120
5962-9089908MUX	28F010-120

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.