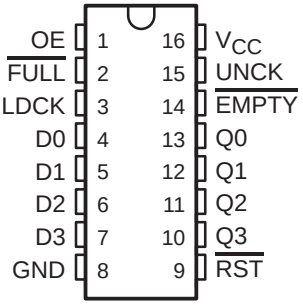
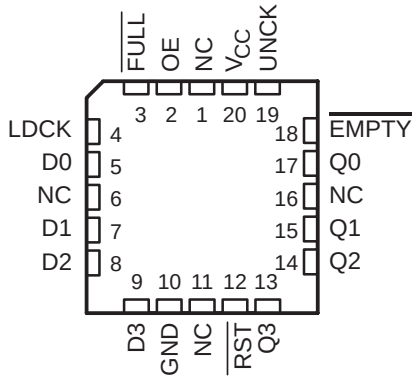
SCAS251B – FEBRUARY 1989 – REVISED APRIL 1998

- **Independent Asynchronous Inputs and Outputs**
- **16 Words by 4 Bits**
- **Data Rates up to 40 MHz**
- **Fall-Through Time 14 ns Typical**
- **3-State Outputs**
- **Package Options Include Plastic Small-Outline Package (DW), Plastic Chip Carriers (FN), and Standard Plastic 300-mil DIPs (N)**

**DW OR N PACKAGE**
**(TOP VIEW)**




**FN PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

This 64-bit memory features high speed and fast fall-through times. It is organized as 16 words by 4 bits.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates up to 40 MHz in a bit-parallel format, word by word.

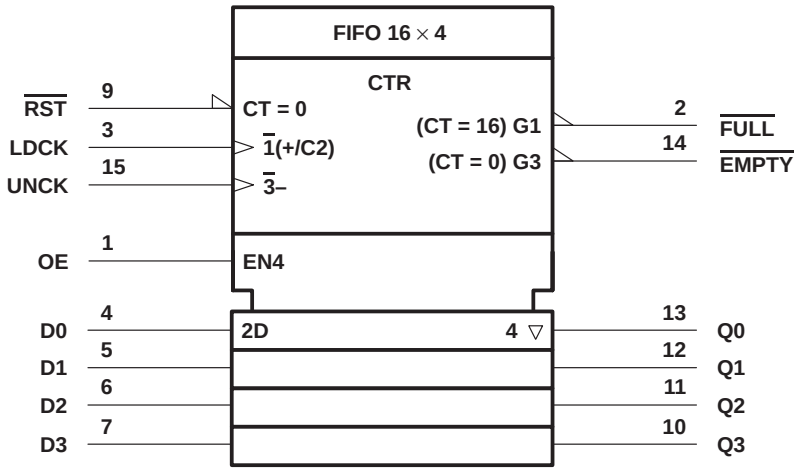
Data is written into memory on a low-to-high transition at the load-clock (LDCK) input and is read out on a low-to-high transition at the unload-clock (UNCK) input. The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ output flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when it is not full. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty.

A low level on the reset ($\overline{\text{RST}}$) input resets the internal stack-control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$ high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a $\overline{\text{RST}}$ pulse or from an empty condition, causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable (OE) input is low. OE does not affect the $\overline{\text{FULL}}$ or $\overline{\text{EMPTY}}$ output flags. Cascading is easily accomplished in the word-width direction but is not possible in the word-depth direction.

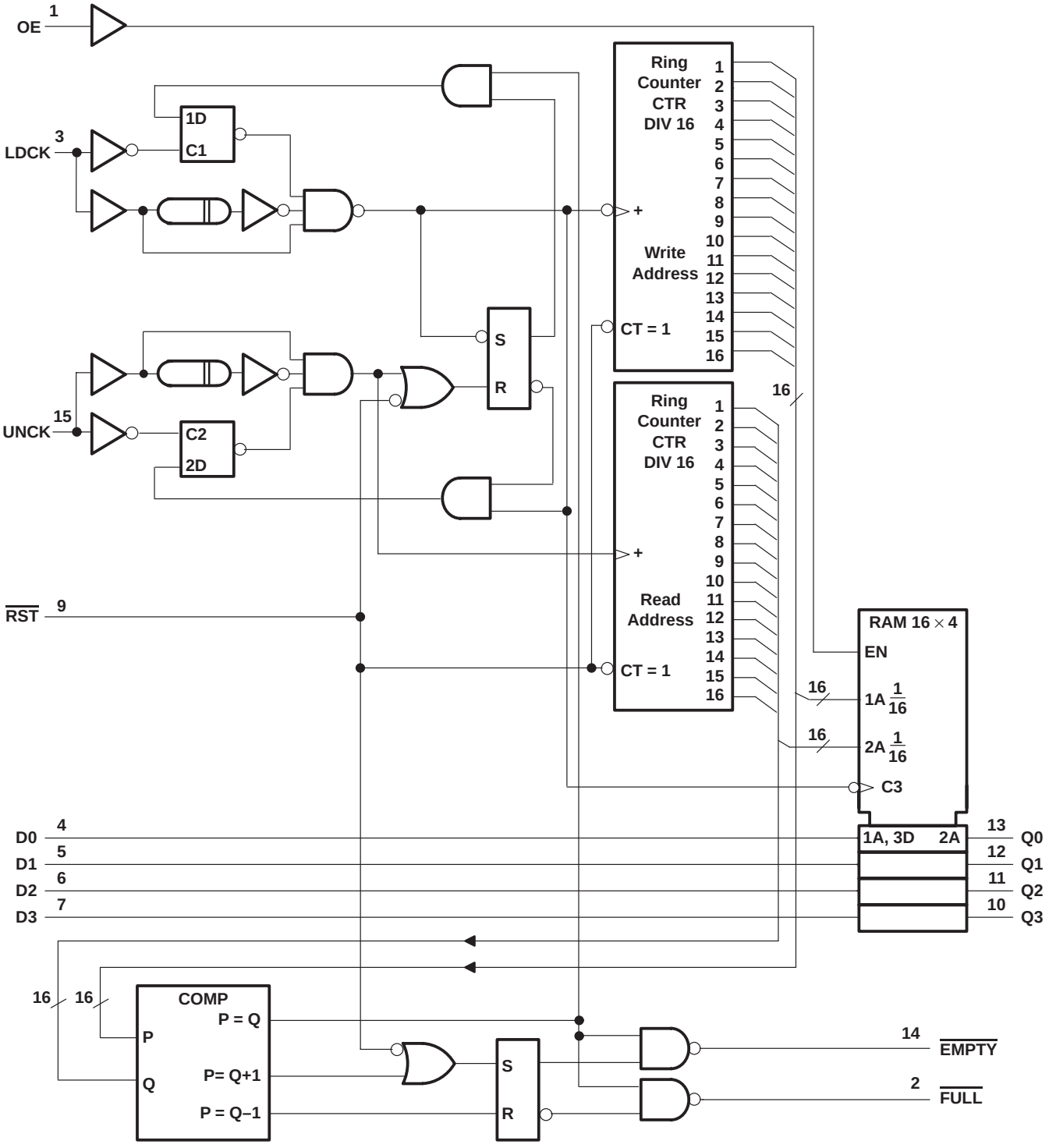
The SN74ALS232B is characterized for operation from 0°C to 70°C.

## logic symbol†



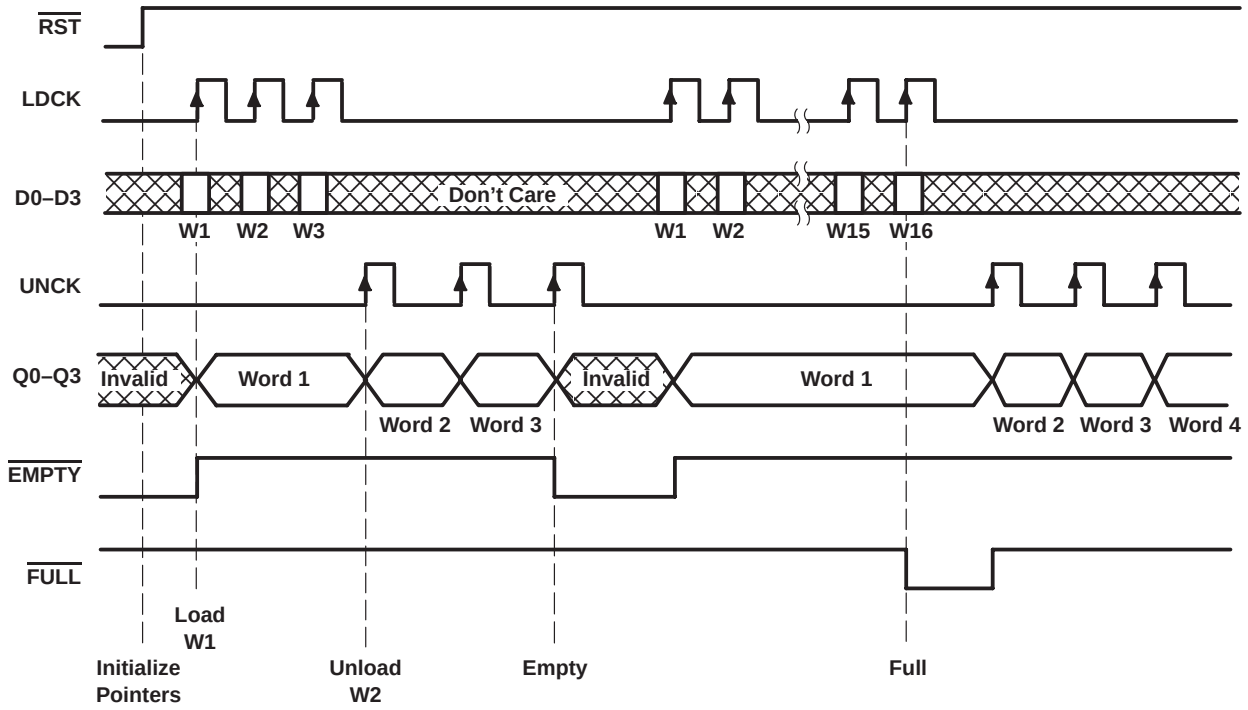

† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.
Pin numbers shown are for the DW and N packages.

## logic diagram (positive logic)




Pin numbers shown are for the DW and N packages.

## timing diagram




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ . . . . . –0.5 V to 7 V
Voltage range applied to a disabled 3-state output . . . . . –0.5 V to 5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package . . . . . 105°C/W
FN package . . . . . 83°C/W
N package . . . . . 78°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | Q outputs | | | –2.6 | mA |
| | | $\overline{FULL}$, $\overline{EMPTY}$ | | | –0.4 | |
| $I_{OL}$ | Low-level output current | Q outputs | | | 24 | mA |
| | | $\overline{FULL}$, $\overline{EMPTY}$ | | | 8 | |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

NOTE 3: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates limits for maximum $V_{IL}$, minimum $V_{IH}$, or minimum pulse duration can cause a false clock or improper operation of the internal read and write pointers.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | V |
| $V_{OH}$ | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –2.6 mA | 2.4 | 3.2 | | V |
| | $\overline{FULL}$, $\overline{EMPTY}$ | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = –0.4 mA | $V_{CC}$–2 | | | |
| $V_{OL}$ | Q outputs | $V_{CC}$ = 4.5 V | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 24 mA | | 0.35 | 0.5 | |
| | $\overline{FULL}$, $\overline{EMPTY}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | |
| | | | $I_{OL}$ = 8 mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 20 | µA |
| $I_{OZL}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | –20 | µA |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | –0.2 | mA |
| $I_O$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | –30 | | –112 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V | | | 80 | 125 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, $I_{OS}$.

## timing requirements over recommended operating free-air temperature range (see Figure 1)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{clock}$† | Clock frequency | LDCK | | | 40 | MHz |
| | | UNCK | | | 40 | |
| $t_w$ | Pulse duration | $\overline{RST}$ low | 18 | | | ns |
| | | LDCK low | 15 | | | |
| | | LDCK high | 10 | | | |
| | | UNCK low | 15 | | | |
| | | UNCK high | 10 | | | |
| $t_{su}$ | Setup time | Data before LDCK↑ | 8 | | | ns |
| | | LDCK inactive before $\overline{RST}$↑ | 5 | | | |
| $t_h$ | Hold time | Data after LDCK↑ | 5 | | | ns |
| | | LDCK inactive after $\overline{RST}$↑ | 5 | | | |

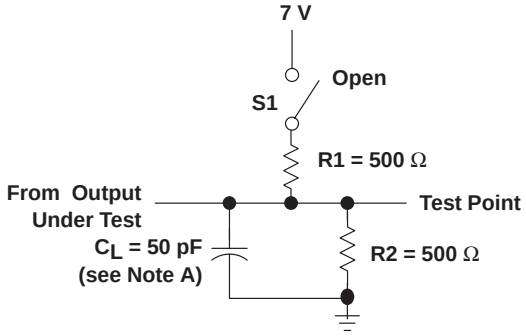
† The maximum possible clock frequency is 40 MHz. The maximum clock frequency when using a 50% duty cycle is 33.3 MHz.

## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP‡ | MAX | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | LDCK, UNCK | | | 50 | | 40 | | MHz |
| $t_{pd}$ | LDCK↑ | Any Q | | 14 | 23 | 6 | 30 | ns |
| | UNCK↑ | | | 15 | 23 | 6 | 30 | |
| $t_{PLH}$ | LDCK↑ | $\overline{EMPTY}$ | | 13 | 20 | 5 | 25 | ns |
| $t_{PHL}$ | UNCK↑ | $\overline{EMPTY}$ | | 15 | 22 | 6 | 27 | ns |
| | $\overline{RST}$↓ | | | 15 | 21 | 5 | 26 | |
| | LDCK↑ | $\overline{FULL}$ | | 15 | 22 | 6 | 27 | |
| $t_{PLH}$ | UNCK↑ | $\overline{FULL}$ | | 13 | 20 | 5 | 25 | ns |
| | $\overline{RST}$↓ | | | 16 | 23 | 7 | 28 | |
| $t_{en}$ | OE↑ | Q | | 5 | 12 | 1 | 14 | ns |
| $t_{dis}$ | OE↓ | Q | | 5 | 12 | 1 | 16 | ns |

‡ Typical values at $V_{CC}$ – 5 V, $T_A$ = 25°C.

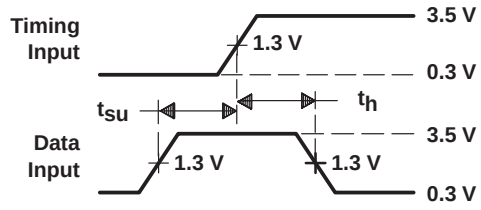
## PARAMETER MEASUREMENT INFORMATION



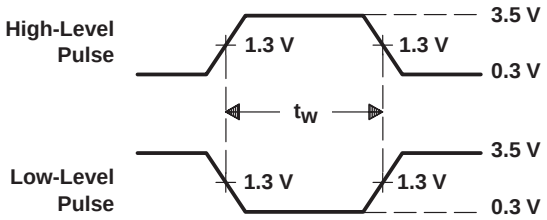

LOAD CIRCUIT FOR 3-STATE OUTPUTS

**SWITCH POSITION TABLE**

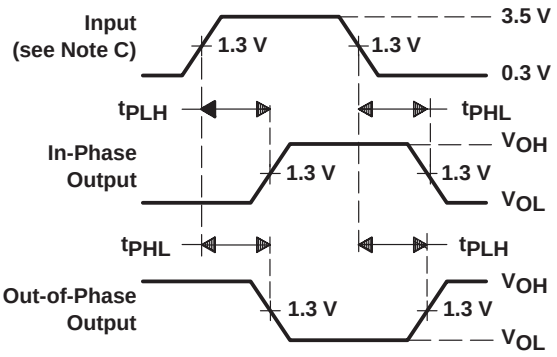
| PARAMETER | | S1 |
|---|---|---|
| $t_{en}$ | $t_{PZH}$ | Open |
| | $t_{PZL}$ | Closed |
| $t_{dis}$ | $t_{PHZ}$ | Open |
| | $t_{PLZ}$ | Closed |
| $t_{pd}$ | $t_{PLH}$ | Open |
| | $t_{PHL}$ | Open |



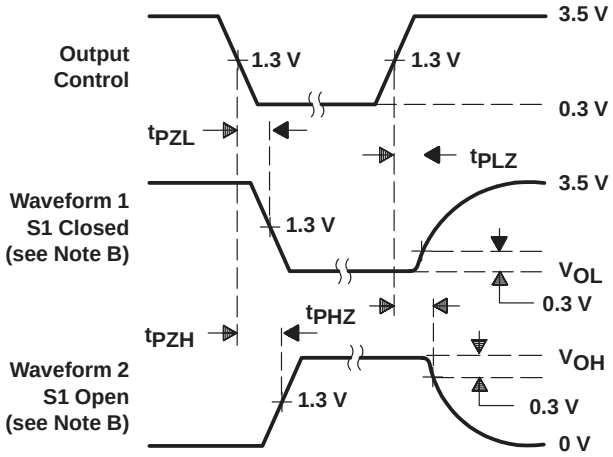

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

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