SN54ACT00, SN74ACT00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES
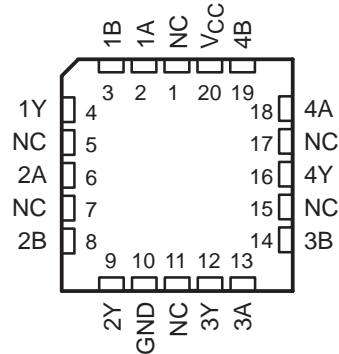
- **4.5-V to 5.5-V V$_{CC}$ Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Max t$_{pd}$ of 8 ns at 5 V**
- **Inputs Are TTL-Voltage Compatible**

SN54ACT00 . . . J OR W PACKAGE
SN74ACT00 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)

```
        ┌───────┐
1A  [ 1   U   14 ]  V_CC
1B  [ 2       13 ]  4B
1Y  [ 3       12 ]  4A
2A  [ 4       11 ]  4Y
2B  [ 5       10 ]  3B
2Y  [ 6        9 ]  3A
GND [ 7        8 ]  3Y
        └───────┘
```
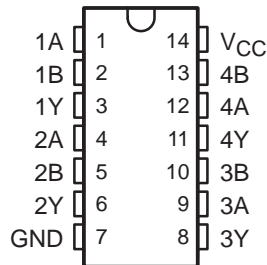
SN54ACT00 . . . FK PACKAGE
(TOP VIEW)

```
          1B  1A  NC  V_CC 4B
           3   2   1  20  19
        ┌─────────────────────┐
1Y  [ 4                   18 ]  4A
NC  [ 5                   17 ]  NC
2A  [ 6                   16 ]  4Y
NC  [ 7                   15 ]  NC
2B  [ 8                   14 ]  3B
        └─────────────────────┘
           9  10  11  12  13
          2Y  GND  NC  3Y  3A
```

NC – No internal connection

description/ordering information

The 'ACT00 devices contain four independent 2-input NAND gates. Each gate performs the Boolean function of $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

ORDERING INFORMATION

T$_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP – N	Tube	SN74ACT00N	SN74ACT00N
	SOIC – D	Tube	SN74ACT00D	ACT00
		Tape and reel	SN74ACT00DR	
	SOP – NS	Tape and reel	SN74ACT00NSR	ACT00
	SSOP – DB	Tape and reel	SN74ACT00DBR	AD00
	TSSOP – PW	Tube	SN74ACT00PW	AD00
		Tape and reel	SN74ACT00PWR	
−55°C to 125°C	CDIP – J	Tube	SNJ54ACT00J	SNJ54ACT00J
	CFP – W	Tube	SNJ54ACT00W	SNJ54ACT00W
	LCCC – FK	Tube	SNJ54ACT00FK	SNJ54ACT00FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	**B**	**Y**
H	H	L
L	X	H
X	L	H

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TEXAS INSTRUMENTS

SN54ACT00, SN74ACT00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

logic diagram, each gate (positive logic)

A ———┐
      ⊃o——— Y
B ———┘

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) .... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±200 mA
Package thermal impedance, θ_{JA} (see Note 2): D package .... 86°C/W
　　　　　　　　　　　　　　　　　　　　　　　　DB package .... 96°C/W
　　　　　　　　　　　　　　　　　　　　　　　　N package .... 80°C/W
　　　　　　　　　　　　　　　　　　　　　　　　NS package .... 76°C/W
　　　　　　　　　　　　　　　　　　　　　　　　PW package .... 113°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
　　　　2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54ACT00		SN74ACT00		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		8		8	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$			SN54ACT00		SN74ACT00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50\ \mu A$		4.5 V	4.4	4.49		4.4		4.4		V
			5.5 V	5.4	5.49		5.4		5.4		
	$I_{OH} = -24\ mA$		4.5 V	3.86			3.7		3.76		
			5.5 V	4.86			4.7		4.76		
	$I_{OH} = -50\ mA$†		5.5 V				3.85				
	$I_{OH} = -75\ mA$†		5.5 V						3.85		
V_{OL}	$I_{OL} = 50\ \mu A$		4.5 V		0.001	0.1		0.1		0.1	V
			5.5 V		0.001	0.1		0.1		0.1	
	$I_{OL} = 24\ mA$		4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
	$I_{OL} = 50\ mA$†		5.5 V					1.65			
	$I_{OL} = 75\ mA$†		5.5 V							1.65	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	$I_O = 0$	5.5 V			2		40		20	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}		5.5 V		0.6			1.6		1.5	mA
C_i	$V_I = V_{CC}$ or GND		5 V		2.6						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\ V \pm 0.5\ V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25°C$			SN54ACT00		SN74ACT00		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	5.5	9	1	9.5	1	9.5	ns
t_{PHL}			1.5	4	7	1	8	1	8	

operating characteristics, $V_{CC} = 5\ V$, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\ pF$, $f = 1\ MHz$	40	pF

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open

From Output Under Test

500 Ω   **S1**   ○ $2 \times V_{CC}$
                     ○ Open

C_L = 50 pF
(see Note A)

500 Ω

LOAD CIRCUIT

Input   3 V
            1.5 V   1.5 V
            0 V

t_{PLH} t_{PHL}

In-Phase Output V_{OH}
                      50% V_{CC} 50% V_{CC}
                      V_{OL}

t_{PHL} t_{PLH}

Out-of-Phase Output V_{OH}
                          50% V_{CC} 50% V_{CC}
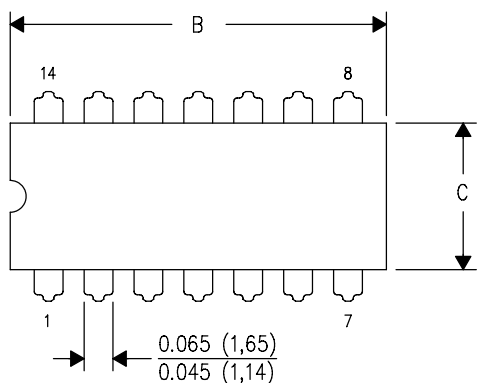 V_{OL}

VOLTAGE WAVEFORMS
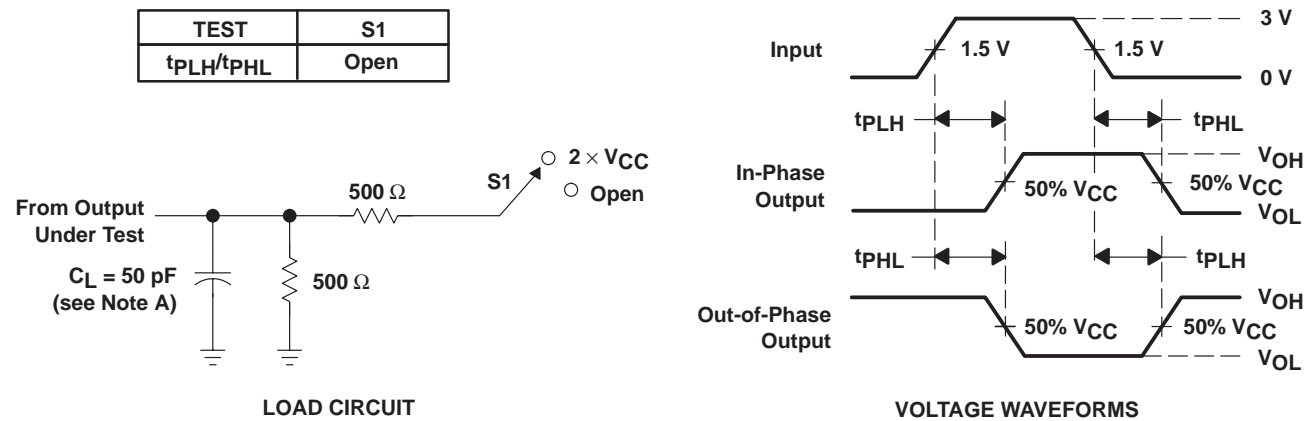
NOTES: A. C_L includes probe and jig capacitance.
       B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
       C. The outputs are measured one at a time with one input transition per measurement.
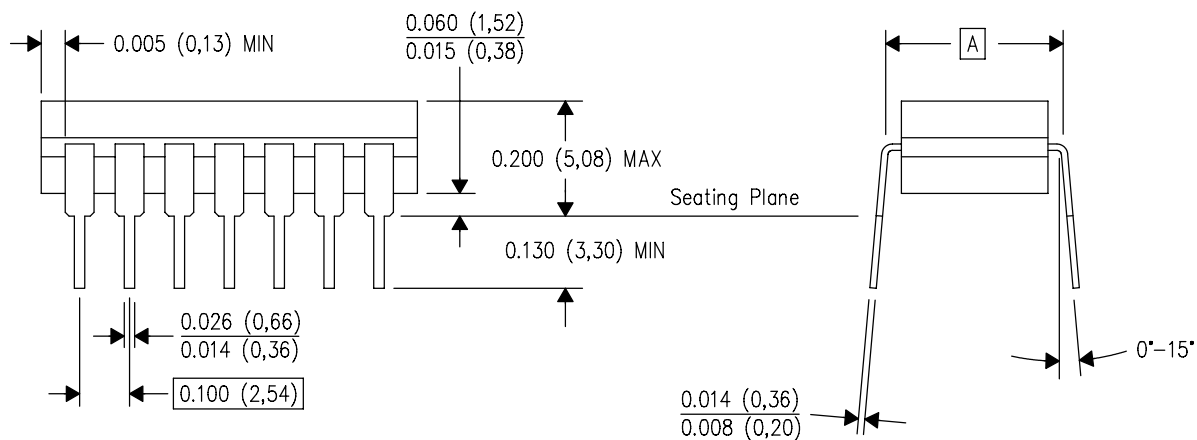
Figure 1. Load Circuit and Voltage Waveforms

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

$\frac{0.065\ (1,65)}{0.045\ (1,14)}$

0.005 (0,13) MIN

$\frac{0.060\ (1,52)}{0.015\ (0,38)}$

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

$\frac{0.026\ (0,66)}{0.014\ (0,36)}$

0.100 (2,54)

A

0°—15°

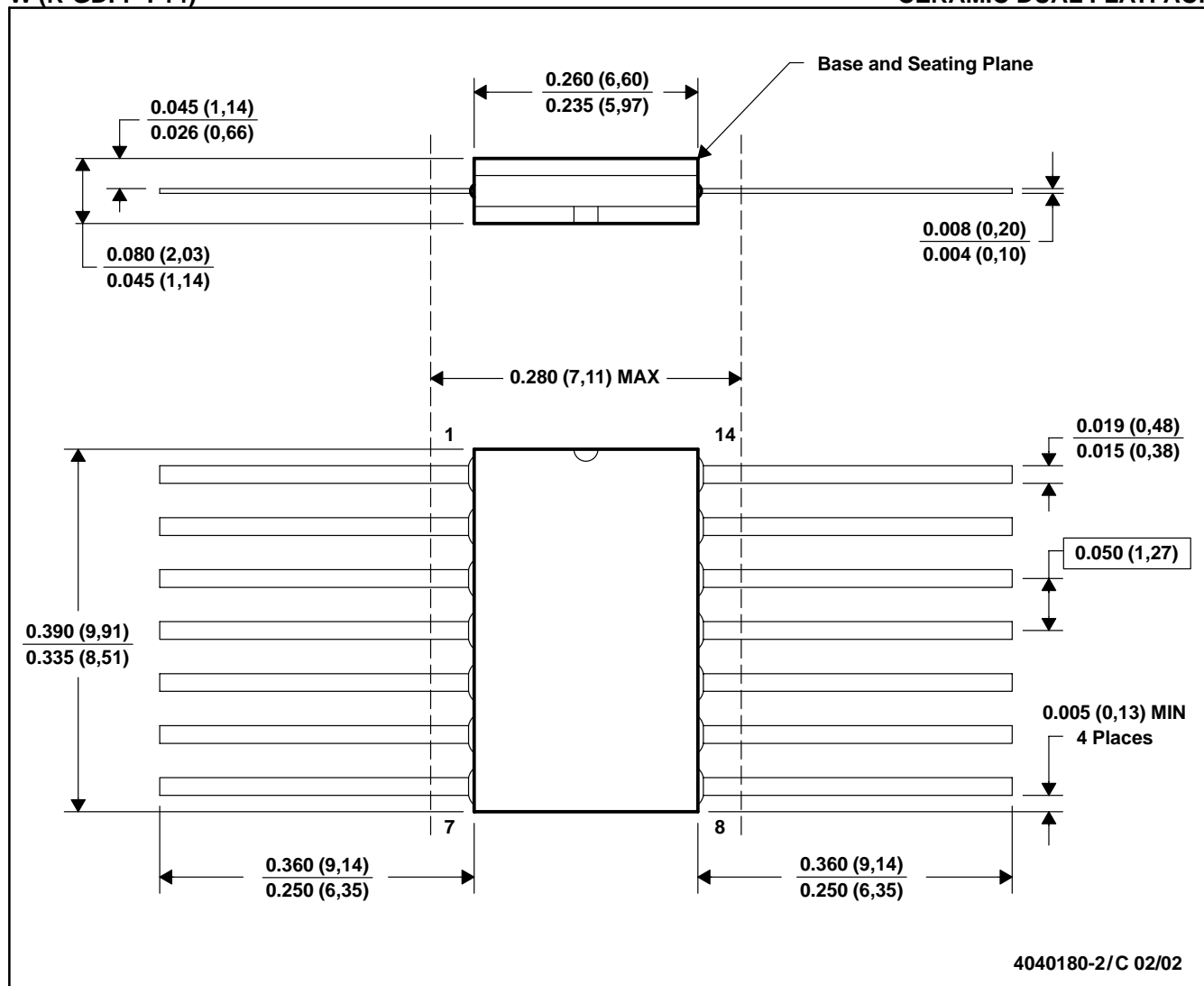$\frac{0.014\ (0,36)}{0.008\ (0,20)}$

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
             B.   This drawing is subject to change without notice.
             C.   This package is hermetically sealed with a ceramic lid using glass frit.
             D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
             E.   Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

W (R-GDFP-F14)   **CERAMIC DUAL FLATPACK**

Base and Seating Plane

0.045 (1,14) / 0.026 (0,66)

0.260 (6,60) / 0.235 (5,97)

0.080 (2,03) / 0.045 (1,14)

0.008 (0,20) / 0.004 (0,10)

0.280 (7,11) MAX

0.019 (0,48) / 0.015 (0,38)

0.050 (1,27)

0.390 (9,91) / 0.335 (8,51)

0.005 (0,13) MIN 4 Places

1   14

7   8

0.360 (9,14) / 0.250 (6,35)

0.360 (9,14) / 0.250 (6,35)

4040180-2 / C 02/02
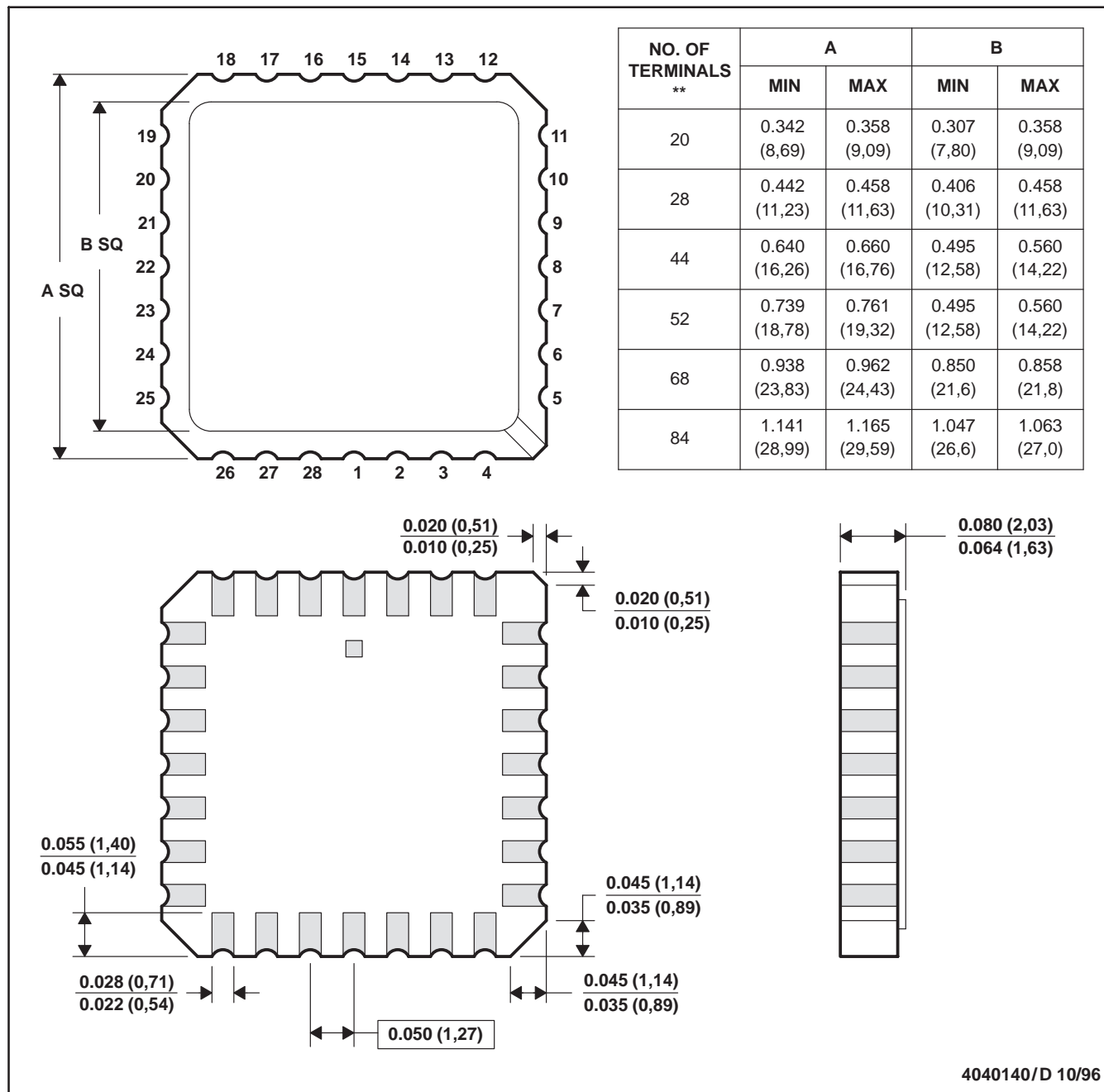
NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package can be hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only.
         E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)   **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN

| NO. OF TERMINALS **	A		B	
	MIN	**MAX**	**MIN**	**MAX**
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package can be hermetically sealed with a metal lid.
         D. The terminals are gold plated.
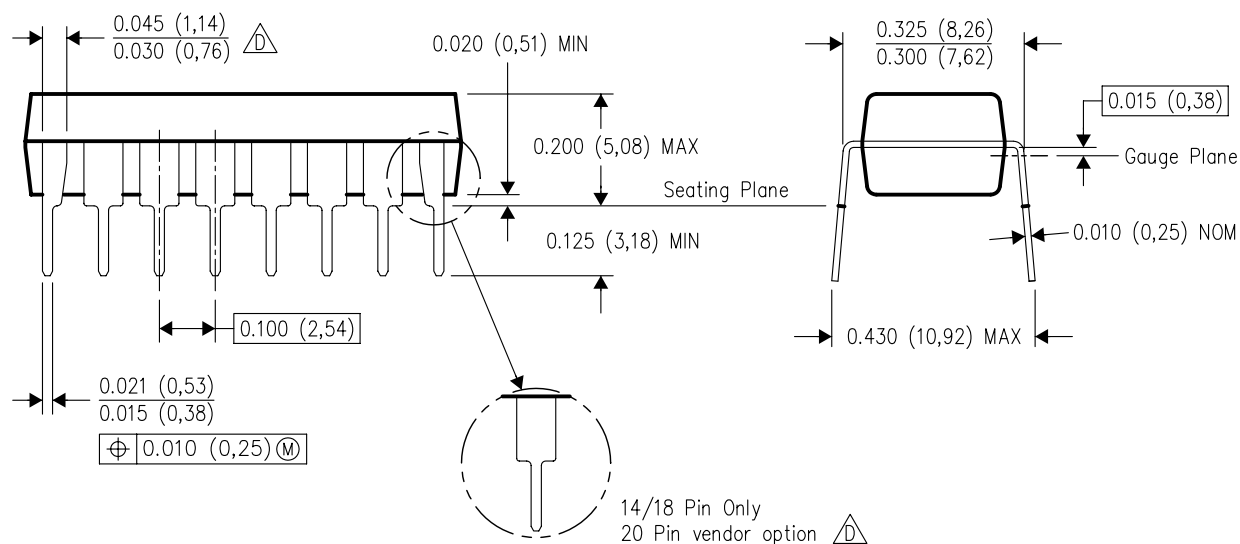   E. Falls within JEDEC MS-004

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N (R−PDIP−T**)
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE
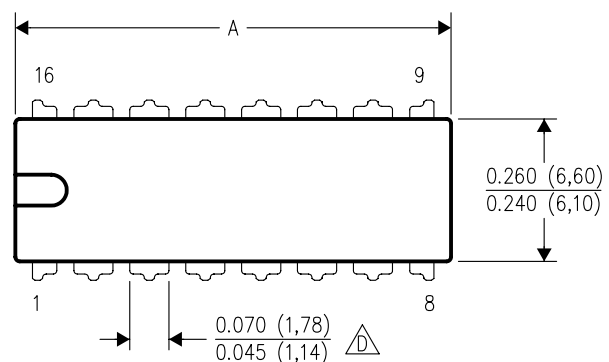
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14) D

0.045 (1,14)
0.030 (0,76) D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) M

14/18 Pin Only
20 Pin vendor option D

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX
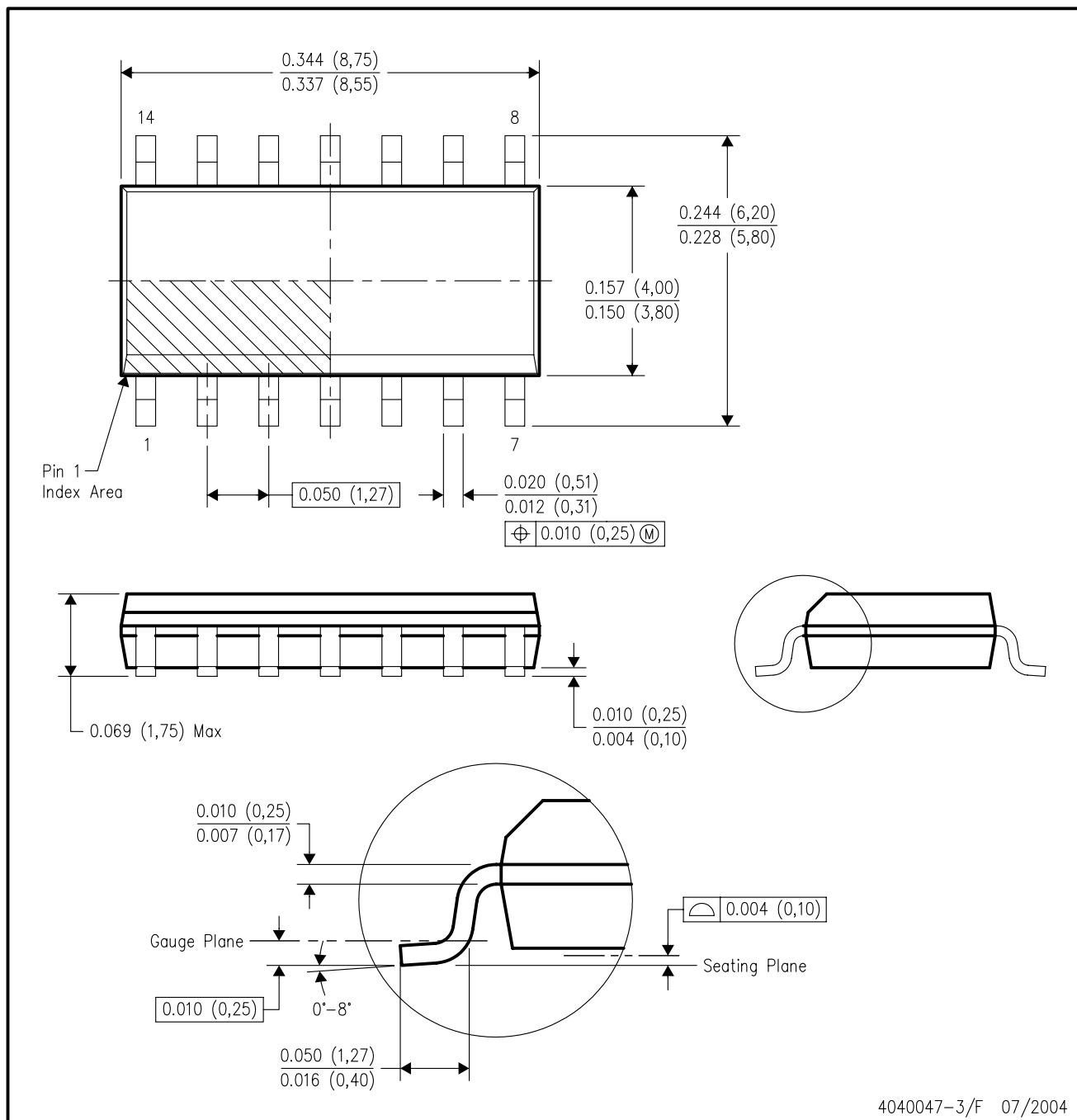
4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
        D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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D (R−PDSO−G14)   PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

14

8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1

7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/F   07/2004

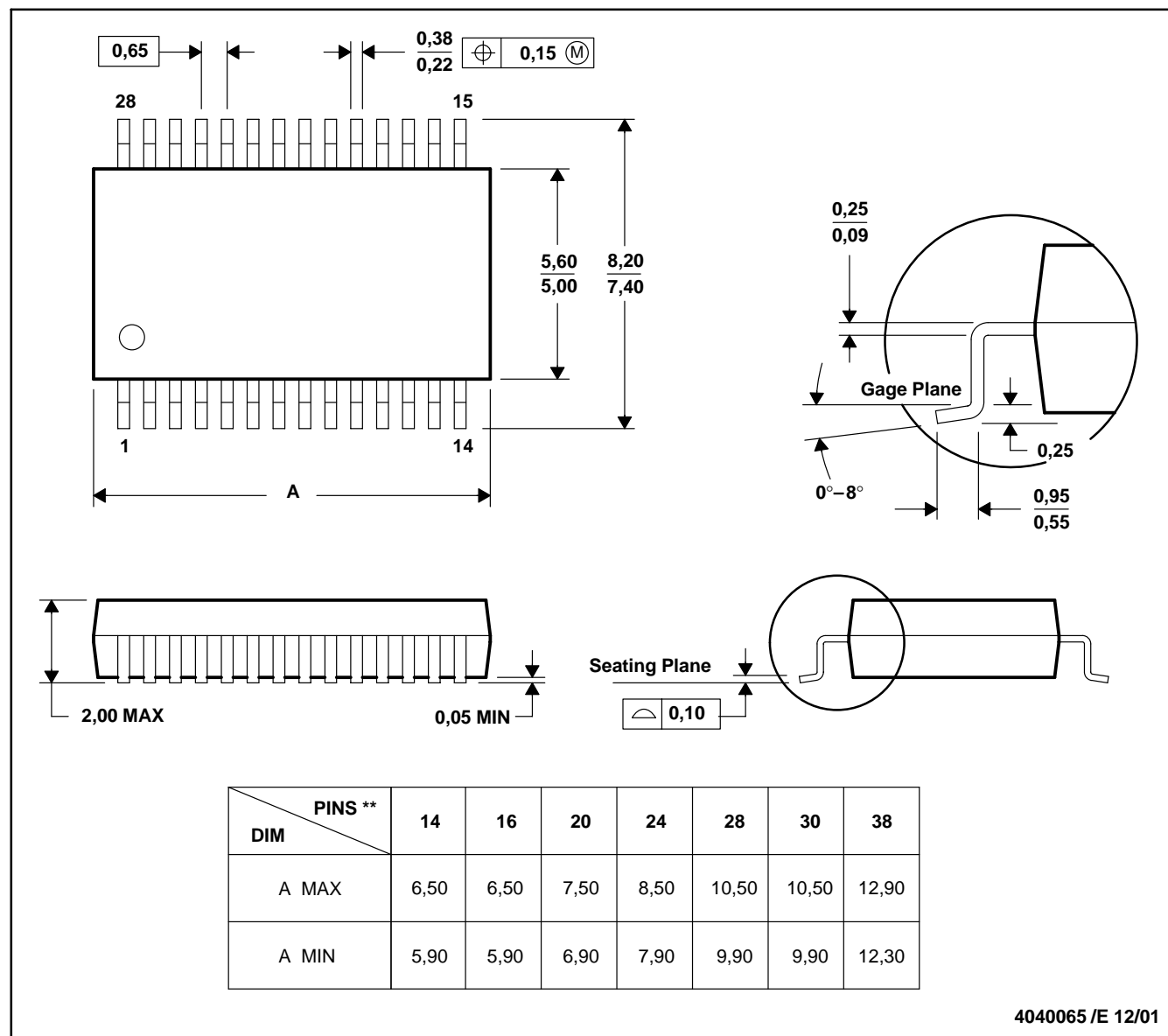NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−012 variation AB.

NS (R-PDSO-G**)   PLASTIC SMALL-OUTLINE PACKAGE
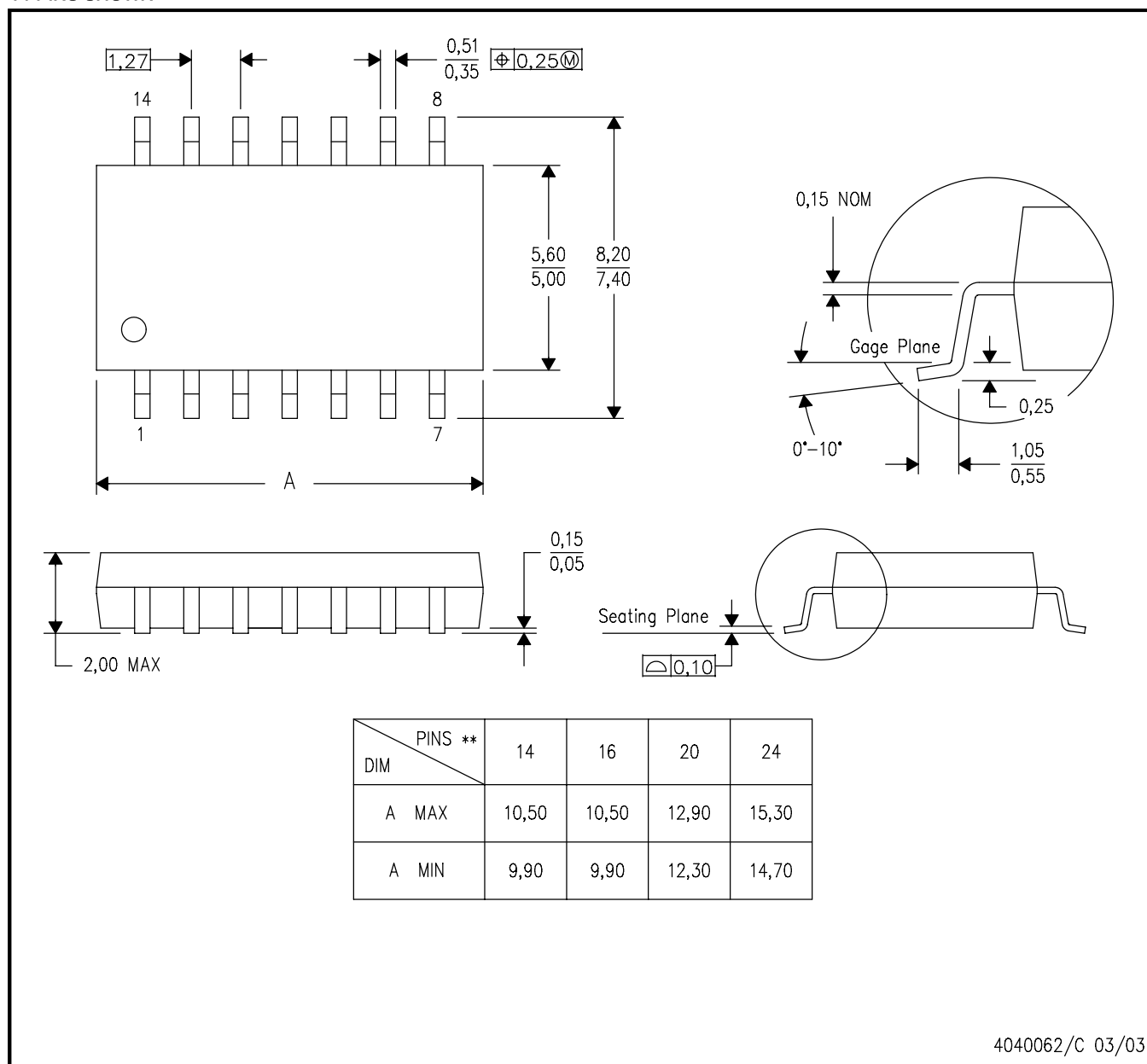
14-PINS SHOWN

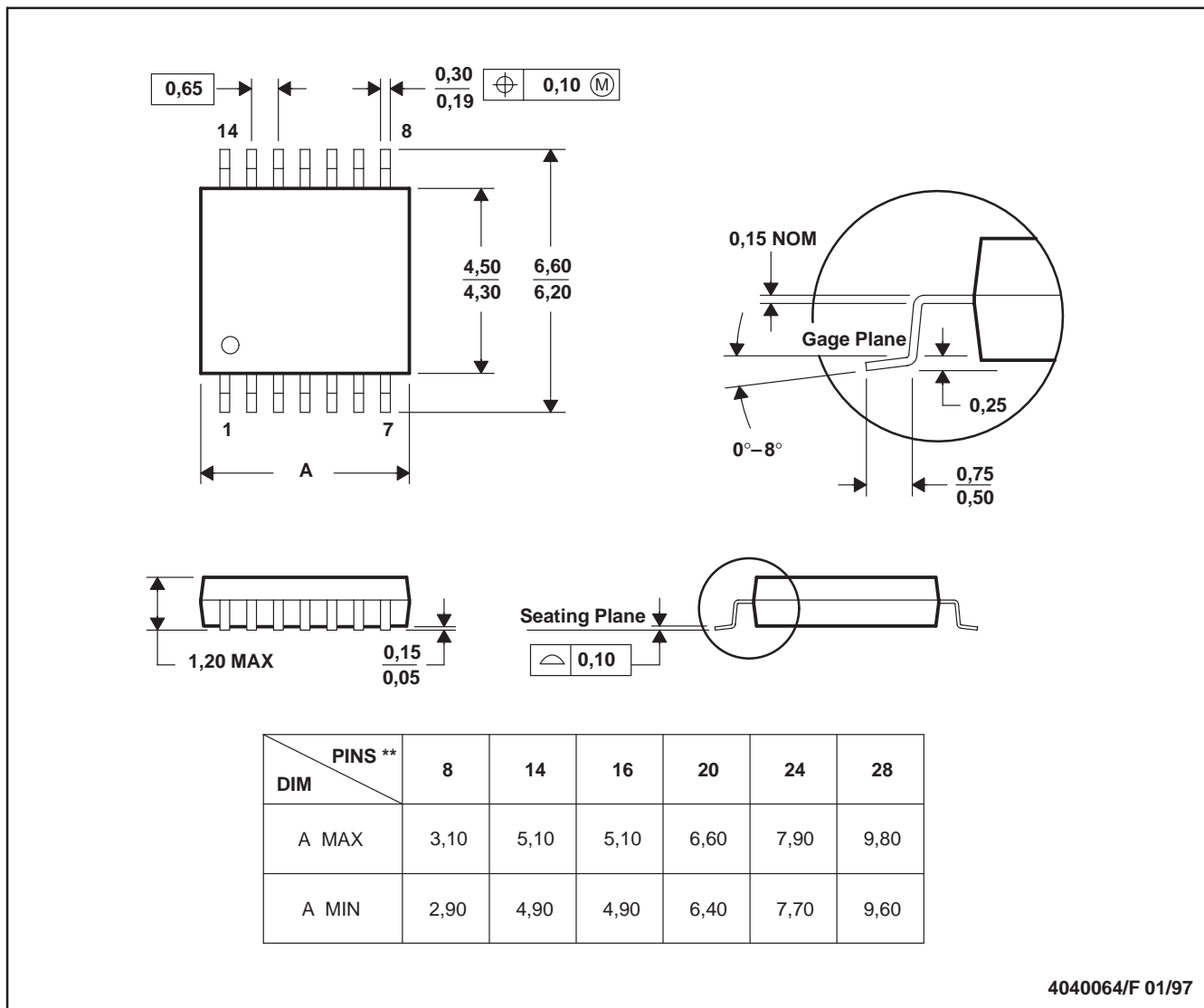| DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)　　　　　　　　　　　　　　　　　　　　　　　　**PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
　　　　B. This drawing is subject to change without notice.
　　　　C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
　　　　D. Falls within JEDEC MO-150

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PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

	PINS **	8	14	16	20	24	28
DIM							
A MAX		3,10	5,10	5,10	6,60	7,90	9,80
A MIN		2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
  B. This drawing is subject to change without notice.
  C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  D. Falls within JEDEC MO-153

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