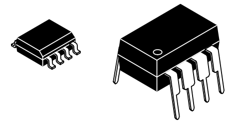


SLUS274A – JANUARY 1999 – REVISED APRIL 2003

NEGATIVE VOLTAGE HOT SWAP POWER MANAGER

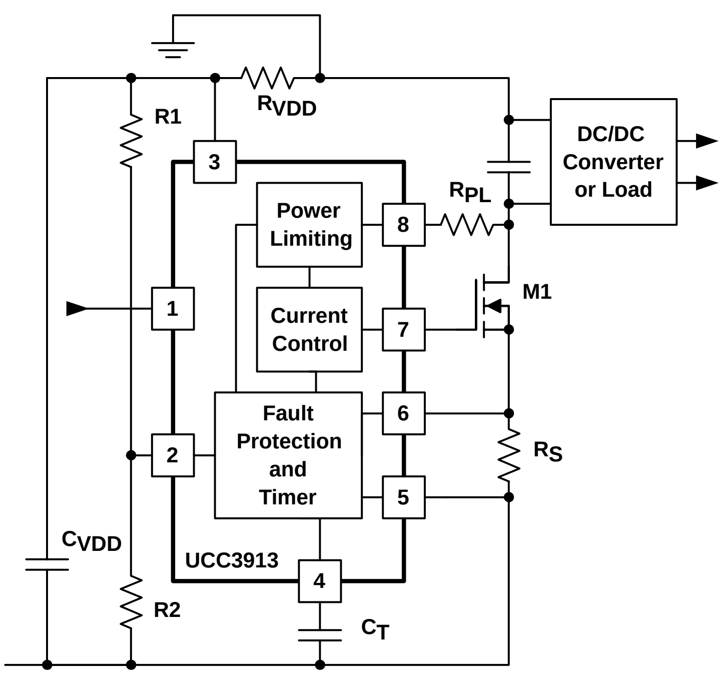
FEATURES

- **Precision Fault Threshold**
- **Programmable Average Power Limiting**
- **Programmable Linear Current Control**
- **Programmable Overcurrent Limit**
- **Programmable Fault Time**
- **Fault Output Indicator**
- **Shutdown Control**
- **Undervoltage Lockout**
- **8-Pin SOIC**

APPLICATIONS

- **–48-V Distributed Power Systems**
- **Central Office Switching**
- **Wireless Base Stations**

SIMPLIFIED APPLICATION DIAGRAM



DESCRIPTION

The UCCx913 family of negative voltage circuit breakers provides complete power management, hot-swap, and fault handling capability. The device is referenced to the negative input voltage and is driven through an external resistor connected to ground, which is essentially a current drive as opposed to the traditional voltage drive. The on-board 10-V shunt regulator protects the device from excess voltage and serves as a reference for programming the maximum allowable output sourcing current during a fault. In the event of a constant fault, the internal timer limits the on-time from less than 0.1% to a maximum of 3%. The duty cycle modulates depending on the current into the PL pin, which is a function of the voltage across the FET, and limits average power dissipation in the FET. The fault level is fixed at 50 mV across the current-sense resistor to minimize total dropout. The fault current level is set with an external current sense resistor. The maximum allowable sourcing current is programmed with a voltage divider from VDD to generate a fixed voltage on the IMAX pin. The current level, when the output appears as a current source, is equal to V_{IMAX}/R_{SENSE}. If desired, a controlled current startup can be programmed with a capacitor on the IMAX pin.

When the output current is below the fault level, the output device is switched on. When the output current exceeds the fault level, but is less than the maximum sourcing level programmed by the IMAX pin, the output remains switched on, and the fault timer starts charging CT. Once CT charges to 2.5 V, the output device is turned off and performs a retry some time later. When the output current reaches the maximum sourcing current level, the output appears as a current source, limiting the output current to the set value defined by IMAX.

Other features of the UCCx913 family include undervoltage lockout, and 8-pin small outline (SOIC) and dual-in-line (DIP) packages.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE(1)	PART NUMBER
–40°C to 85°C	PDIP (N)	UCC2913N
	SOIC (D)	UCC2913D
–0°C to 70°C	PDIP (N)	UCC3913N
	SOIC (D)	UCC3913D

(1) The N and D packaged are also available taped and reeled. Add an R suffix to the device type (i.e., UCC2913NR).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

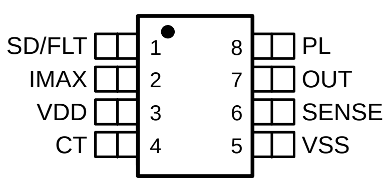
		UCC2923 UCC3913	UNIT
Input voltage	IMAX	limited to VDD	V
Input current	VDD	50	mA
	SHUTDOWN	10	
	PL	10	
Operating junction temperature range, T_J		–55 to 150	°C
Storage temperature, T_{stg}		–65 to 150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to VSS (the most negative voltage). All currents are positive into and negative out of the specified terminal.

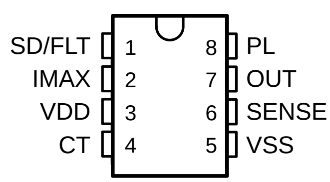
RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input current, I_{VDD}	2	5	20	mA

D PACKAGE
(TOP VIEW)



N PACKAGE
(TOP VIEW)



ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C for UCC2913, T_A = 0°C to 70°C for UCC3913, T_J = T_A, I_{VDD} = 2 mA, CT = 4.7 pF, T_A = T_J (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY					
Minimum input current, VDD			1	2	mA
Regulator voltage	2 mA≤ I_{SOURCE} ≤ 10 mA	8.5	9.5	10.5	V
Undervoltage lockout off-voltage		6	7	8	V
FAULT TIMING					
Overcurrent threshold voltage	T_J = 25 °C	47.5	50.0	53.0	mV
	Over temperature	46.0	50.0	53.5	mV
Overcurrent input bias			50	500	nA
Timing capacitance charge current	V_{CT} = 1.0 V, I_{PL} = 0 A	–22	–36	–50	µA
	Overload condition, V_{SENSE} – V_{IMAX} = 300 mV	–0.7	–1.2	–1.7	mA
Timing capacitance discharge current	V_{CT} = 1.0 V, I_{PL} = 0 A	0.6	1.0	1.5	µA
Timing capacitance fault threshold voltage		2.2	2.4	2.6	V
Timing capacitance reset threshold voltage		0.32	0.50	0.62	V
Output duty cycle	Fault condition, I_{PL} = 0 A	1.7%	2.7%	3.7%	
OUTPUT					
High-level output voltage	I_{OUT} = 0 A	8.5	10		V
	I_{OUT} = –1 A	6	8		V
Low-level output voltage	I_{OUT} = 0 A, V_{SENSE} – V_{IMAX} = 100mV			0.01	V
	I_{OUT} = 2 A, V_{SENSE} – V_{IMAX} = 100mV		0.2	0.6	V
LINEAR AMPLIFIER					
Sense control voltage	V_{IMAX} = 100 mV	85	100	115	mV
	V_{IMAX} = 400 mV	370	400	430	mV
Input bias			50	500	nA
SHUTDOWN/FAULT					
Shutdown threshold voltage		1.4	1.7	2.0	V
Input current	$V_{SD/FLT}$ = 5 V	15	25	45	µA
High-level output voltage		6.0	7.5	9.0	V
Low-level output voltage				0.01	V
Delay-to-output time			150	300	ns
POWER LIMITING					
PL regulator voltage	I_{PL} = 64 µA	4.35	4.85	5.35	V
Duty cycle control	I_{PL} = 64 µA	0.6%	1.2%	1.7%	
	I_{PL} = 1 mA	0.045%	0.1%	0.17%	
OVERLOAD					
Delay-to-output time			300	500	ns
Output sink current	V_{SENSE} – V_{IMAX} = 300mV	40	100		mA
Overload threshold voltage	Relataive to I_{IMAX}	140	200	260	mV

TERMINAL FUNCTIONS

TERMINAL NAME	NO.	I/O	DESCRIPTION
CT	4	I	A capacitor is connected to this pin in order to set the maximum fault time.
IMAX	2	I	This pin programs the maximum allowable sourcing current.
OUT	7	O	Output drive to the MOSFET pass element.
PL	8	I	This feature ensures that the average MOSFET power dissipation is controlled.
SENSE	6	I	Input voltage from the current sense resistor.
SD/FLT	1	O	This pin provides fault output indication and shutdown control.
VDD	3	O	Current driven with a resistor to a voltage at least 10V more positive than VSS.
VSS	5	O	Ground reference for the device and the most negative voltage available.

DETAILED PIN DESCRIPTIONS

CT

A capacitor connected to this pin allows setting of the maximum fault time. The maximum fault time must be more than the time to charge external load capacitance. The maximum fault time is defined as:

$$t_{FAULT} = \frac{\left(2 \times C_T\right)}{I_{CH}} \tag{1}$$

where

$$I_{CH} = 36\ \mu A + I_{PL} \tag{2}$$

and I_{PL} is the current into the power limit pin. Once the fault time is reached the output shuts down for a time given by:

$$t_{SD} = 2 \times 10^6 \times C_T \tag{3}$$

IMAX

This pin programs the maximum allowable sourcing current. Since V_{DD} is a regulated voltage, a voltage divider can be derived from V_{DD} to generate the program level for the IMAX pin. The current level at which the output appears as a current source is equal to the voltage on the IMAX pin over the current sense resistor. If desired, a controlled current startup can be programmed with a capacitor on the IMAX pin, and a programmed start delay can be achieved by driving the shutdown with an open collector/drain device into an R-C network.

PL

This pin's feature ensures that the average MOSFET power dissipation is controlled. A resistor is connected from this pin to the drain of the N-channel MOSFET pass element. When the voltage across the N-channel MOSFET exceeds 5 V, current flows into the PL pin which adds to the fault timer charge current, reducing the duty cycle from the 3% level. When I_{PL} is much greater 36 μA, then the average MOSFET power dissipation is given by:

$$P_{FET(avg)} = IMAX \times 1 \times 10^{-6} \times R_{PL} \tag{4}$$

SENSE

Input voltage from the current sense resistor. When there is greater than 50 mV across this pin with respect to VSS, a fault is sensed, and C_T starts to charge.

DETAILED PIN DESCRIPTIONS (continued)

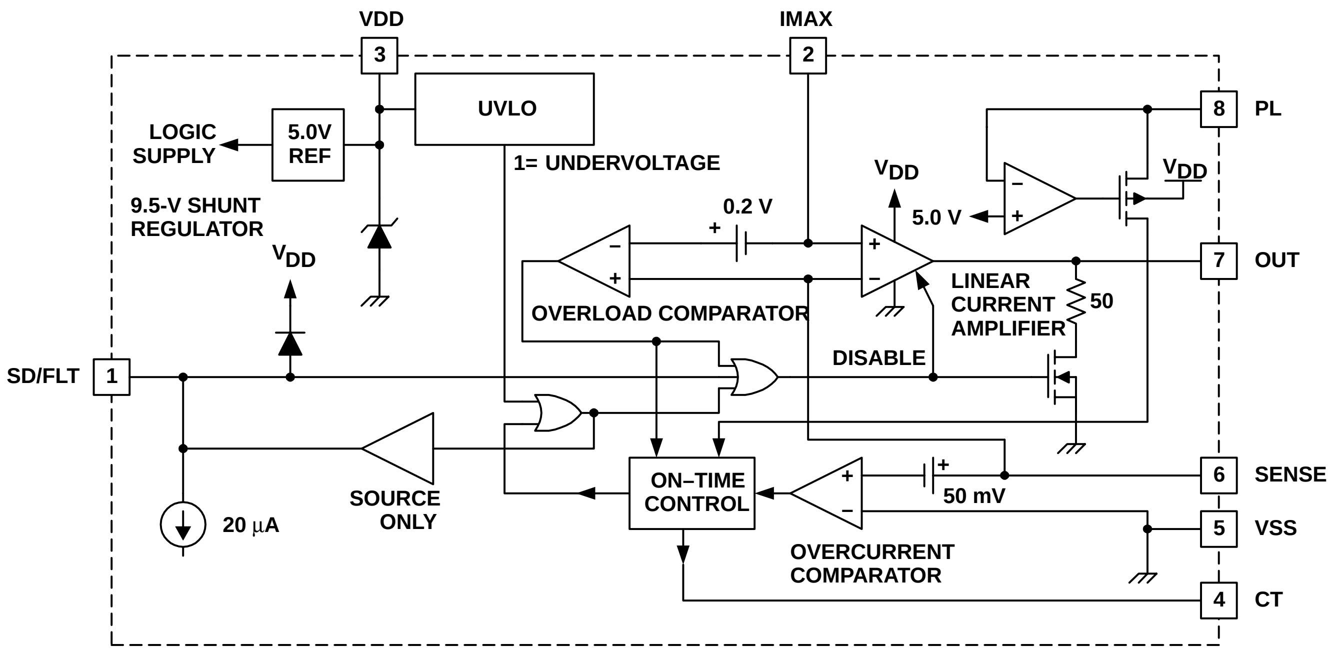
SD/FLT

This pin provides fault output indication and shutdown control. Interface into and out of this pin is usually performed through level shift transistors. When 20 µA is sourced into this pin, shutdown drives high causing the output to disable the N-channel MOSFET pass device. When opened, and under a non-fault condition, the SD/FLT pin pulls to a low state. When a fault is detected by the fault timer, or undervoltage lockout, this pin drives to a high state, indicating the output MOSFET is off.

VDD

Current driven with a resistor to a voltage at least 10-V more positive than VSS. Typically a resistor is connected to ground. The 10-V shunt regulator clamps VDD at 10 V above the VSS pin, and is also used as an output reference to program the maximum allowable sourcing current.

BLOCK DIAGRAM



UDG–99001

APPLICATION INFORMATION

Typical Fault Mode

Figure 1 shows the detailed circuitry for the fault timing function of the UCCx913. This initial discussion of the typical fault mode ignores the overload comparator, and current source I3. Once the voltage across the current sense resistor, R_S, exceeds 50 mV, a fault has occurred. This causes the timing capacitor to charge with a combination of 36 µA plus the current from the power limiting amplifier. The PL amplifier is designed to source current into the CT pin only and to begin sourcing current once the voltage across the output FET exceeds 5 V. The current I_{PL} is related to the voltage across the FET with the following expression:

$$I_{PL} = \frac{V_{FET} - 5\ V}{R_{PL}} \qquad (5)$$

where V_{FET} is the voltage across the N-channel MOSFET pass device.

(How this feature limits average power dissipation in the pass device is described in further detail in the following sections). Note that under a condition where the output current is more than the fault level, but less than the maximum level, $V_{OUT} \approx V_{SS}$ (input voltage), I_{PL} = 0, the C_T charging current is 36 µA.

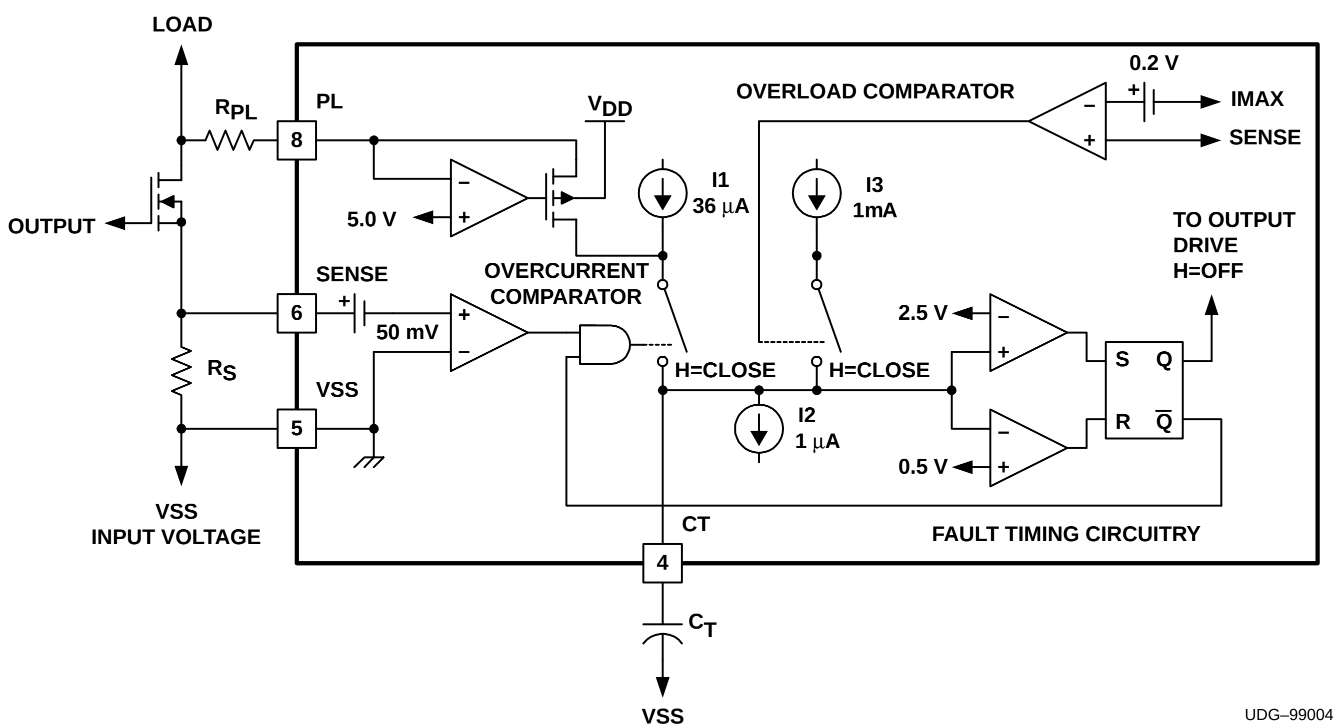


Figure 1. Fault Timing Circuitry Including Power Limit and Overload Comparator

APPLICATION INFORMATION

During a fault, C_T charges at a rate determined by the internal charging current and the external timing capacitor. Once C_T charges to 2.5 V, the fault comparator switches and sets the fault latch. Setting of the fault latch causes both the output to switch off and the charging switch to open. C_T must now discharge with the 1-µA current source, I2, until 0.5 V is reached. Once the voltage at CT reaches 0.5 V, the fault latch resets, which re-enables the output and allows the fault circuitry to regain control of the charging switch. If a fault is still present, the fault comparator closes the charging switch causing the cycle to begin. Under a constant fault, the duty cycle is given by:

$$\text{Duty Cycle} = \frac{1\ \mu A}{I_{PL} + 36\ \mu A} \tag{6}$$

Average power dissipation in the pass element is given by:

$$P_{FET(avg)} = V_{FET} \times IMAX \times \left(\frac{1\ \mu A}{I_{PL} + 36\ \mu A}\right) \tag{7}$$

Where VFET >> 5 V I_{PL} can be approximated as :

$$I_{PL} \cong \frac{V_{FET}}{R_{PL}} \tag{8}$$

and where I_{PL} >> 36 µA, the duty cycle can be approximated as :

$$\text{Duty Cycle} = \frac{1\ \mu A \times R_{PL}}{V_{FET}} \tag{9}$$

Therefore, the maximum average power dissipation in the MOSFET can be approximated by:

$$P_{FET(avg)} = V_{FET} \times IMAX \times \left(\frac{1\ \mu A \times R_{PL}}{V_{FET}}\right) = IMAX \times 1\ \mu A \times R_{PL} \tag{10}$$

Notice that in the approximation, V_{FET} cancels. therefore, average power dissipation is limited in the N-channel MOSFET pass element.

Overload Comparator

The linear amplifier in the UCCx913 ensures that the output N-channel MOSFET does not pass more than I_{MAX} (which is V_{IMAX}/R_S). In the event the output current exceeds the programmed IMAX by 0.2 V/R_S (which can only occur if the output MOSFET is not responding to a command from the device) the CT pin begins charging with I3, 1 mA, and continue to charge to approximately 8 V. This allows a constant fault to show up on the SD/FLT pin, and also since the voltage on CT charges past 2.5 V only in an overload fault mode, it can be used for detection of output FET failure or to build in redundancy in the system.

APPLICATION INFORMATION

Determining External Component Values (See FIgure 2)

To set R_{VDD} the following must be achieved:

$$\frac{V_{IN(min)}}{R_{VDD}} > \frac{10\ V}{(R1 + R2)} + 2\ mA \tag{11}$$

In order to estimate the minimum timing capacitor, C_T, several things must be taken into account. For example, given the schematic below as a possible (and at this point, a standard) application, certain external component values must be known in order to estimate $C_{T(min)}$.

Then use the given the values of C_{OUT}, Load, R_{SENSE}, VSS, and the resistors determining the voltage on the IMAX pin, to calculate the approximate startup time of the node V_{OUT}. This startup time must be faster than the time it takes for CT to charge to 2.5 V (relative to VSS), and is the basis for estimating the minimum value of CT. In order to determine the value of the sense resistor, R_{SENSE}, assuming the user has determined the fault current, R_{SENSE} can be calculated by:

$$R_{SENSE} = \frac{50\ mV}{I_{FAULT}} \tag{12}$$

Next, calculate the variable I_{MAX}. I_{MAX} is the maximum current that the device allows through the transistor, M1, and during startup with an output capacitor the power MOSFET, M1, can be modeled as a constant current source of value I_{MAX} where:

$$I_{MAX} = \frac{V_{IMAX}}{R_{SENSE}} \tag{13}$$

where V_{IMAX} = voltage on IMAX pin.

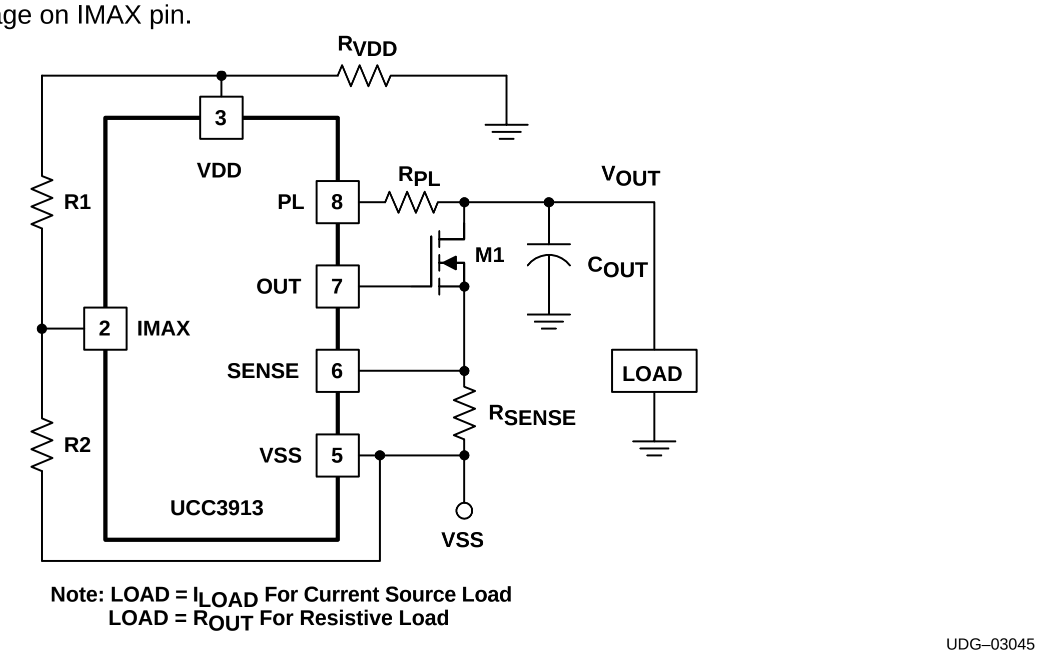
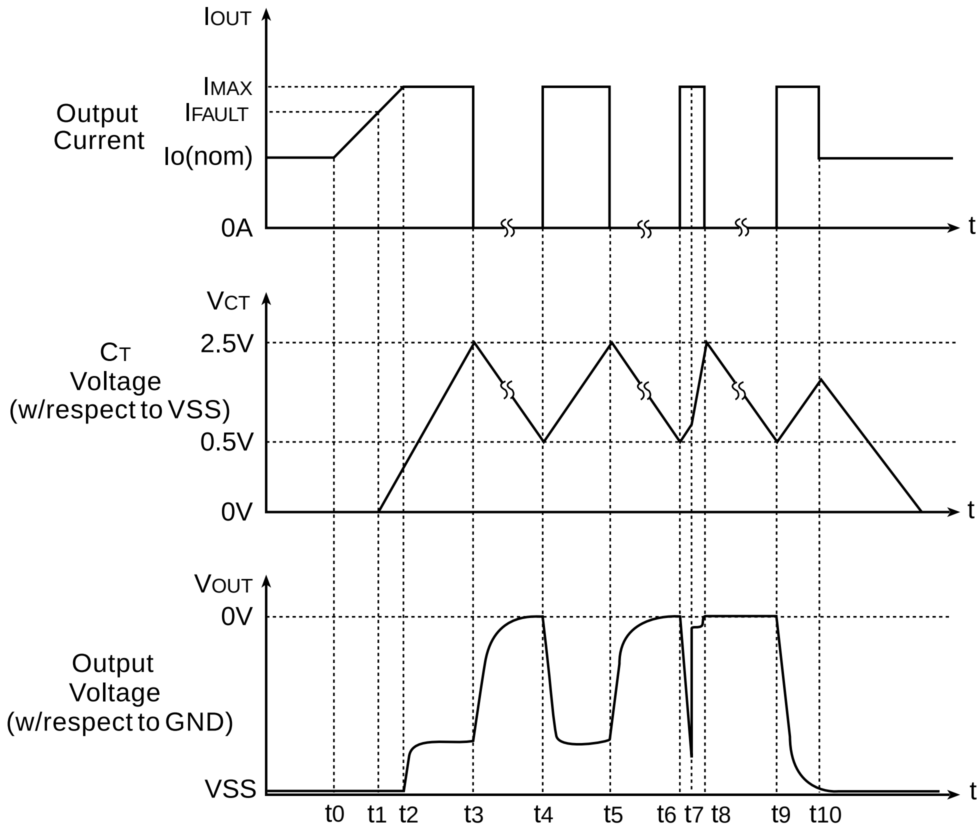


Figure 2. External Component Connections

APPLICATION INFORMATION

TIMING DIAGRAM



TIME	DESCRIPTION
t0	Safe condition. Output current is nominal, output voltage is at the negative rail, VSS.
t1	Fault control reached. Output current reaches the programmed fault value. CT begins to charge at approximately 36-µA.
t2	Maximum current reached. Output current reaches the programmed maximum level and becomes a constant current with value IMAX.
t3	Fault occurs. CT has charged to 2.5V. Fault output goes high. The FET turns off allowing no output current to flow. VOUT floats up to ground.
t4	Retry. CT has discharged to 0.5 V, but fault current is still exceeded, CT begins charging again, FET is on, V_{OUT} pulled down to VSS.
t5	t5 = t3. Illustrates 3% duty cycle.
t6	t6 = t4
t7	Output short circuit. If V_{OUT} is short circuited to ground, CT charges at a higher rate depending upon the values for VSS and R_{PL}.
t8	Fault occurs. Output is still short circuited, but the occurrence of a fault turns the FET off so no current is conducted.
t9	t9 = t4. Output short circuit released, still in fault mode.
t10	t10 = t0. Fault released. Safe condition. Return to normal operaton of the circuit breaker.

APPLICATION INFORMATION

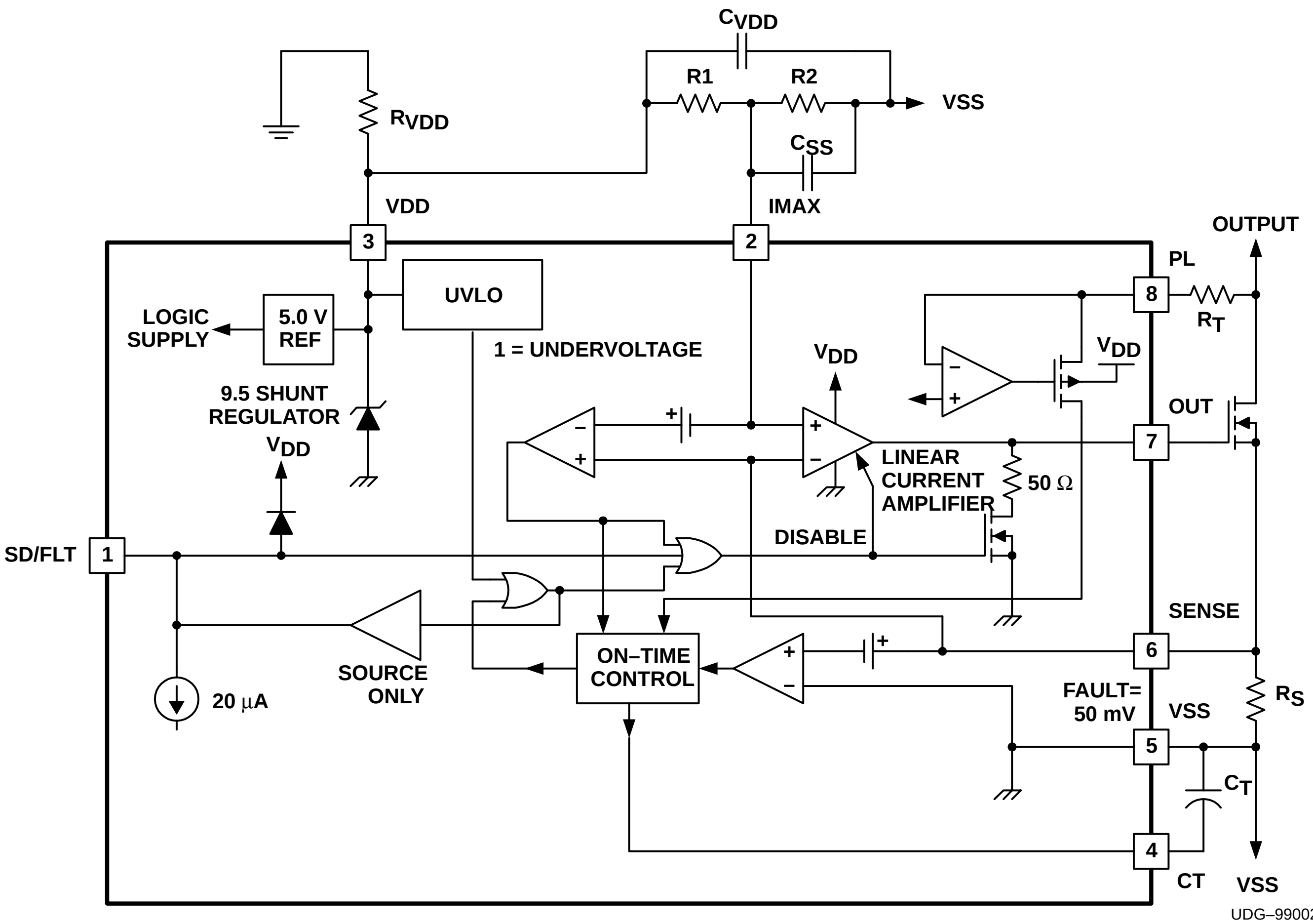


Figure 3. Typical Application Diagram

To calculate the startup time using the current source load.

$$t_{START} = \frac{C_{OUT} \times |VSS|}{I_{MAX} - I_{LOAD}} \tag{14}$$

To calculate the startup time using the resistive load.

$$t_{START} = C_{OUT} \times R_{OUT} \times \ln\left(\frac{I_{MAX} \times R_{OUT}}{I_{MAX} \times R_{OUT} - |VSS|}\right) \tag{15}$$

APPLICATION INFORMATION

Once t_{START} is calculated, the power limit feature of the UCCx913 must be addressed and component values derived. Assuming the designer chooses to limit the maximum allowable average power that is associated with the circuit breaker, the power limiting resistor, R_{PL}, can be easily determined by the following:

$$R_{PL} = \frac{P_{FET(avg)}}{1\ \mu A \times I_{MAX}} \tag{16}$$

where a minimum R_{PL} exists defined by

$$R_{PL(min)} = \frac{|VSS|}{10mA} \tag{17}$$

Finally, after computing the aforementioned variables, the minimum timing capacitor can be derived for a current source load with the following equation.

$$C_{T(min)} = \frac{t_{START} \times \left(98\ \mu A \times R_{PL} + |VSS| - 10\ V\right)}{4\ V \times R_{PL}} \tag{18}$$

The minimum timing capacitor can be derived for a resistive load with the following equation.

$$C_{T(min)} = \tag{19}$$

$$\frac{t_{START} \times \left(49\ \mu A \times R_{PL} + |VSS| - 5\ V - I_{MAX} \times R_{OUT}\right) + R_{OUT} \times C_{OUT} \times |VSS|}{2\ V \times R_{PL}}$$

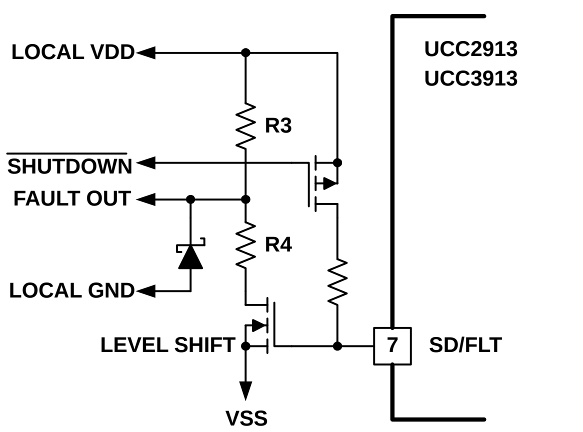


Figure 4. Possible Level Shift Circuitry Interface

AVERAGE POWER DISSIPATION
vs
MOSFET VOLTAGE

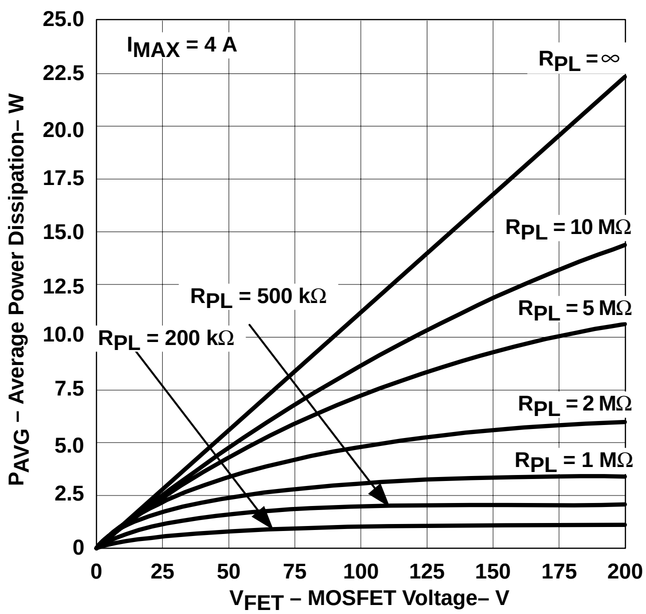
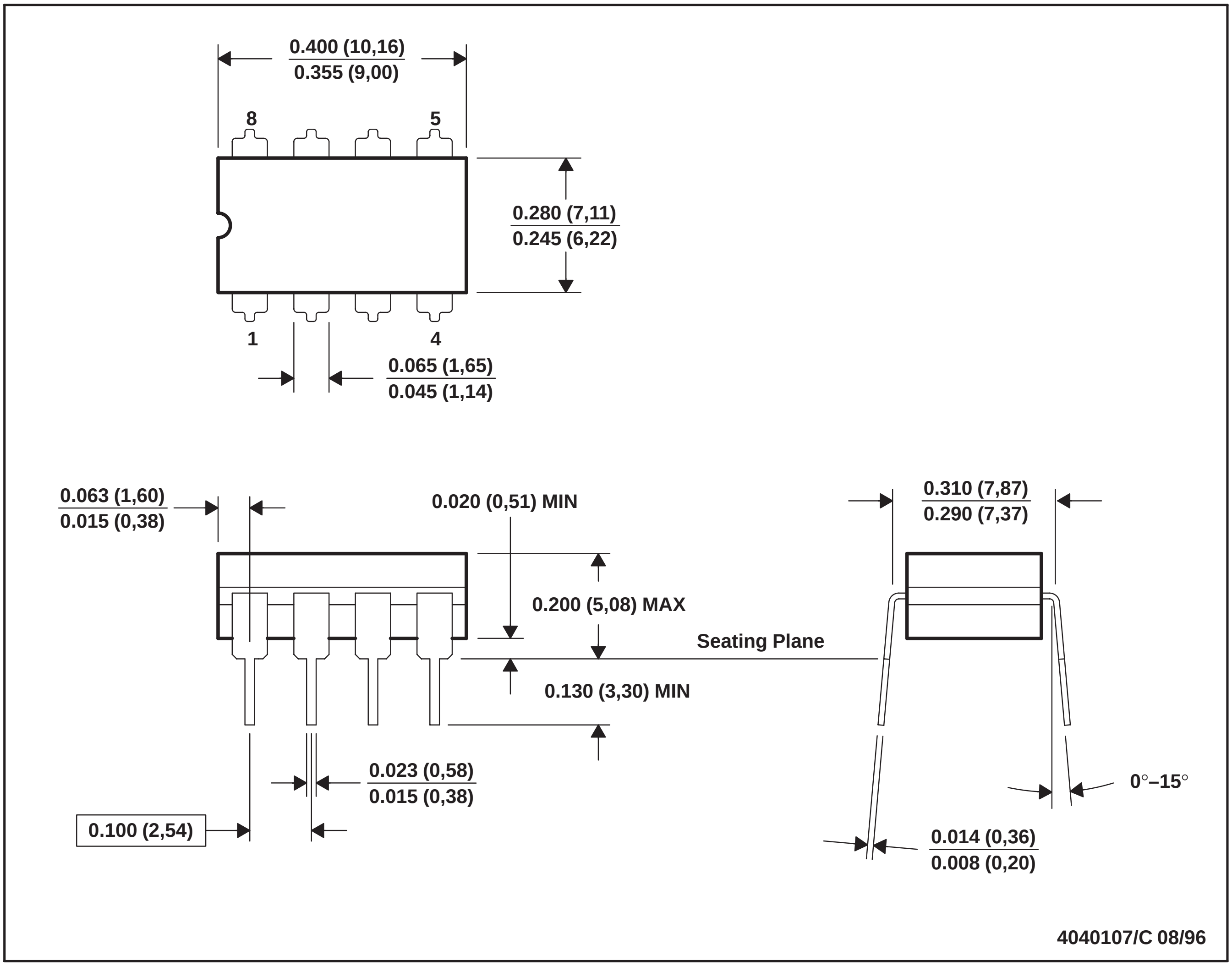


Figure 5

SAFETY RECOMMENDATION

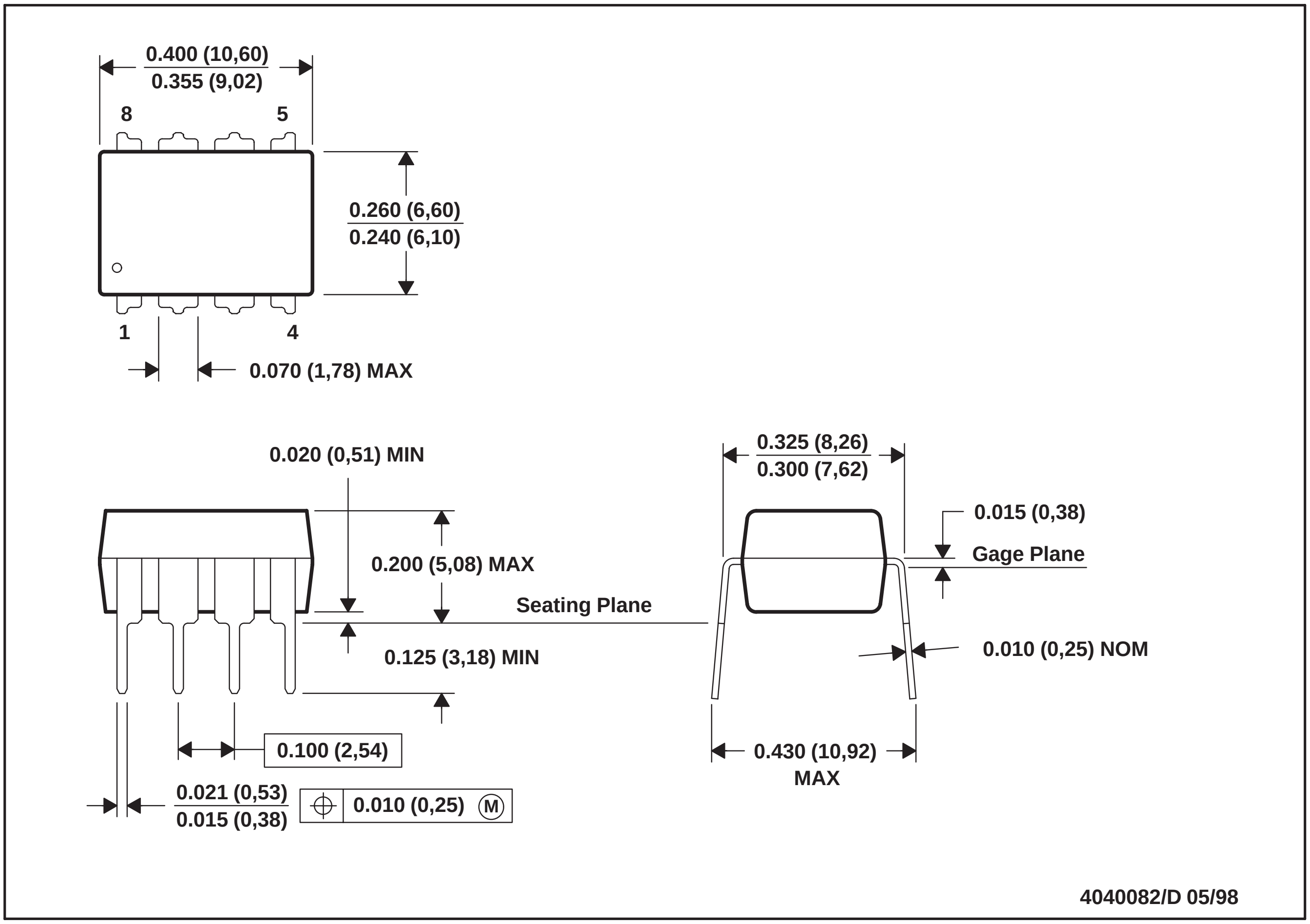
Although the UCC3913 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3913 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3913 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



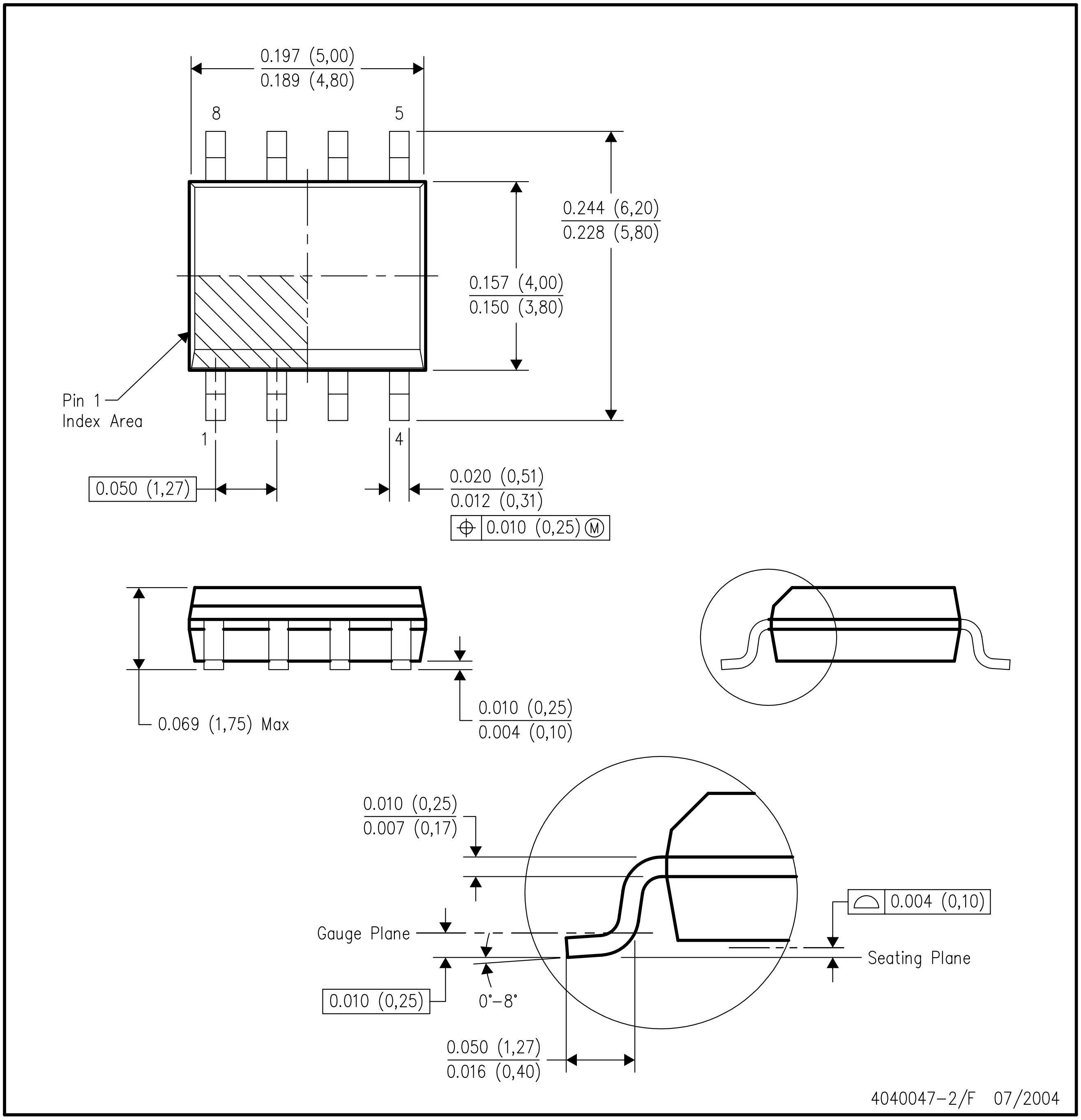
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AA.

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