High-Speed Quad SPST CMOS Analog Switch

FEATURES

- Fast Switching—t_{ON}: 38 ns
- Low On-Resistance: 25 Ω
- Low Leakage: 100 pA
- Low Charge Injection
- TTL/CMOS Logic Compatible
- Single Supply Compatibility
- High Current Rating: –30 mA

BENEFITS

- Faster Throughput
- Higher Accuracy
- Reduced Pedestal Error
- Upgrades Existing Designs
- Simple Interfacing
- Replaces HI201HS, ADG201HS
- Space Savings (TSSOP)

APPLICATIONS

- Data Acquisition
- Hi-Rel Systems
- Sample-and-Hold Circuits
- Communication Systems
- Automatic Test Equipment
- Integrator Reset Circuits
- Choppers
- Gain Switching
- Avionics

DESCRIPTION

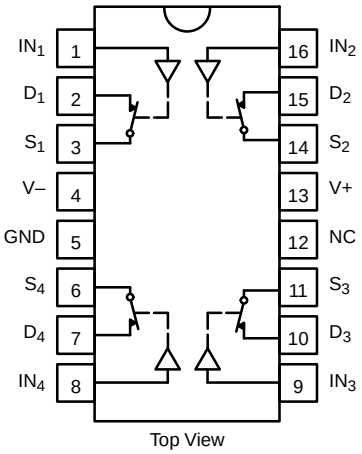
The DG201HS is an improved monolithic device containing four independent analog switches. It is designed to provide high speed, low error switching of analog signals. Combining low on-resistance (25 Ω) with high speed (t_{ON}: 38 ns), the DG201HS is ideally suited for high speed data acquisition requirements.

To achieve high voltage ratings and superior switching performance, the DG201HS is built on a proprietary high-voltage silicon-gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks input voltages to the supply values, when off.

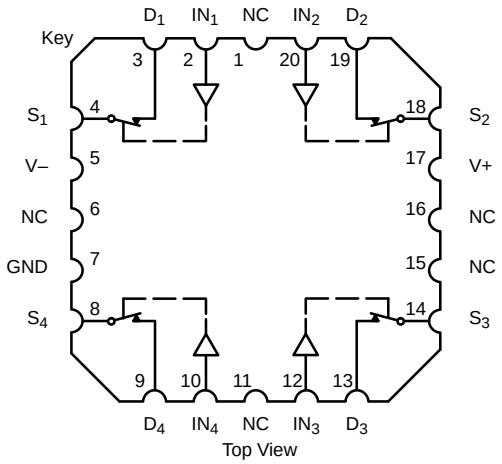
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

Dual-In-Line, SOIC and TSSOP



Top View

LCC



Top View

TRUTH TABLE	
Logic	**Switch**
0	ON
1	OFF

Logic “0” ≤ 0.8 V
Logic “1” ≥ 2.4 V

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
–40 to 85°C	16-Pin Plastic DIP	DG201HSDJ
	16-Pin Narrow SOIC	DG201HSDY
	16-Pin TSSOP	DG201HSDQ
–55 to 125°C	16-Pin CerDIP	DG201HSAK/883
	LCC-20	DG201HSAZ/883

ABSOLUTE MAXIMUM RATINGS

V+ to V– . . . . . 44 V
GND to V– . . . . . 25 V
Digital Inputs[a] V_S, V_D . . . . . (V–) –4 V to (V+) +4 V
or 30 mA, whichever occurs first
Continuous Current (Any Terminal) . . . . . 30 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle) . . . . . 100 mA
Storage Temperature (A Suffix) . . . . . –65 to 150°C
(D Suffix) . . . . . –65 to 125°C
Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] . . . . . 470 mW
16-Pin CerDIP[d] . . . . . 900 mW
16-Pin Narrow Body SOIC and TSSOP[e] . . . . . 600 mW
LCC-20[d] . . . . . 900 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6 mW/°C above 75°C.
d. Derate 12 mW/°C above 75°C.
e. Derate 7.6 mW/°C above 75°C.

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

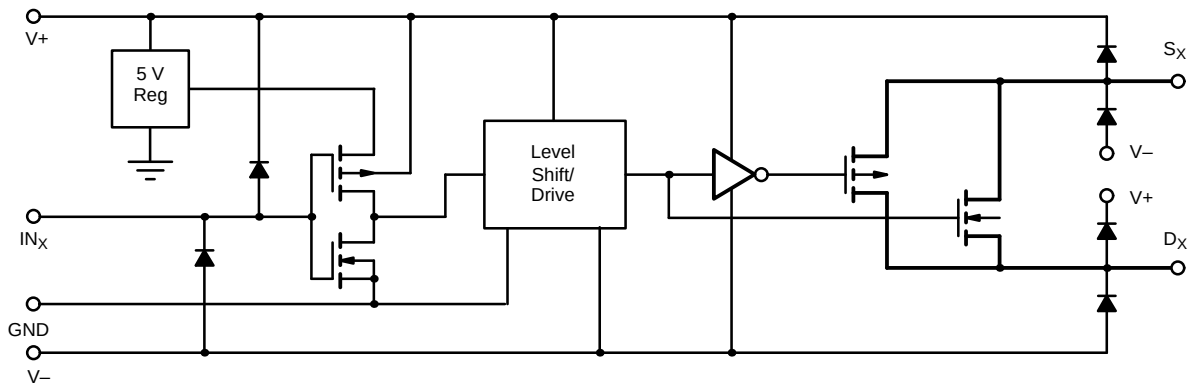


FIGURE 1.

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Specified V+ = 15 V, V– = –15 V V_{IN} = 3 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix –55 to 125°C Min[d]	A Suffix –55 to 125°C Max[d]	D Suffix –40 to 85°C Min[d]	D Suffix –40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		V–	V+	V–	V+	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = –10 mA, V_D = ±8.5 V V+ = 13.5 V, V– = –13.5 V	Room Full	25		50 75		50 75	Ω
$r_{DS(on)}$ Match			Room	3					%
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5 V, V– = –16.5 V V_D = ±15.5 V V_S = ∓15.5 V	Room Full	0.1	–1 –60	1 60	–1 –20	1 20	nA
	$I_{D(off)}$		Room Full	0.1	–1 –60	1 60	–1 –20	1 20	
Channel On Leakage Current	$I_{D(on)}$	V+ = 16.5 V, V– = –16.5 V V_S = V_D = ∓15.5 V	Room Full	0.1	–1 –60	1 60	–1 –20	1 20	
Digital Control									
Input, High Voltage	V_{INH}		Full		2.4		2.4		V
Input, Low Voltage	V_{INL}		Full			0.8		0.8	
Input Capacitance	C_{in}		Full	5					pF
Input Current	I_{INL} or I_{INH}	V_{IN} under test = 0.8 V, 3 V	Full		–1	1	–1	1	µA
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF V_S = ±10 V, V_{INH} = 3 V See Figure 2	Room Full	48		60 75		60 75	ns
Turn-Off Time	t_{OFF1}		Room Full	30		50 70		50 70	
	t_{OFF2}		Room	150					
Output Settling Time to 0.1%	t_s		Room	180					
Charge Injection	Q	C_L = 1 nF, V_S = 0 V V_{gen} = 0 V, R_{gen} = 0 Ω	Room	–5					pC
OFF Isloation	OIRR	R_L = 1 kΩ, C_L = 10 pF f = 100 kHz	Room	85					dB
Crosstalk (Channel-to-Channel)	X_{TALK}	Any Other Channel Switches R_L = 1 kΩ, C_L = 10 pF f = 100 kHz	Room	100					
Source Off Capacitance	$C_{S(off)}$	V_S, V_D = 0 V, f = 1 MHz	Room	8					pF
Drain Off Capacitance	$C_{D(off)}$		Room	8					
Channel On Capacitance	$C_{D(on)}$		Room	30					
Drain-to-Source Capacitance	$C_{DS(off)}$		Room	0.5					
Power Supplies									
Positive Supply Current	I+	V+ = 15 V, V– = –15 V V_{IN} = 0 or 5 V	Room Full	4.5		10		10	mA
Negative Supply Current	I–		Room Full	3.5	–6		–6		
Power Consumption[c]	P_C		Full			240		240	mW

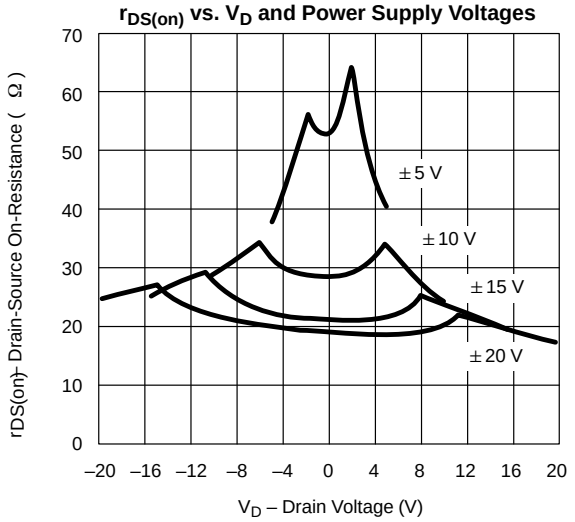
SPECIFICATIONS[a] FOR SINGLE SUPPLY

Parameter	Symbol	Test Conditions Unless Specified V+ = 10.8 V to 16.5 V V– = GND = 0 V V_{IN} = 3 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix –55 to 125°C Min[d]	A Suffix –55 to 125°C Max[d]	D Suffix –40 to 85°C Min[d]	D Suffix –40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	V+	0	V+	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = –10 mA, V_D = 8.5 V V+ = 10.8 V	Room Full	65		90 120		90 120	Ω
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5 V, V_S = 0.5 V, 10 V V_D = 10 V, 0.5 V	Room Full	0.1	–1 –60	1 60	–1 –20	1 20	nA
	$I_{D(off)}$		Room Full	0.1	–1 –60	1 60	–1 –20	1 20	
Channel On Leakage Current	$I_{D(on)}$ + $I_{S(on)}$	V+ = 16.5 V, V_D = 0.5 V, 10 V	Room Full	0.1	–1 –60	1 60	–1 –20	1 20	
Digital Control									
Input, High Voltage	V_{INH}		Full		2.4		2.4		V
Input, Low Voltage	V_{INL}		Full			0.8		0.8	
Input Capacitance	C_{in}		Full	5					pF
Input Current	I_{INL} or I_{INH}	V+ = 16.5 V V_{IN} under test = 0.8 V, 3 V	Full		–1	1	–1	1	µA
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, V_S = 2 V V= 10.8 V, See Figure 2	Room Full			50 70		50 70	ns
Turn-Off Time	t_{OFF1}		Room Full			50 70		50 70	
	t_{OFF2}		Room	150					
Output Settling Time to 0.1%	t_s		Room	180					
Charge Injection	Q	C_L = 1 nF, V_S = 0 V V_{gen} = 0 V, R_{gen} = 0 Ω	Room	10					pC
Off Isloation	OIRR	R_L = 1 kΩ, C_L = 10 pF f = 100 kHz	Room	85					dB
Crosstalk (Channel-to-Channel)	X_{TALK}	Any Other Channel Switches R_L = 1 kΩ, C_L = 10 pF f = 100 kHz	Room	100					
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz	Room	10					pF
Drain Off Capacitance	$C_{D(off)}$		Room	10					
Channel On Capacitance	$C_{D(on)}$	V_{ANALOG} = 0 V	Room	30					
Power Supplies									
Positive Supply Current	I+	V+ = 15 V, V_{IN} = 0 or 5 V	Full			10		10	mA
Power Consumption[c]	P_C		Full			150		150	mW

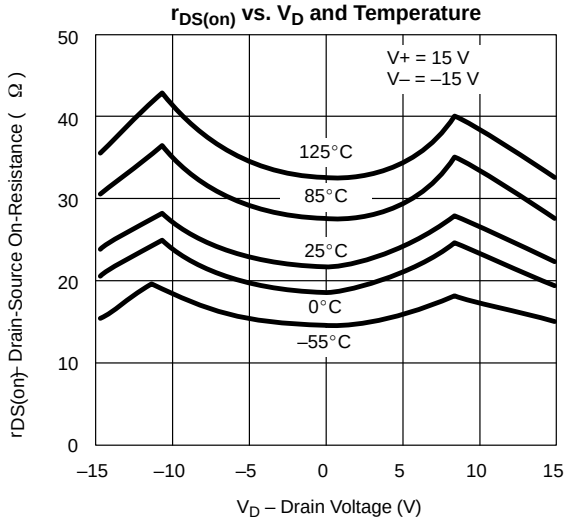
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

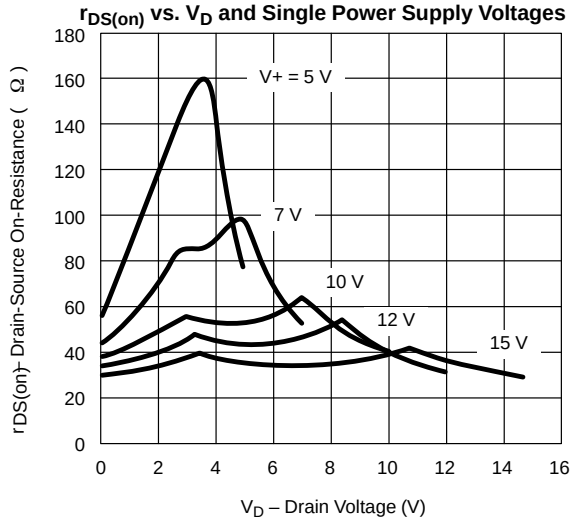
$r_{DS(on)}$ vs. V_D and Power Supply Voltages



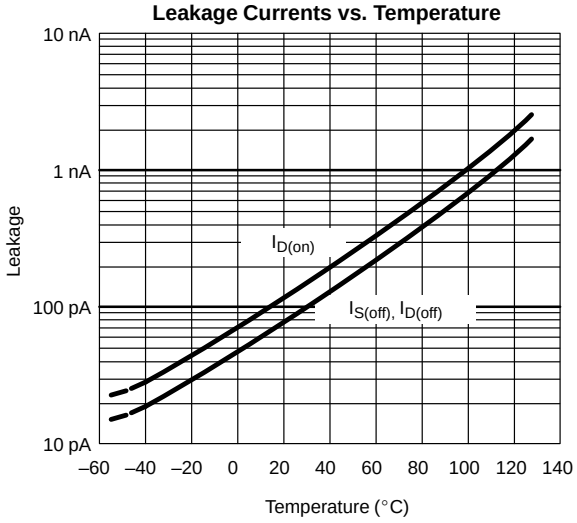
$r_{DS(on)}$ vs. V_D and Temperature



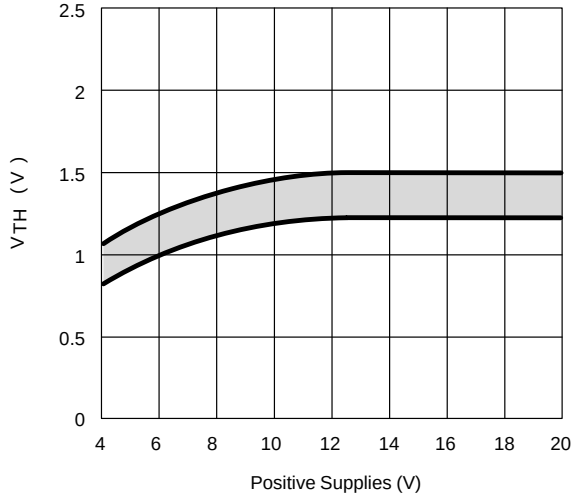
$r_{DS(on)}$ vs. V_D and Single Power Supply Voltages



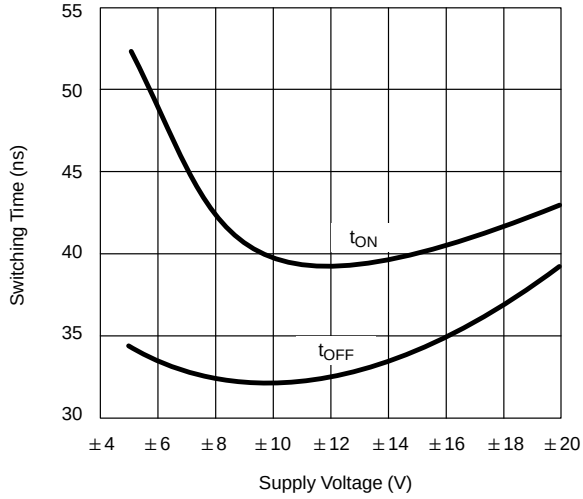
Leakage Currents vs. Temperature



Input Switching Threshold vs. Supply Voltage

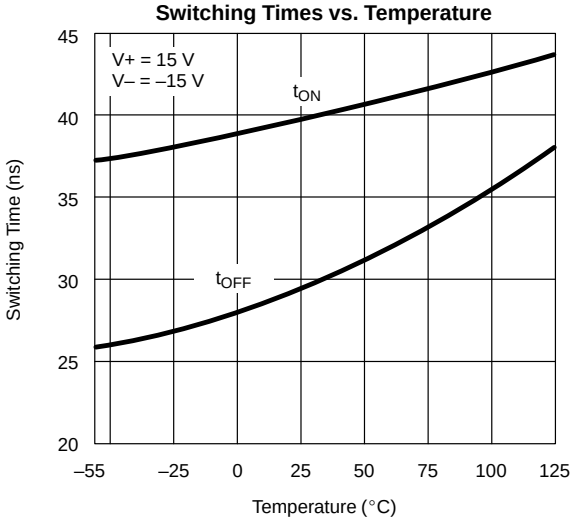


Switching Time vs. Power Supply Voltage

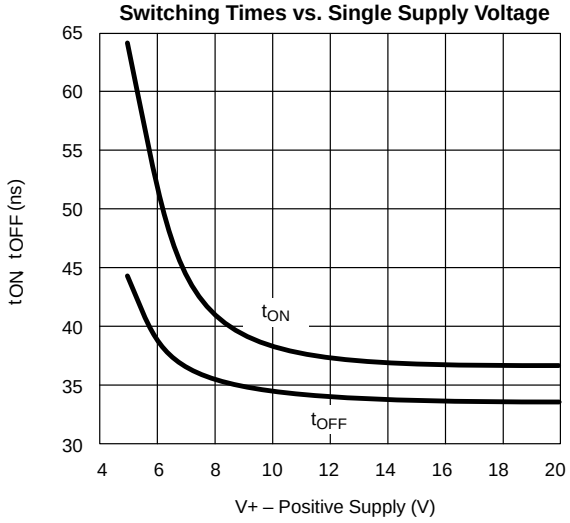


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

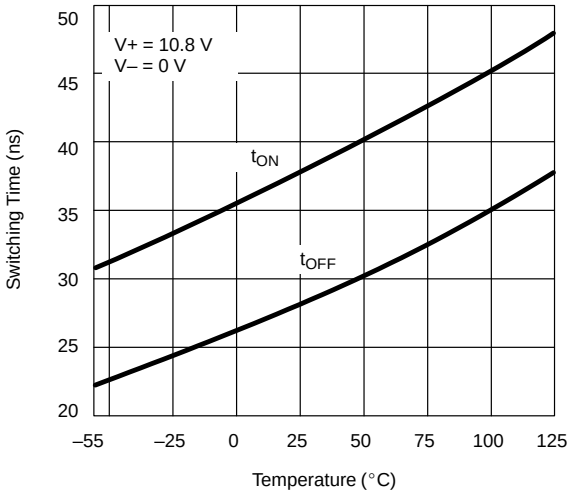
Switching Times vs. Temperature



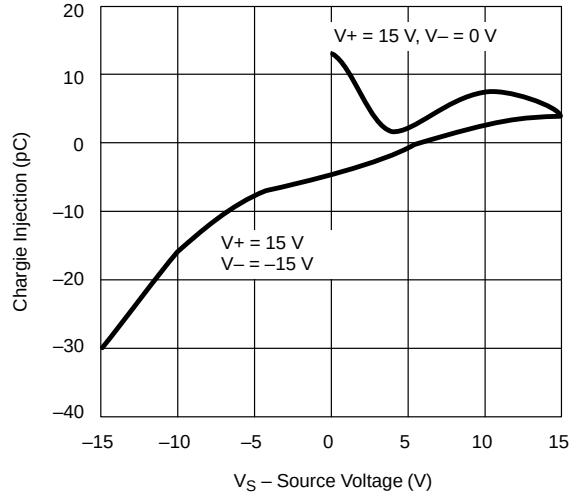
Switching Times vs. Single Supply Voltage



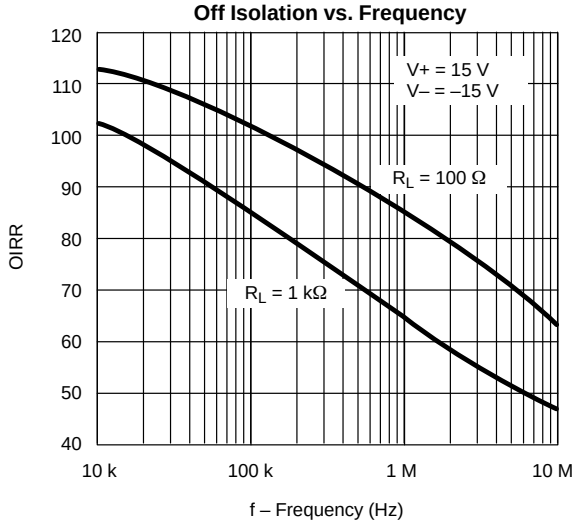
Switching Times vs. Temperature



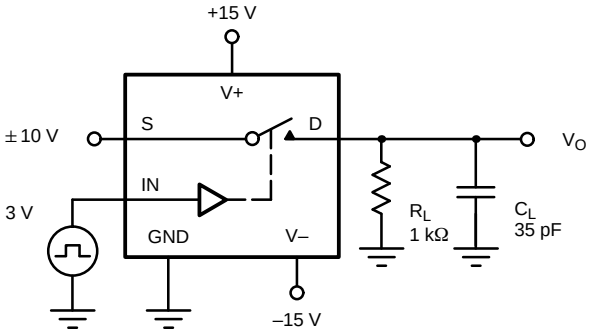
Charge Injection vs. Source Voltage

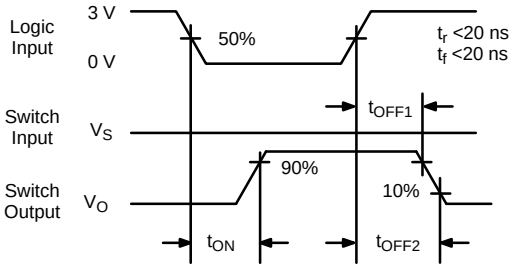


Off Isolation vs. Frequency



TEST CIRCUITS

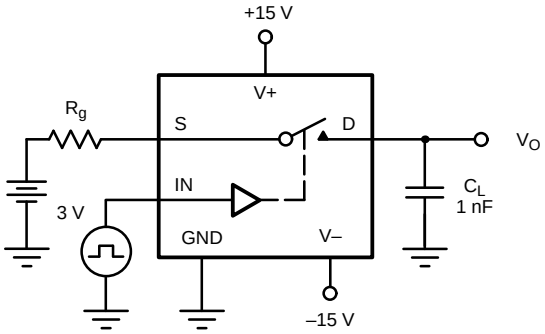


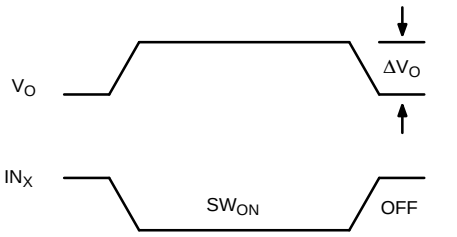


C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

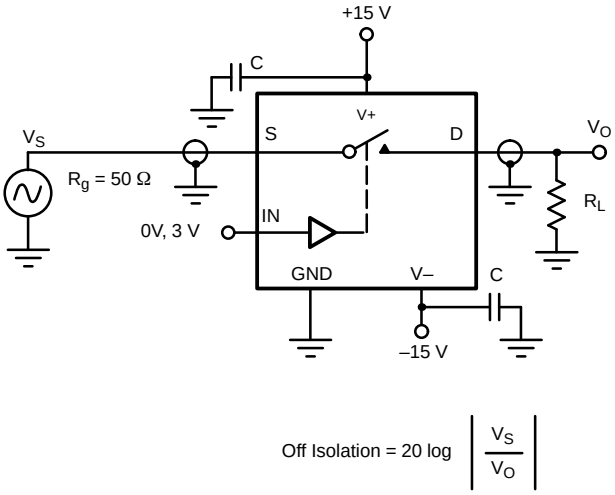
FIGURE 2. Switching Time





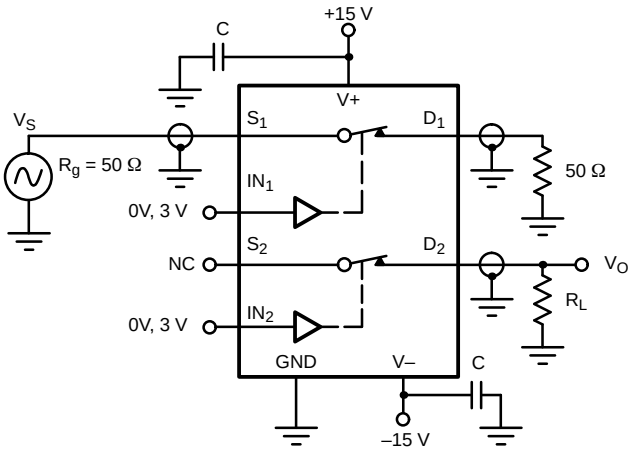
$Q = \Delta V_O \times C_L$

FIGURE 3. Charge Injection



Off Isolation = $20 \log \left| \frac{V_S}{V_O} \right|$

FIGURE 4. Off Isolation



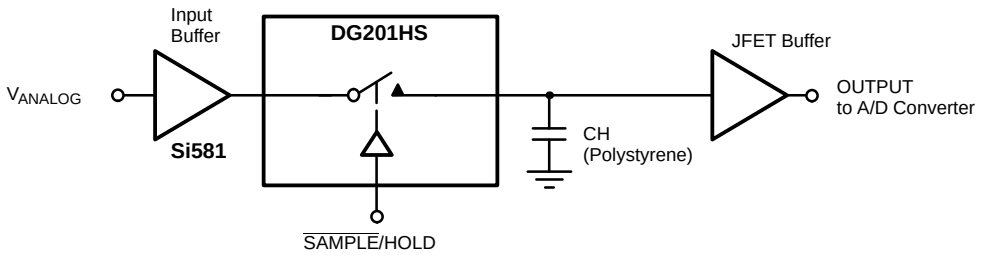
X_{TALK} Isolation = $20 \log \left| \frac{V_S}{V_O} \right|$

C = RF bypass

FIGURE 5. Crosstalk

APPLICATIONS

A high-speed, low-glitch analog switch such as Vishay Siliconix's DG201HS improves the accuracy and shortens the acquisition and settling times of a sample-and-hold circuit.



Notice

Specifications of the products displayed herein are subject to change without notice. Vishay Intertechnology, Inc., or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Vishay's terms and conditions of sale for such products, Vishay assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of Vishay products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Vishay for any damages resulting from such improper use or sale.