2 Megabit LPC Flash
SST49LF020

Advance Information

FEATURES:

- **Standard LPC Interface**
  - Conforms to Intel LPC Interface Specification 1.0
- **Organized as 256K x8**
- **Flexible Erase Capability**
  - Uniform 4 KByte sectors
  - Uniform 16 KByte overlay blocks
  - 16 KBytes Top boot block protection
  - Chip-Erase for PP Mode
- **Single 3.0-3.6V Read and Write Operations**
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption**
  - Active Read Current: 10 mA (typical)
  - Standby Current: 10 µA (typical)
- **Fast Sector-Erase/Byte-Program Operation**
  - Sector-Erase Time: 18 ms (typical)
  - Block-Erase Time: 18 ms (typical)
  - Chip-Erase Time: 70 ms (typical)
  - Byte-Program Time: 14 µs (typical)
  - Chip Rewrite Time: 4 seconds (typical)
  - Single-pulse Program or Erase
  - Internal timing generation
- **Two Operational Modes**
  - Low Pin Count (LPC) Interface mode for in-system operation
  - Parallel Programming (PP) Mode for fast production programming
- **LPC Interface Mode**
  - 5-signal communication interface supporting byte Read and Write
  - 33 MHz clock frequency operation
  - WP# and TBL# pins provide hardware write protect for entire chip and/or top boot block
  - Standard SDP Command Set
  - Data# Polling and Toggle Bit for End-of-Write detection
  - 5 GPI pins for system design flexibility
- **Parallel Programming (PP) Mode**
  - 11 pin multiplexed address and 8 pin data I/O interface
  - Supports fast In-System or PROM programming for manufacturing
- **CMOS I/O Compatibility**
- **Packages Available**
  - 32-lead PLCC
  - 32-lead TSOP (8mm x 14mm)

PRODUCT DESCRIPTION

The SST49LF020 flash memory device is designed to interface with the LPC bus for PC and Internet Applicance applications. It provides protection for the storage and update of code and data in addition to adding system design flexibility through five General Purpose Inputs (GPI). The SST49LF020 is in compliance with Intel Low Pin Count (LPC) Interface Specification 1.0. Two interface modes are supported: LPC Mode for In-System programming and Parallel Programming (PP) Mode for fast factory programming.

The SST49LF020 flash memory device is manufactured with SST's proprietary, high performance SuperFlash Technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST49LF020 device significantly improves performance and reliability, while lowering power consumption. The SST49LF020 device writes (Program or Erase) with a single 3.0-3.6V power supply. It uses less energy during Erase and Program than alternative flash memory technologies. The total energy consumed is a function of the applied voltage, current and time of application. Since for any give voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash memory technologies. The SST49LF020 product provides a maximum Byte-Program time of 20µsec. The entire memory can be erased and programmed byte-by-byte typically in 4 seconds, when using status detection features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. The SuperFlash technology provides fixed Erase and Program time, independent of the number of Erase/Program cycles that have performed. Therefore the system software or hardware does not have to be calibrated or correlated to the cumulative number of Erase/Program cycles as is necessary with alternative flash memory technologies, whose Erase and Program time increase with accumulated Erase/Program cycles.

To protect against inadvertent write, the SST49LF020 device has on-chip hardware and software data (SDP) protection schemes. It is offered with a typical endurance of 100,000 cycles. Data retention is rated at greater than 100 years.

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To meet high density, surface mount requirements, the SST49LF020 device is offered in 32-lead TSOP and 32-lead PLCC packages. See Figures 1 and 2 for pinouts and Table 2 for pin descriptions.

Mode Selection and Description

The SST49LF020 flash memory device operates in two distinct interface modes: the LPC mode and the Parallel Programming (PP) mode. The Mode pin is used to set the interface mode selection. If the Mode pin is set to logic High, the device is in PP mode; while if the Mode pin is set Low, the device is in the LPC mode. The Mode selection pin must be configured prior to device operation.

In LPC mode, the device is configured to its host using standard LPC interface protocol. Communication between Host and the SST49LF020 occurs via the 4-bit I/O communication signals, LAD [3:0] and LFRAME#.

In PP mode, the device is programmed via an 11-bit address and an 8-bit data I/O parallel signals. The address inputs are multiplexed in row and column selected by control signal R/C# pin. The row addresses are mapped to the higher internal addresses, and the column addresses are mapped to the lower internal addresses. See Device Memory Map for address assignments.

LPC MODE

Device Operation

The LPC mode uses a 5-signal communication interface, a 4-bit address/data bus, LAD[3:0], and a control line, LFRAME#, to control operations of the SST49LF020. Cycle type operations such as Memory Read and Memory Write are defined in Intel Low Pin Count Interface Specification, Revision 1.0. JEDEC Standard SDP (Software Data Protection) Program and Erase commands sequences are incorporated into the standard LPC memory cycles. See Figure 8 through Figure 13 timing diagrams for command sequences.

LPC operations are transmitted via the 4-bit Address/Data bus (LAD[3:0]), and follow a particular sequence, depending on whether they are Read or Write operations. The standard LPC memory cycle is defined in Table 13.

Both LPC Read and Write operations start in a similar way as shown in Figures 6 and 7 timing diagrams. The host (which is the term used here to describe the device driving the memory) asserts LFRAME# for one or more clocks and drives a start value on the LAD[3:0] bus.

At the beginning of an operation, the host may hold the LFRAME# active for several clock cycles, and even change the Start value. The LAD[3:0] bus is latched every rising edge of the clock. On the cycle in which LFRAME# goes inactive, the last latched value is taken as the Start value. CE# must be asserted one cycle before the start cycle to select the SST49LF020 for Read and Write operations.

Once the SST49LF020 identifies the operation as valid (a start value of all zeros), it next expects a nibble that indicates whether this is a memory read or program cycle. Once this is received, the device is now ready for the Address and Data cycles. For Program operation the Data cycle will follow the Address cycle, and for Read operation TAR and SYNC cycles occur between the Address and Data cycles. At the end of every operation, the control of the bus must be returned to the host by a 2 clock TAR cycle.

Device Memory Hardware Write Protection

The Top Boot Lock (TBL#) and Write Protect (WP#) pins are provided for hardware write protection of device memory in the SST49LF020. The TBL# pin is used to write protect four boot sectors (16 KBytes) at the highest memory address range. WP# pin write protects the remaining sectors in the flash memory.

An active low signal at the TBL# pin prevents Program and Erase operations of the top boot sectors. When TBL# pin is held high, the write protection of the top boot sectors is disabled. The WP# pin serves the same function for the remaining sectors of the device memory. The TBL# and WP# pins write protection functions operate independently of one another.

Both TBL# and WP# pins must be set to their required protection states prior to starting a Program or Erase operation. A logic level change occurring at the TBL# or WP# pin during a Program or Erase operation could cause unpredictable results.

Reset

A V_{IL} on INIT# or RST# pins initiates a device reset. INIT# and RST# pins have same function internally. It is required to drive INIT# or RST# pins low during a system reset to ensure proper CPU initialization.

During a Read operation, driving INIT# or RST# pins low deselects the device and places the output drivers, LAD[3:0], in a high-impedance state. The reset signal must be held low for a minimal duration of time T_{RSTP}. A reset latency will occur if a reset procedure is performed during a Program or Erase operation. See Table 12, Reset Timing Parameters, for more information. A device reset during an active Program or Erase will abort the operation and mem-

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ory contents may become invalid due to data being altered had been disrupted from an incomplete Erase or Program operation.

GENERAL PURPOSE INPUTS REGISTER

Bit	Function	Pin#	
		32-PLCC	32-TSOP
7:5	Reserved	-	-
4	GPI[4] Reads status of general purpose input pin	30	7
3	GPI[3] Reads status of general purpose input pin	3	15
2	GPI[2] Reads status of general purpose input pin	4	16
1	GPI[1] Reads status of general purpose input pin	5	17
0	GPI[0] Reads status of general purpose input pin	6	18

Registers

There is one register available on the SST49LF020. The General Purpose Inputs Register. This register appears at its respective address location in the 4 GByte system memory map.

General Purpose Inputs Register

The GPI_REG (General Purpose Inputs Register) passes the state of GPI[4:0] pins at power-up on the SST49LF020. It is recommended that the GPI[4:0] pins be in the desired state before LFRAME# is brought low for the beginning of the next bus cycle, and remain in that state until the end of the cycle. There is no default value since this is a pass-through register. The GPI register appears at FFBC0100H in the 4 GBytes system memory map. See General Purpose Inputs Register table for the GPI_REG bits and function.

CE#

The CE# pin, enables and disables the SST49LF020, controlling read and write access of the device. To enable the SST49LF020, the CE# pin must be driven low one cycle prior to LFRAME# being driven low. For write (erase or program) cycles, the CE# pin must remain low during the internal programming. When CE# is high, the SST49LF020 is placed in low-power standby-mode.

LFRAME#

The LFRAME# signifies the start of a frame or the termination of a broken frame. Asserting LFRAME# for one or more clock cycle and driving a valid START value on LAD[3:0] will initiate device operation. The device enters standby mode when LFRAME# and CE# are high and no internal operations is in progress.

Abort Mechanism

If LFRAME# is driven low for one or more clock cycles during a LPC cycle, the cycle will be terminated and the device will wait for the ABORT command. The host must drive the LAD[3:0] with ‘1111b’ (ABORT command) to return the device to the ready mode. If abort occurs during the internal write cycle, the data may be incorrectly programmed or erased. It is required to wait for the Write operation to complete prior to initiation of the abort command. It is recommended to check the write status with Data# Polling (DQ_7) or Toggle Bit (DQ_6) pins. One other option is to wait for the fixed write time to expire.

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PARALLEL PROGRAMMING MODE

Device Operation

Commands are used to initiate the memory operation functions of the device. The data portion of the software command sequence is latched on the rising edge of WE#. During the software command sequence the row address is latched on the falling edge of R/C# and the column address is latched on the rising edge of R/C#.

Read

The Read operation of the SST49LF020 device is controlled by OE#. OE# is the output control and is used to gate data from the output pins. Refer to the Read cycle timing diagram, Figure 15, for further details.

Reset

Driving the RST# low will initiate a hardware reset of the SST49LF020.

Byte-Program Operation

The SST49LF020 device is programmed on a byte-by-byte basis. The Byte-Program operation is initiated by executing a four-byte-command load sequence for Software Data Protection with address (BA) and data in the last byte sequence. During the Byte-Program operation, the row address (A_{10}-A_0) is latched on the falling edge of R/C# and the column address (A_{21}-A_{11}) is latched on the rising edge of R/C#. The data bus is latched on the rising edge of WE#. The Program operation, once initiated, will be completed, within 20 µs. See Figures 7 and 19 for Program operation timing diagram and Figure 31 for its flowchart. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

Sector-Erase Operation

The Sector-Erase operation allows the system to erase the device on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector-Erase operation is initiated by executing a six-byte-command load sequence for Software Data Protection with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 20 for Sector-Erase timing waveforms. Any commands written during the Sector-Erase operation will be ignored.

Block-Erase Operation

The Block-Erase Operation allows the system to erase the device in 16 KByte uniform block size. The Block-Erase operation is initiated by executing a six-byte-command load sequence for Software Data Protection with Block-Erase command (50H) and block address. The internal Block-Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 21 for Block-Erase timing waveforms. Any commands written during the Block-Erase operation will be ignored.

Chip-Erase

The SST49LF020 device provides a Chip-Erase operation only in PP Mode, which allows the user to erase the entire memory array to the “1” state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte Software Data Protection command sequence with Chip-Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE#. During the internal Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4 for the command sequence, Figure 22 for Chip-Erase timing diagram, and Figure 34 for the flowchart. Any commands written during the Chip-Erase operation will be ignored.

Write Operation Status Detection

The SST49LF020 device provides two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The End-of-Write detection mode is enabled after the rising edge of WE# which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

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Data# Polling (DQ_7)

When the SST49LF020 device is in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. The device is then ready for the next operation. During internal Erase operation, any attempt to read DQ_7 will produce a '0'. Once the internal Erase operation is completed, DQ_7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# pulse for Program operation. For Sector-, Block- or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# pulse. See Figures 9 and 17 for Data# Polling timing diagram and Figure 33 for a flowchart.

Toggle Bit (DQ_6)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating "0" and "1", i.e., toggling between "0" and "1". When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# pulse for Program operation. For Sector-, Block- or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# pulse. See Figures 10 and 18 for Toggle Bit timing diagram and Figure 32 for a flowchart.

Data Protection

The SST49LF020 device provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The SST49LF020 provides the JEDEC approved Software Data Protection scheme for all data alteration operation, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three byte sequence. The three byte-load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six byte load sequence. The SST49LF020 device is shipped with the Software Data Protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to read mode, within T_{RC}.

Electrical Specifications

The AC and DC specifications for the LPC interface signals (LAD[3:0], LCLCK. LFRAME# and RST#) as defined in Section 4.2.2 of the "PCI Local Bus specification, Rev. 2.1". Refer to Table 5 for the DC voltage and current specifications. Refer to Tables 11, 12, 14, and 15 for the AC timing specifications for Clock, Read, Program, Erase and Reset operations.

Product Identification Mode

The product identification mode identifies the device as SST49LF020 and the manufacturer as SST.

TABLE 1: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer's ID	00000H	BFH
Device ID SST49LF020	00001H	61H

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Design Considerations

SST recommends a high frequency 0.1 µF ceramic capacitor to be placed as close as possible between V_{DD} and V_{SS} less than 1 cm away from the V_{DD} pin of the device. Additionally, a low frequency 4.7 µF electrolytic capacitor from V_{DD} to V_{SS} should be placed within 5 cm of the V_{DD} pin. If you use a socket for programming purposes add an additional 1-10 µF next to each socket.

The RST# pin must remain stable at V_{IH} for the entire duration of an Erase operation. WP# must remain stable at V_{IH} for the entire duration of the Erase and Program operations for non-boot block sectors. To write data to the top boot block sectors, the TBL# pin must also remain stable at V_{IH} for the entire duration of the Erase and Program operations.

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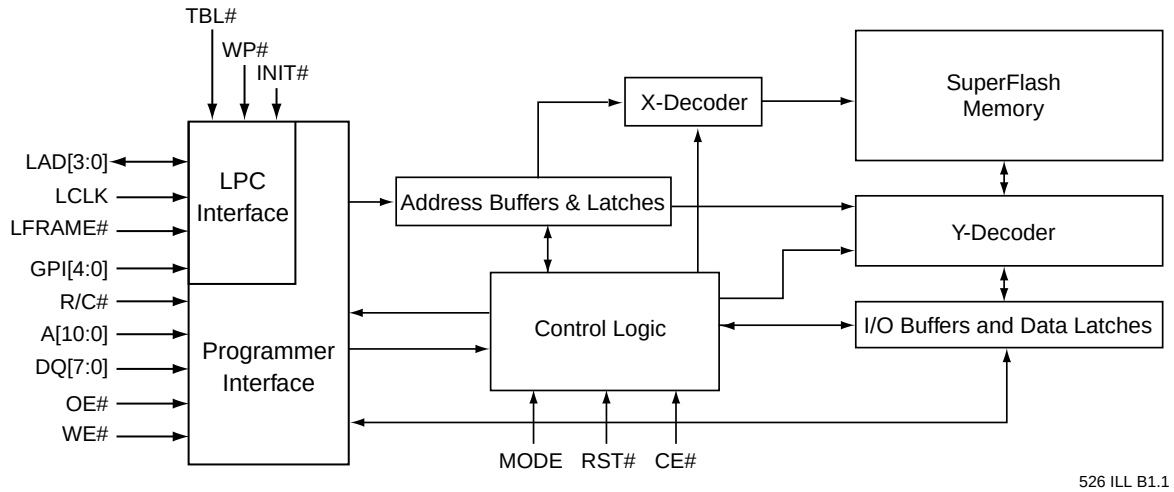
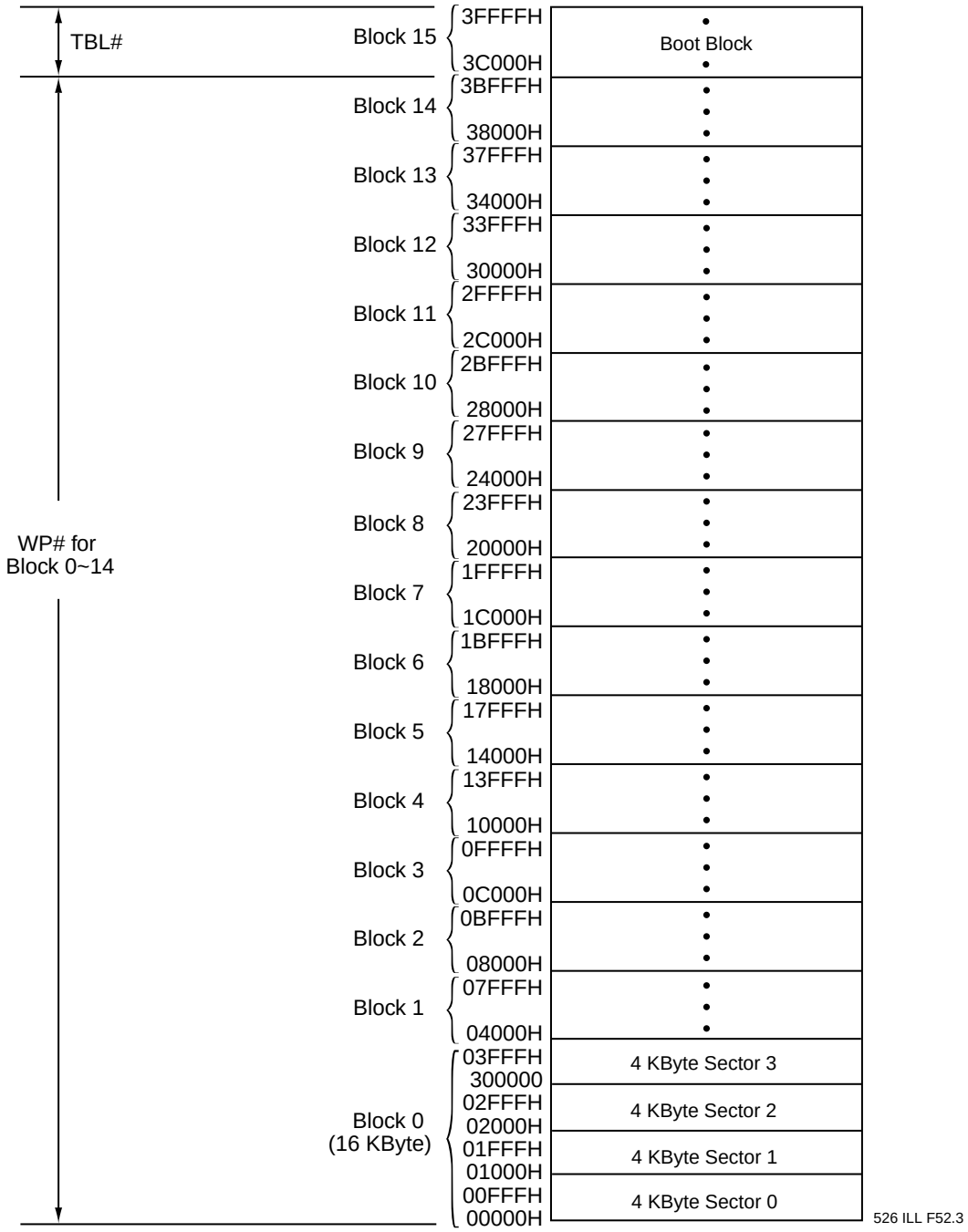
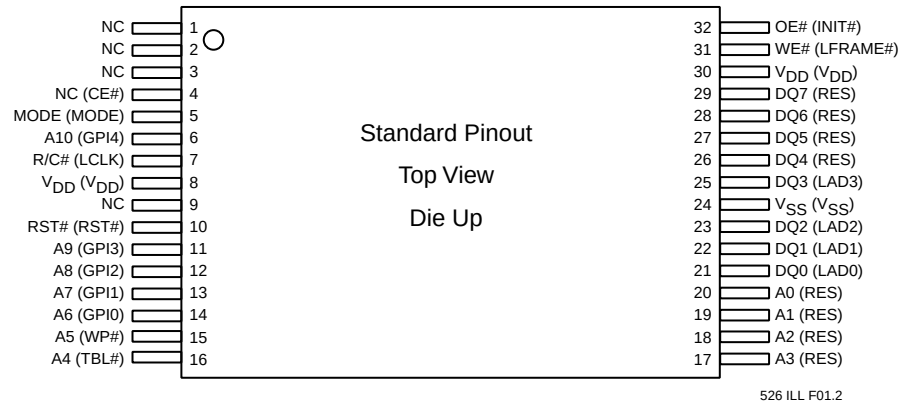
FUNCTIONAL BLOCK DIAGRAM



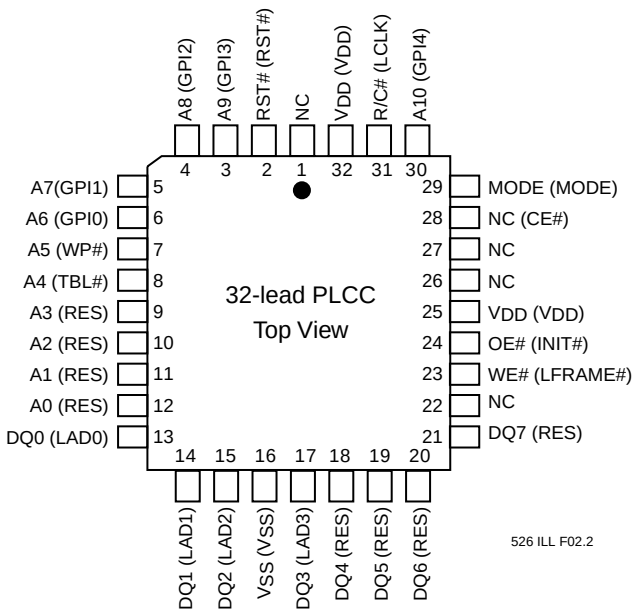


DEVICE MEMORY MAP FOR SST49LF020



( ) Designates LPC Mode

FIGURE 1: PIN ASSIGNMENTS FOR 32-LEAD TSOP (8MM X 14MM)



( ) Designates LPC Mode

FIGURE 2: PIN ASSIGNMENTS FOR 32-LEAD PLCC

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Type[1]	Interface		Functions
			PP	LPC	
A_{10}-A_0	Address	I	X		Inputs for low-order addresses during Read and Write operations. Addresses are internally latched during a Write cycle. For the programming interface, these addresses are latched by R/C# and share the same pins as the high-order address inputs.
DQ_7-DQ_0	Data	I/O	X		To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# is high.
OE#	Output Enable	I	X		To gate the data output buffers.
WE#	Write Enable	I	X		To control the Write operations.
MODE	Interface Mode Select	I	X	X	This pin determines which interface is operational. When held high, programmer mode is enabled and when held low, LPC mode is enabled. This pin must be setup at power-up or before return from reset and not change during device operation. This pin is internally pulled down with a resistor between 20-100KΩ.
INIT#	Initialize	I		X	This is the second reset pin for in-system use. This pin is internally combined with the RST# pin; If this pin or RST# pin is driven low, identical operation is exhibited.
GPI[4:0]	General Purpose Inputs	I		X	These individual inputs can be used for additional board flexibility. The state of these pins can be read through LPC registers. These inputs should be at their desired state before the start of the PCI clock cycle during which the read is attempted, and should remain in place until the end of the Read cycle. Unused GPI pins must not be floated.
TBL#	Top Block Lock	I		X	When low, prevents programming boot block sectors at top of memory. When TBL# is high it disables hardware write protection for the top block sectors.
LAD[3:0]	Address and Data	I/O		X	To provide LPC control signals, as well as addresses and Command Inputs/Outputs data.
LCLK	Clock	I		X	To provide a clock input to the control unit
LFRAME#	Frame	I		X	To indicate start of a data transfer operation; also used to abort an LPC cycle in progress.
RST#	Reset	I	X	X	To reset the operation of the device
WP#	Write Protect	I		X	When low, prevents programming to all but the highest addressable top boot blocks. When WP# is high it disables hardware write protection for these blocks.
R/C#	Row/Column Select	I	X		Select for the Programming interface, this pin determines whether the address pins are pointing to the row addresses, or to the column addresses.
RES	Reserved			X	These pins must be left unconnected.
V_{DD}	Power Supply	I	X	X	To provide power supply (3.0-3.6V)
Vss	Ground	I	X	X	Circuit ground (OV reference)
CE#	Chip Enable	I		X	This signal must be asserted to select the device. When CE# is low, the device is enabled. When CE# is high, the device is placed in low power standby mode.
NC	No Connection	I	X	X	Unconnected pins.

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1. I=Input, O=Output

TABLE 3: OPERATION MODES SELECTION (PP MODE)

Mode	RST#	OE#	WE#	DQ	Address
Read	V_{IH}	V_{IL}	V_{IL}	D_{OUT}	A_{IN}
Program	V_{IH}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Erase	V_{IH}	V_{IH}	V_{IL}	X[1]	Sector or Block address, XXH for Chip-Erase
Reset	V_{IL}	X	X	High Z	X
Write Inhibit	V_{IH}	V_{IL}	V_{IL}	High Z/D_{OUT}	X
	X	V_{IH}	X	High Z/D_{OUT}	X
Product Identification	V_{IH}	V_{IL}	V_{IL}	Manufacturer's ID (BFH) Device ID[2]	A_{18}-A_1=V_{IL}, A_0=V_{IL} A_{18}-A_1=V_{IL}, A_0=V_{IH}

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1. X can be V_{IL} or V_{IH}, but no other value.
2. Device ID = 61H

TABLE 4: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st[1] Write Cycle		2nd[1] Write Cycle		3rd[1] Write Cycle		4th[1] Write Cycle		5th[1] Write Cycle		6th[1] Write Cycle	
	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data
Byte-Program	5555H	AAH	2AAAH	55H	5555H	A0H	BA[3]	Data				
Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SAx[4]	30H
Block-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	BAx[5]	50H
Chip-Erase[6]	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry[7]	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit[8]	XXH	F0H										
Software ID Exit[8]	5555H	AAH	2AAAH	55H	5555H	F0H						

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1. LPC Mode use consecutive Write cycles to complete a command sequence;
   PP Mode use consecutive bus cycles to complete a command sequence.
2. Address format A_{14}-A_0 (Hex), Addresses A_{15}-A_{21} can be V_{IL} or V_{IH}, but no other value, for the Command sequence in PP Mode.
3. BA = Program Byte address
4. SA_x for Sector-Erase Address
5. BA_x for Block-Erase Address
6. Chip-Erase is supported in PP Mode only
7. With A_{17}-A_1=0; SST Manufacturer's ID=BFH, is read with A_0=0.
   SST49LF020 Device ID = 61H, is read with A_0=1.
8. Both Software ID Exit operations are equivalent

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Advance Information

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD} + 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -1.0V to V_{DD} + 1.0V
Package Power Dissipation Capability (Ta=25°C) 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) . . . . . 240°C
Output Short Circuit Current[1] . . . . . 50 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0°C to +85°C	3.0-3.6V

AC CONDITIONS OF TEST[1]

Input Rise/Fall Time	3 ns
Output Load	C_L = 30 pF
See Figures 25 and 26	

1. LPC interface signals use PCI load condition.

TABLE 5: DC OPERATING CHARACTERISTICS (ALL INTERFACES)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Power Supply Current				Address input=V_{IL}/V_{IH}, at f=1/T_{RC} Min, V_{DD}=V_{DD} Max (PP Mode)
	Read		12	mA	OE#=V_{IH}, WE#=V_{IH}
	Write		24	mA	OE#=V_{IH}, WE#=V_{IL}, V_{DD}=V_{DD} Max (PP Mode)
I_{SB}	Standby V_{DD} Current (LPC Interface)		100	µA	LFRAME#=V_{IH}, f=33 MHz, CE#=V_{IH} V_{DD}=V_{DD} Max, All other inputs ≥ 0.9 V_{DD} or ≤ 0.1 V_{DD}
I_{RY}[1]	Ready Mode V_{DD} Current (LPC Interface)		10	mA	LFRAME#=V_{IL}, f=33 MHz, V_{DD}=V_{DD} Max All other inputs ≥ 0.9 V_{DD} or ≤ 0.1 V_{DD}
I_I	Input Current for IC Pin		200	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current		1	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IHI}	INIT# Input High Voltage	1.0	V_{DD}+0.5	V	V_{DD}=V_{DD} Max
V_{ILI}	INIT# Input Low Voltage	-0.5	0.4	V	V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage	-0.5	0.3 V_{DD}	V	V_{DD}=V_{DD} Min
V_{IH}	Input High Voltage	0.5 V_{DD}	V_{DD}+0.5	V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage		0.1 V_{DD}	V	I_{OL}=1500 µA, V_{DD}=V_{DD} Min
V_{OH}	Output High Voltage	0.9 V_{DD}		V	I_{OH}=-500 µA, V_{DD}=V_{DD} Min

T5.5 526

1. The device is in Ready Mode when no activity is on the LPC bus.

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TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	100	µs

T6.1 526

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter

TABLE 7: PIN CAPACITANCE (V_{DD}=3.3V, Ta=25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$=0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN}=0V	6 pF
L_{PIN}[2]	Pin Inductance		20 nH

T7.0 526

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. Refer to PCI Spec.

TABLE 8: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

T8.1 526

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 9: CLOCK TIMING PARAMETERS (LPC MODE)

Symbol	Parameter	Min	Max	Units
T_{CYC}	LCLK Cycle Time	30		ns
T_{HIGH}	LCLK High Time	11		ns
T_{LOW}	LCLK Low Time	11		ns
-	LCLK Slew Rate (peak-to-peak)	1	4	V/ns
-	RST# or INIT# Slew Rate	50		mV/ns

T9.0 526

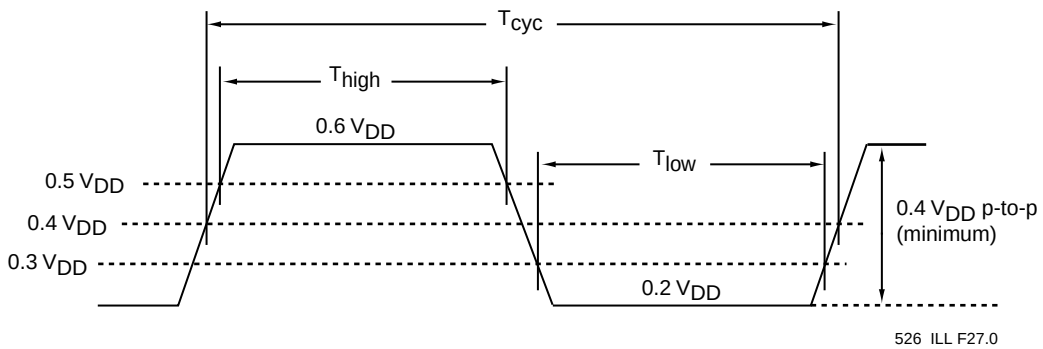

FIGURE 3: LCLK WAVEFORM

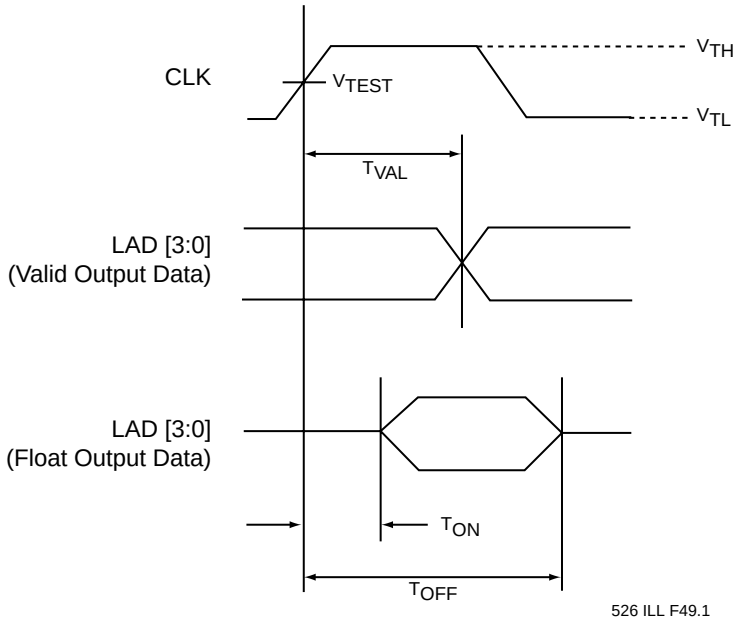

FIGURE 4: OUTPUT TIMING PARAMETERS

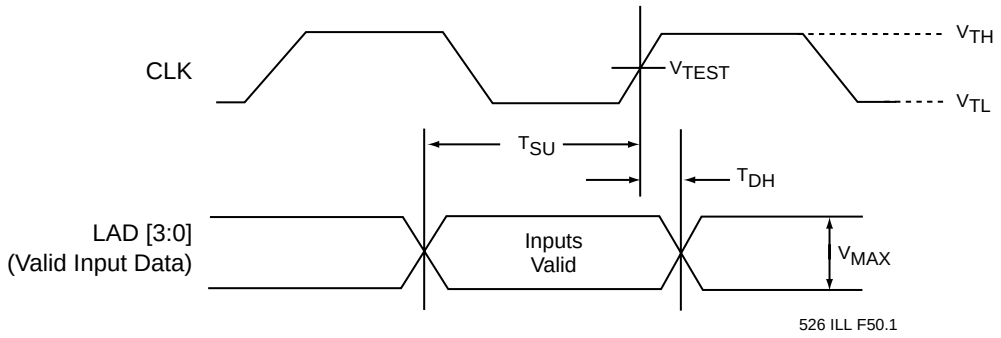

FIGURE 5: INPUT TIMING PARAMETERS

TABLE 10: INTERFACE MEASUREMENT CONDITION PARAMETERS

Symbol	Value	Units
V_{TH}[1]	0.6 V_{DD}	V
V_{TL}[1]	0.2 V_{DD}	V
V_{TEST}	0.4 V_{DD}	V
V_{MAX}[1]	0.4 V_{DD}	V
Input Signal Edge Rate	1 V/ns	

T10.2 526

1. The input test environment is done with 0.1 V_{DD} of overdrive over V_{IH} and V_{IL}. Timing parameters must be met with no more overdrive than this. V_{MAX} specifies the maximum peak-to-peak waveform allowed for measuring input timing. Production testing may use different voltage values, but must correlate results back to these parameters.

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AC CHARACTERISTICS (LPC MODE)

TABLE 11: READ/WRITE CYCLE TIMING PARAMETERS (LPC MODE), V_{DD}=3.0-3.6V

Symbol	Parameter	Min	Max	Units
T_{CYC}	Clock Cycle Time	30		ns
T_{SU}	Data Set Up Time to Clock Rising	7		ns
T_{DH}	Clock Rising to Data Hold Time	0		ns
T_{VAL}	Clock Rising to Data Valid	2	11	ns
T_{BP}	Byte Programming Time		20	µs
T_{SE}	Sector-Erase Time		25	ms
T_{BE}	Block-Erase Time		25	ms

T11.1 526

TABLE 12: RESET TIMING PARAMETERS, V_{DD} = 3.0-3.6V

Symbol	Parameter	Min	Max	Units
T_{PRST}	V_{DD} stable to Reset Active	1		ms
T_{KRST}	Clock Stable to Reset Active	100		µs
T_{RSTP}	Reset Pulse Width	100		ns
T_{RSTF}	Reset Active to Output Float		50	ns
T_{RST}	Reset Inactive to Input Active		1	µs

T12.1 526

TABLE 13: STANDARD LPC MEMORY CYCLE DEFINITION (LPC MODE)

Field	No. of Clocks	Description
START	1	“0000b” appears on LPC bus to indicate the start of cycle
CYCTYPE + DIR	1	Cycle Type: Indicates the type of cycle. Bits 3:2 must be “01b” for memory cycle. Bit 2 indicates the type of transfer “0” for Read, “1” for write. DIR: Indicates the direction of the transfer. “0b” for Read, “1b” for Write. Bit 0 is reserved. “010Xb” indicates memory Read cycle; while “011xb” indicates memory Write cycle.
TAR	2	The last component driving LAD[3:0] will drive it to “1111b” during the first clock, and tri-state it during the second clock.
ADDR	8	Address Phase for Memory Cycle. LPC supports the 32-bit address protocol. The addresses transfer most significant nibble first and least significant nibble last. (i.e., Address[31:28] on LAD[3:0] first, and Address[3:0] on LAD[3:0] last.)
Sync	N	Synchronize to host or peripheral by adding wait states. “0000b” means Ready, “0101b” means Short Wait, “0110b” means Long Wait, “1001b” for DMA only, “1010b” means error, other values are reserved.
Data	2	Data Phase for Memory Cycle. **The data transfer least significant nibble first and most significant nibble last.** (i.e., DQ[3:0] on LAD[3:0] first, then DQ[7:4] on LAD[3:0] last.)

T13.0 526

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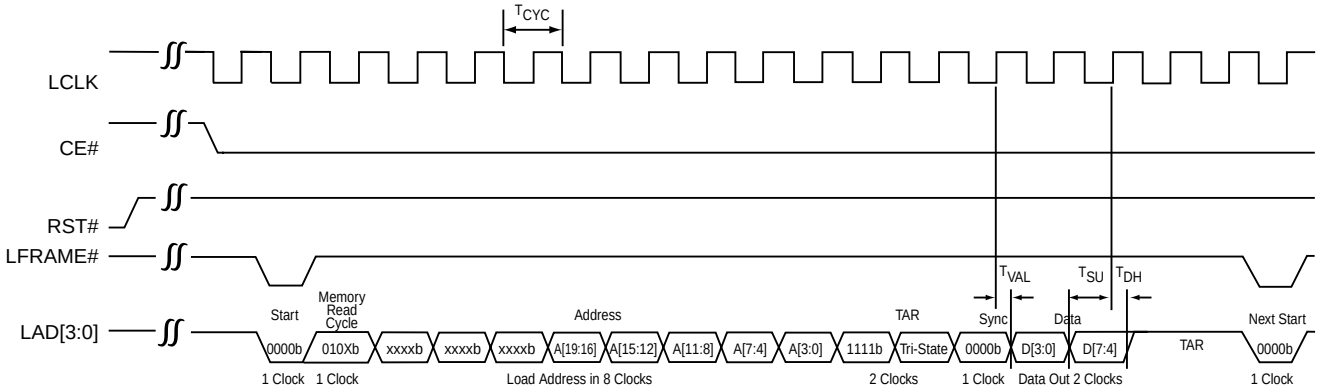

FIGURE 6: READ CYCLE TIMING DIAGRAM (LPC MODE)

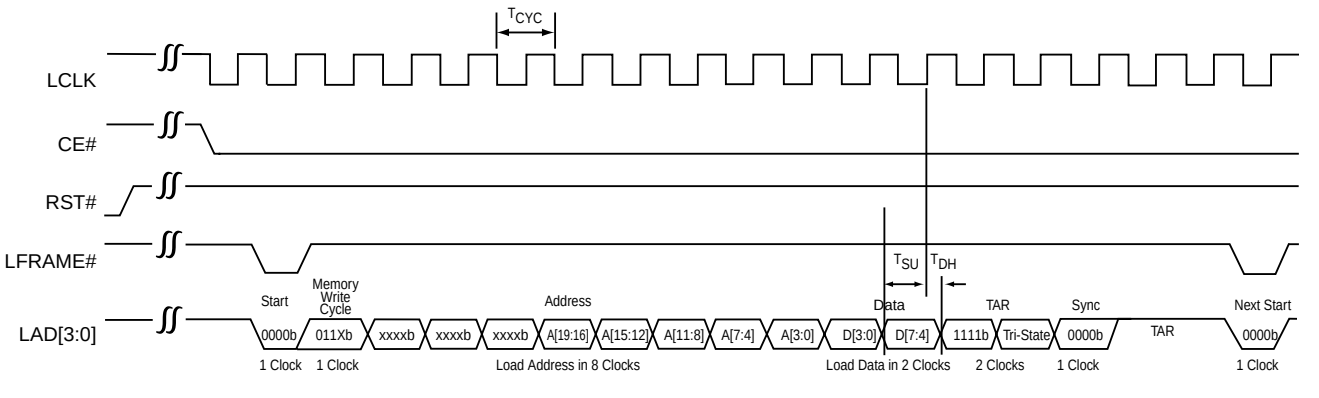

FIGURE 7: WRITE CYCLE TIMING DIAGRAM (LPC MODE)

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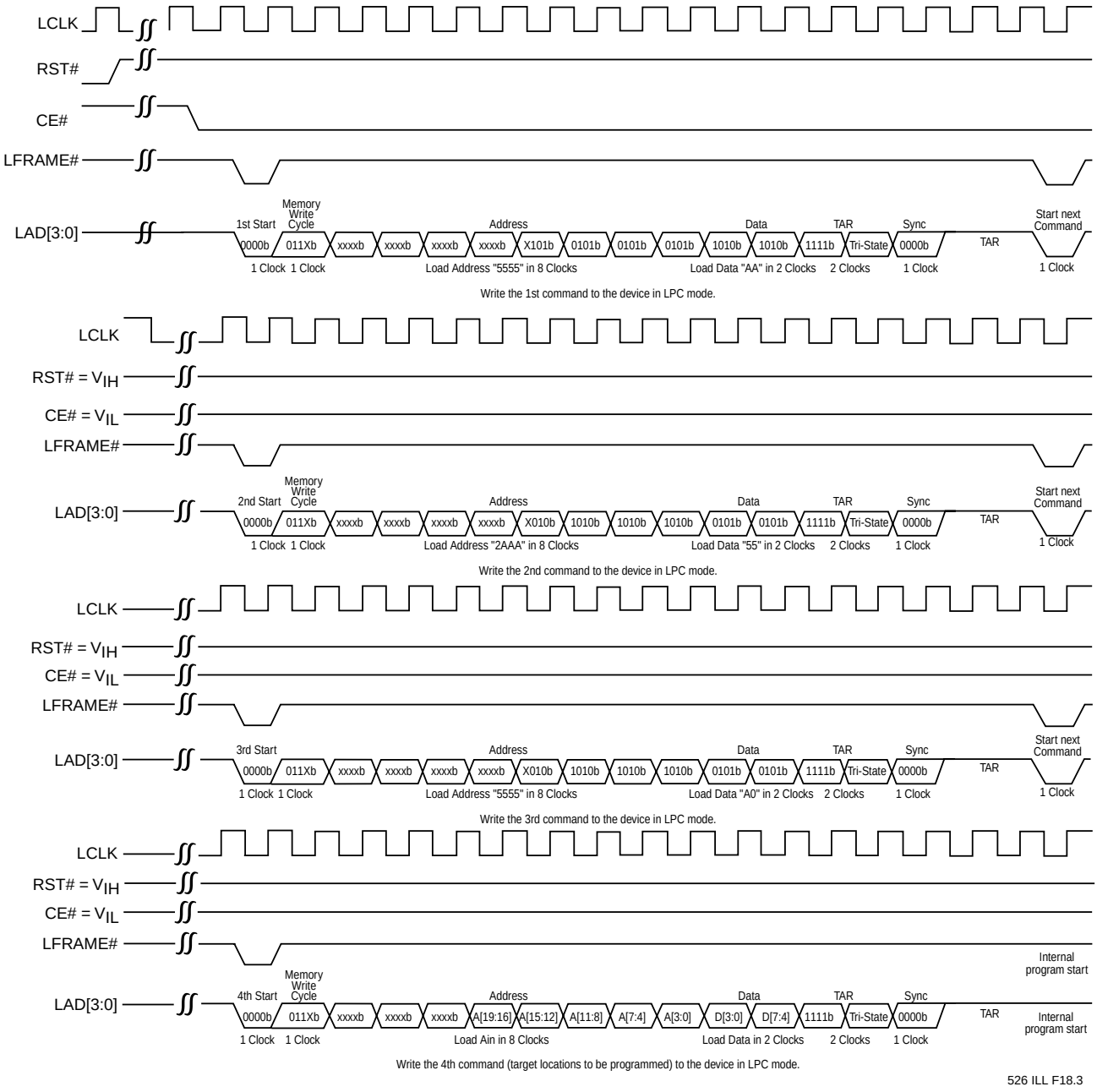


FIGURE 8: PROGRAM CYCLE TIMING DIAGRAM (LPC MODE)

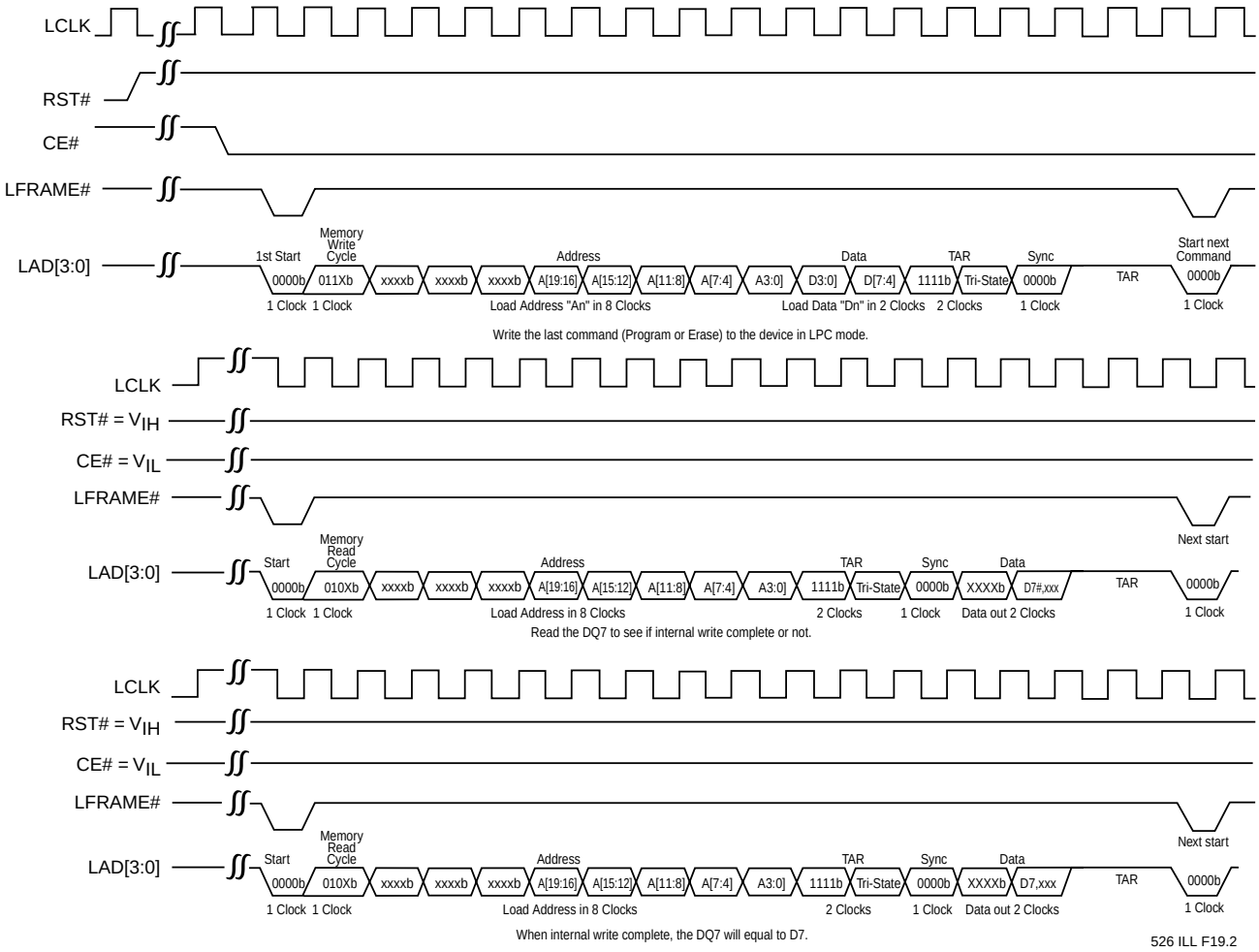


FIGURE 9: DATA# POLLING TIMING DIAGRAM (LPC MODE)

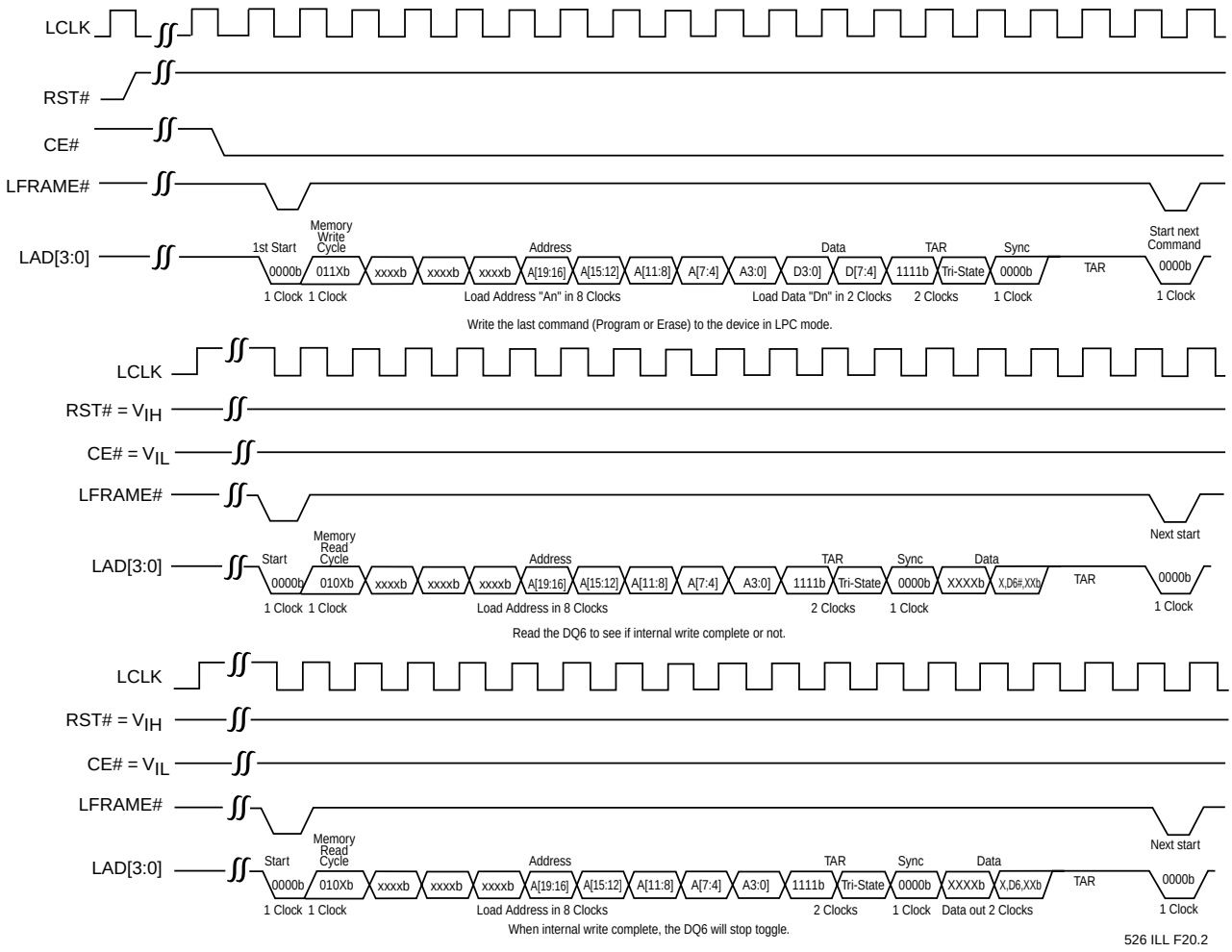


FIGURE 10: TOGGLE BIT TIMING DIAGRAM (LPC MODE)

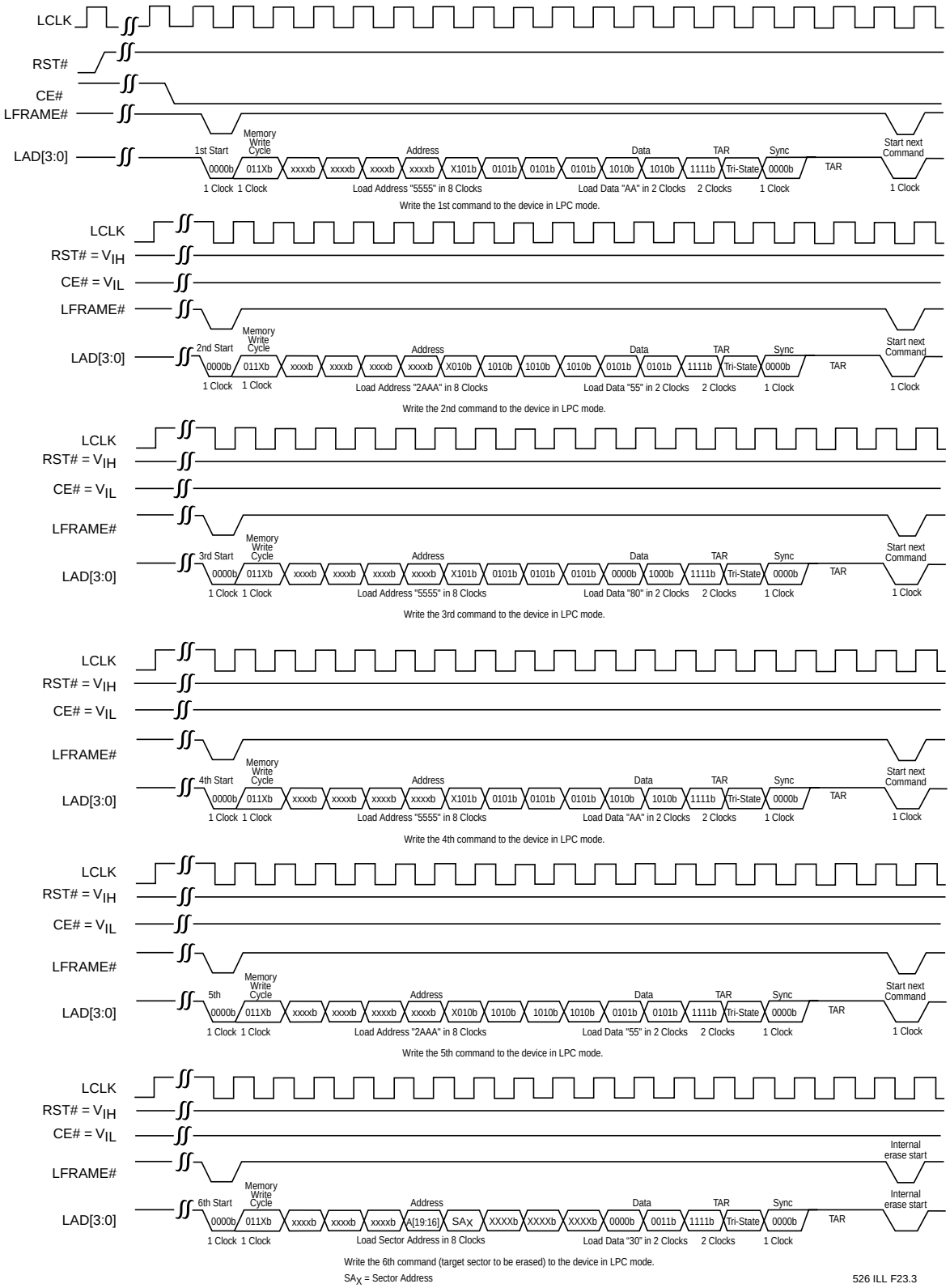


FIGURE 11: SECTOR-ERASE TIMING DIAGRAM (LPC MODE)

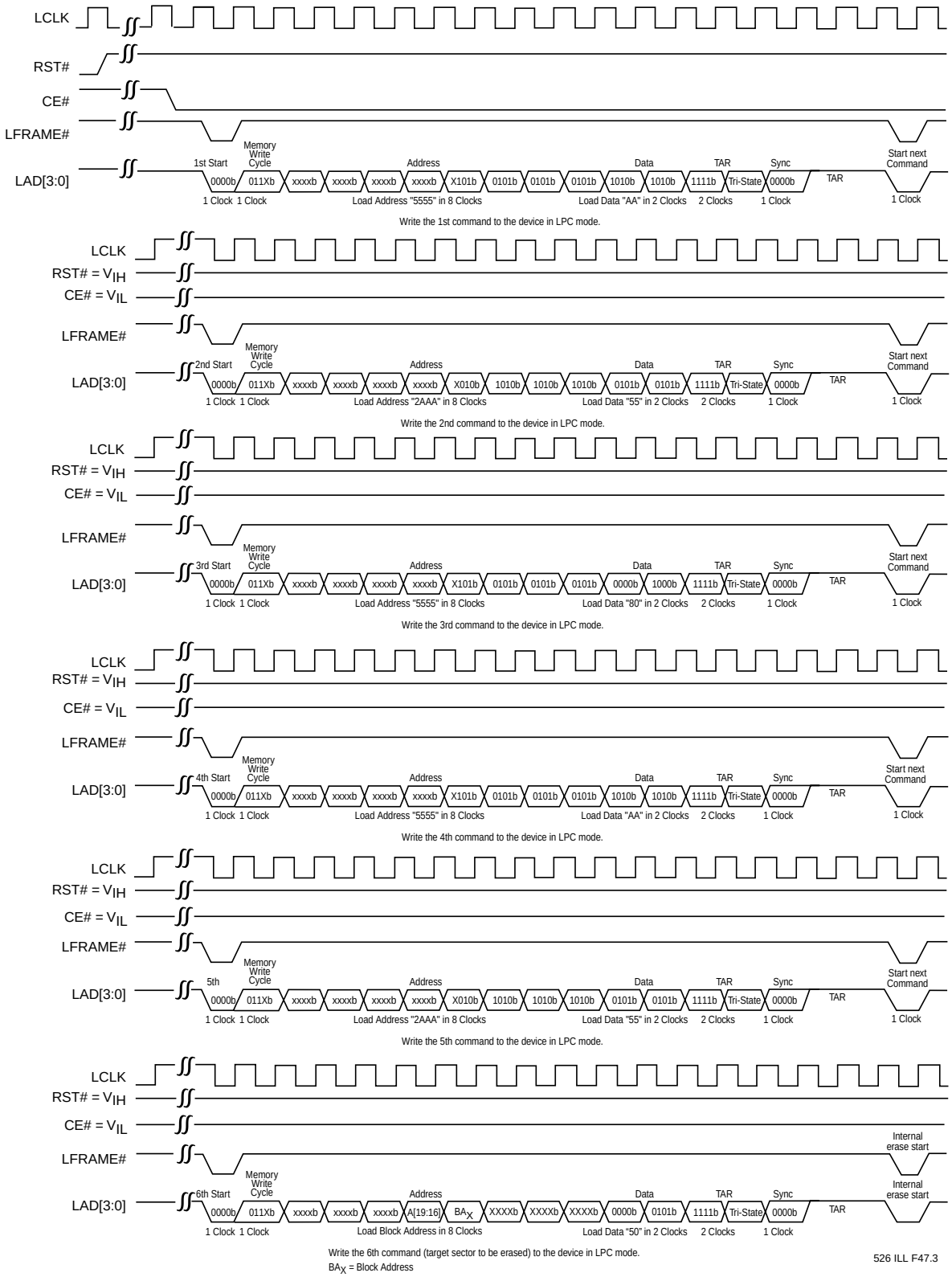
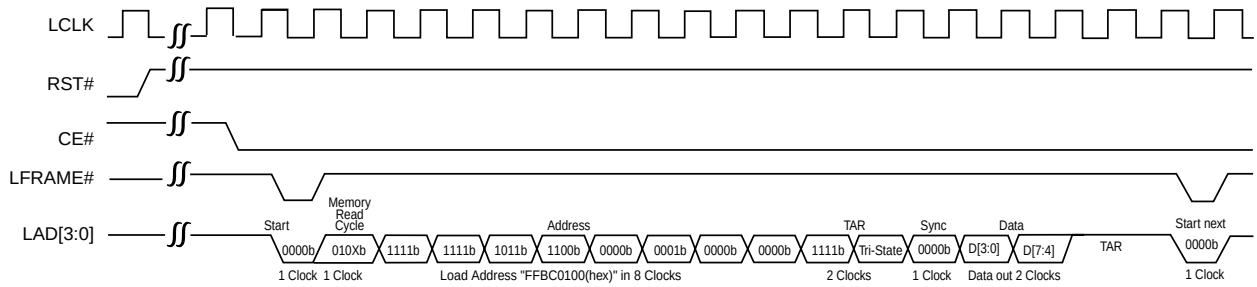


FIGURE 12: BLOCK-ERASE TIMING DIAGRAM (LPC MODE)



Note: Read the DQ[4:0] to capture the states (High or Low) of the GPI[4:0] input pins. The DQ[7:5] are reserved pins.

FIGURE 13: GPI REGISTER READOUT TIMING DIAGRAM (LPC MODE)

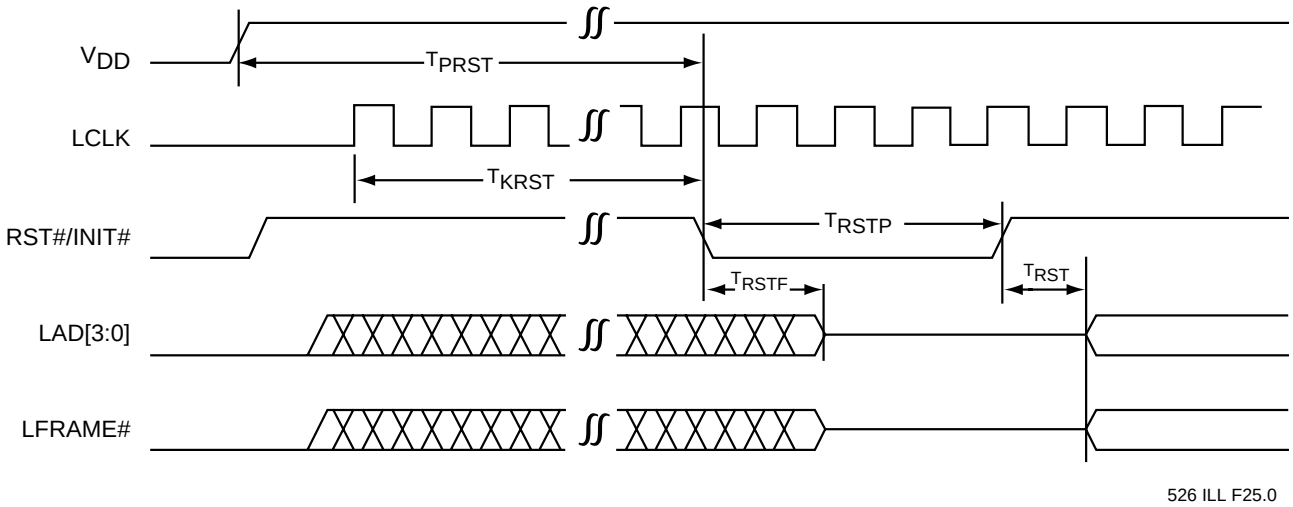


FIGURE 14: RESET TIMING DIAGRAM (LPC MODE)

AC CHARACTERISTICS (PP MODE)

TABLE 14: READ CYCLE TIMING PARAMETERS V_{DD}=3.0-3.6V (PP MODE)

Symbol	Parameter	Min	Max	Units
T_{RC}	Read Cycle Time	270		ns
T_{RST}	RST# High to Row Address Setup	1		µs
T_{AS}	R/C# Address Set-up Time	45		ns
T_{AH}	R/C# Address Hold Time	45		ns
T_{AA}	Address Access Time		120	ns
T_{OE}	Output Enable Access Time		60	ns
T_{OLZ}	OE# Low to Active Output	0		ns
T_{OHZ}	OE# High to High-Z Output		35	ns
T_{OH}	Output Hold from Address Change	0		ns

T14.1 526

TABLE 15: PROGRAM/ERASE CYCLE TIMING PARAMETERS V_{DD}=3.0-3.6V (PP MODE)

Symbol	Parameter	Min	Max	Units
T_{RST}	RST# High to Row Address Setup	1		µs
T_{AS}	R/C# Address Setup Time	50		ns
T_{AH}	R/C# Address Hold Time	50		ns
T_{CWH}	R/C# to Write Enable High Time	50		ns
T_{OES}	OE# High Setup Time	20		ns
T_{OEH}	OE# High Hold Time	20		ns
T_{OEP}	OE# to Data# Polling Delay		40	ns
T_{OET}	OE# to Toggle Bit Delay		40	ns
T_{WP}	WE# Pulse Width	100		ns
T_{WPH}	WE# Pulse Width High	100		ns
T_{DS}	Data Setup Time	50		ns
T_{DH}	Data Hold Time	5		ns
T_{IDA}	Software ID Access and Exit Time		150	ns
T_{BP}	Byte Programming Time		20	µs
T_{SE}	Sector-Erase Time		25	ms
T_{BE}	Block-Erase Time		25	ms
T_{SCE}	Chip-Erase Time		100	ms

T15.1 526

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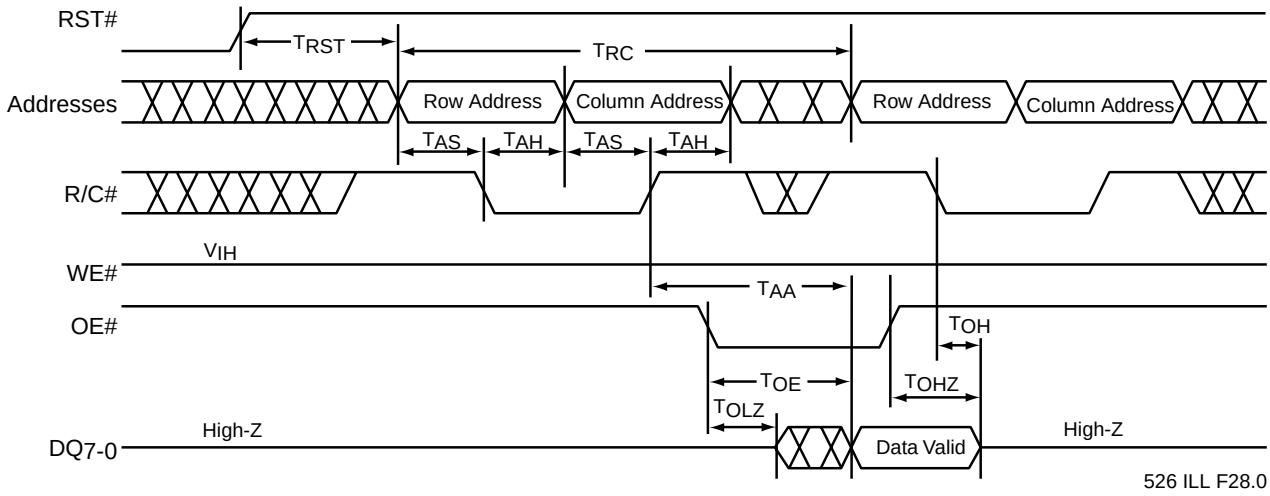


FIGURE 15: READ CYCLE TIMING DIAGRAM (PP MODE)

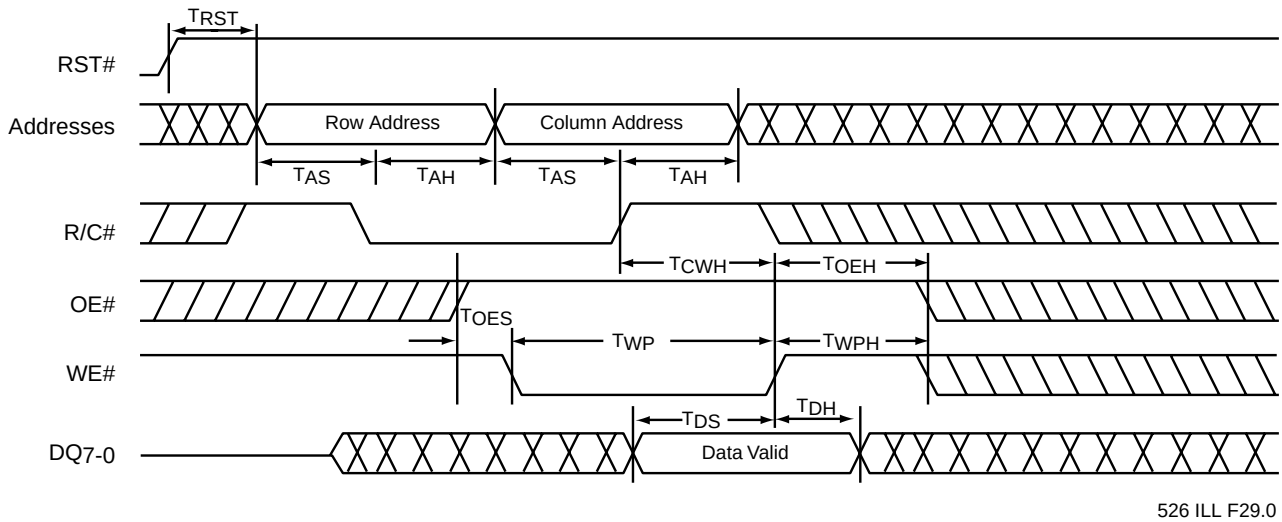


FIGURE 16: WRITE CYCLE TIMING DIAGRAM (PP MODE)

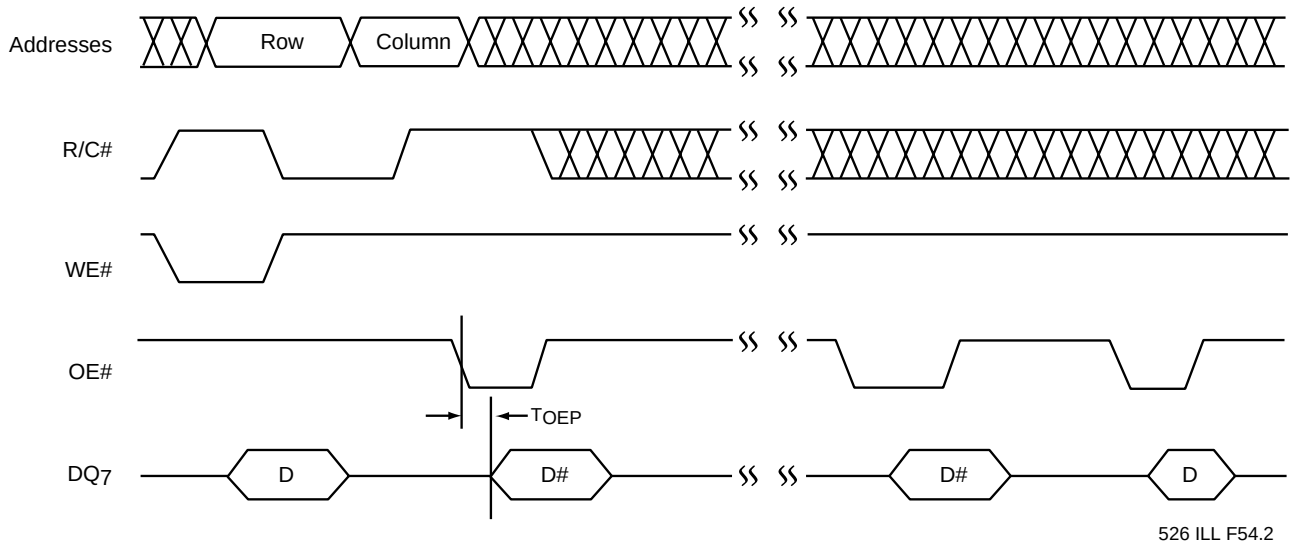


FIGURE 17: DATA# POLLING TIMING DIAGRAM (PP MODE)

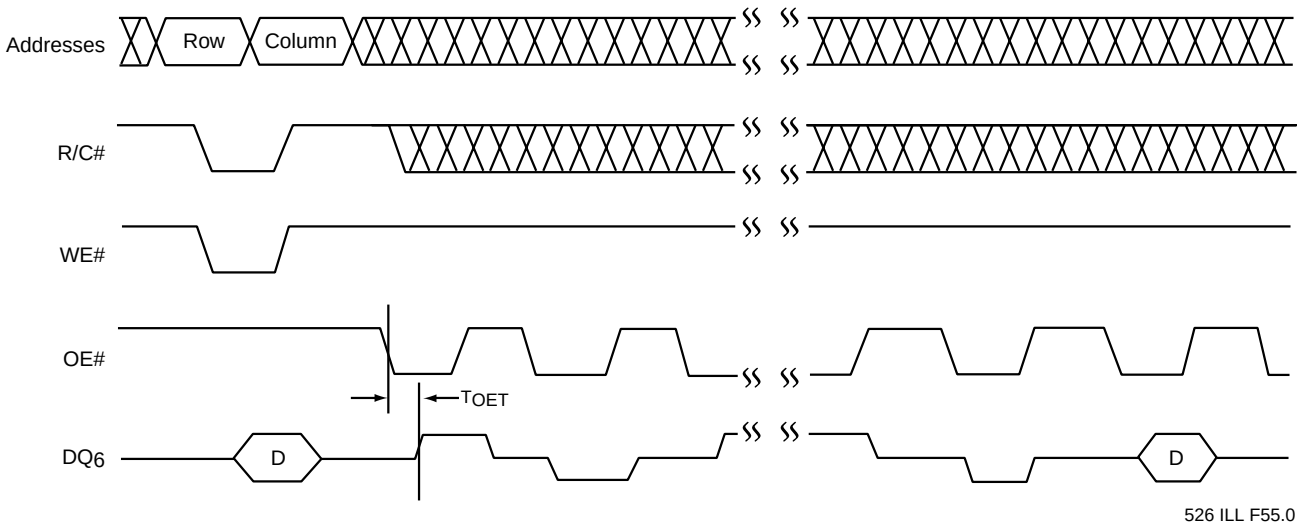


FIGURE 18: TOGGLE BIT TIMING DIAGRAM (PP MODE)

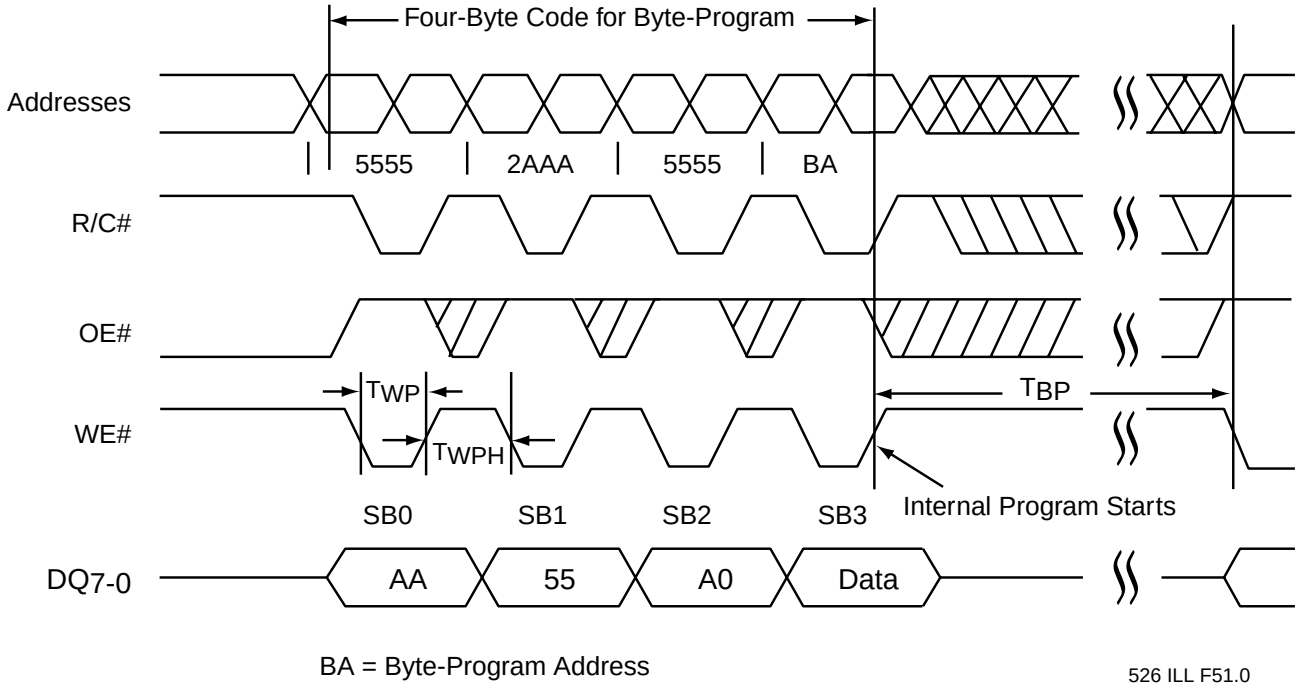


FIGURE 19: BYTE-PROGRAM TIMING DIAGRAM (PP MODE)

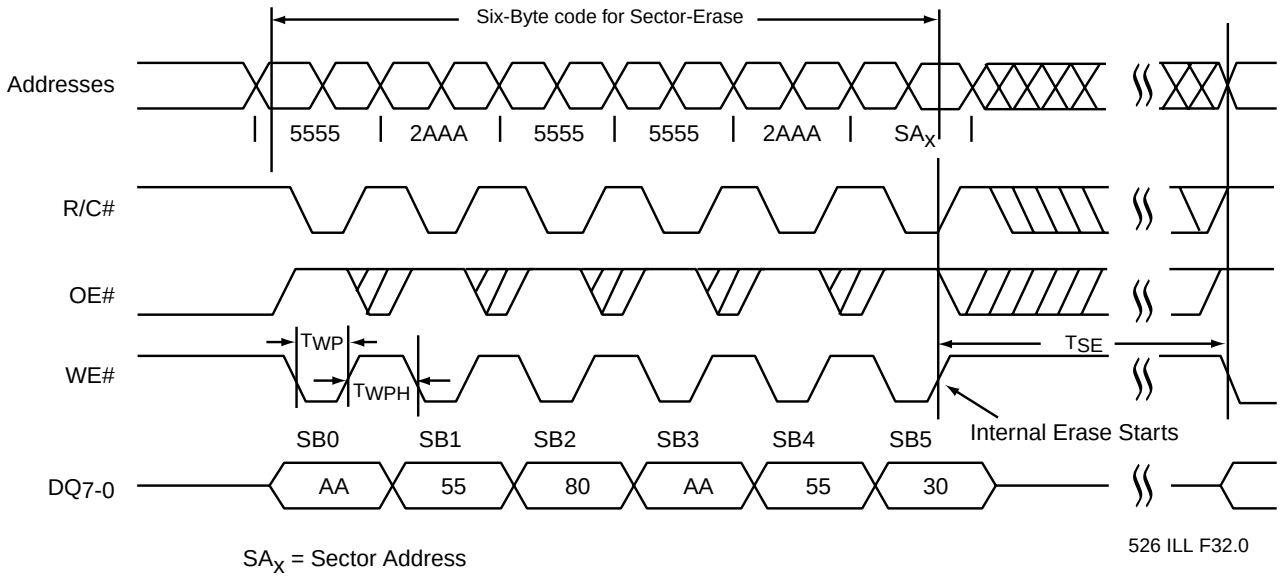
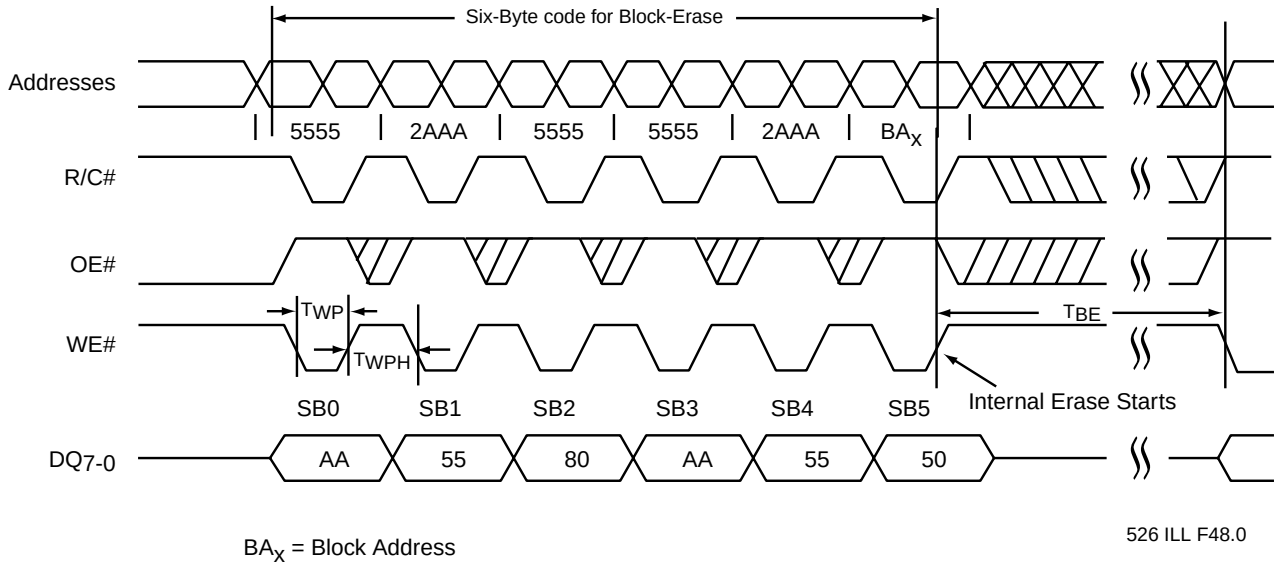


FIGURE 20: SECTOR-ERASE TIMING DIAGRAM (PP MODE)



BA_X = Block Address

FIGURE 21: BLOCK-ERASE TIMING DIAGRAM (PP MODE)

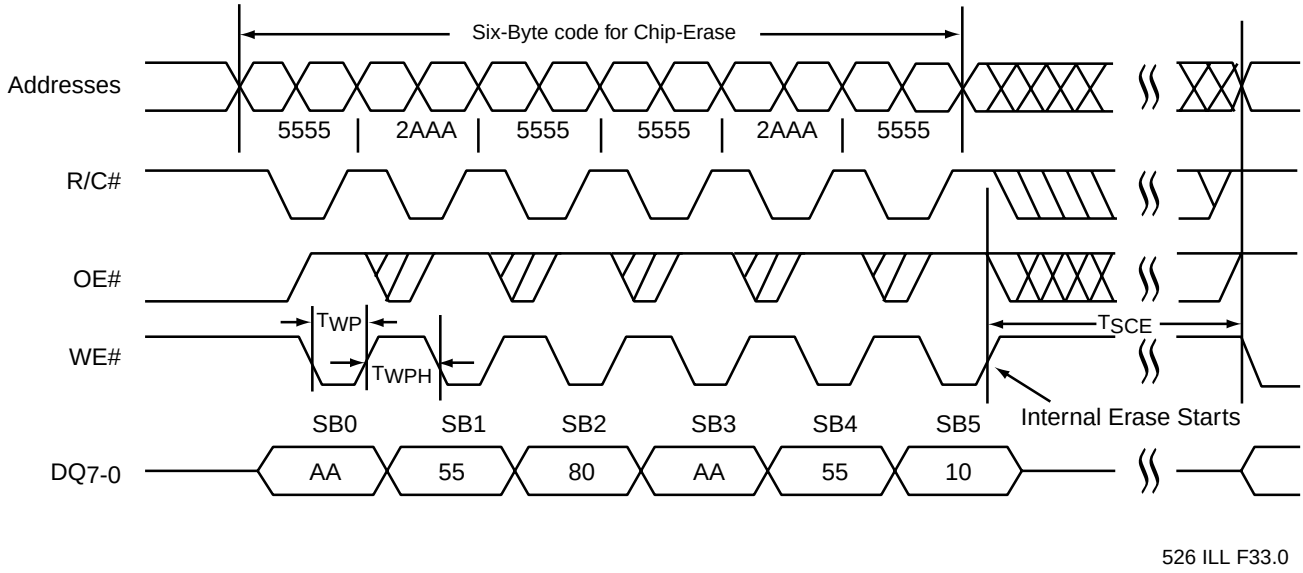


FIGURE 22: CHIP-ERASE TIMING DIAGRAM (PP MODE)

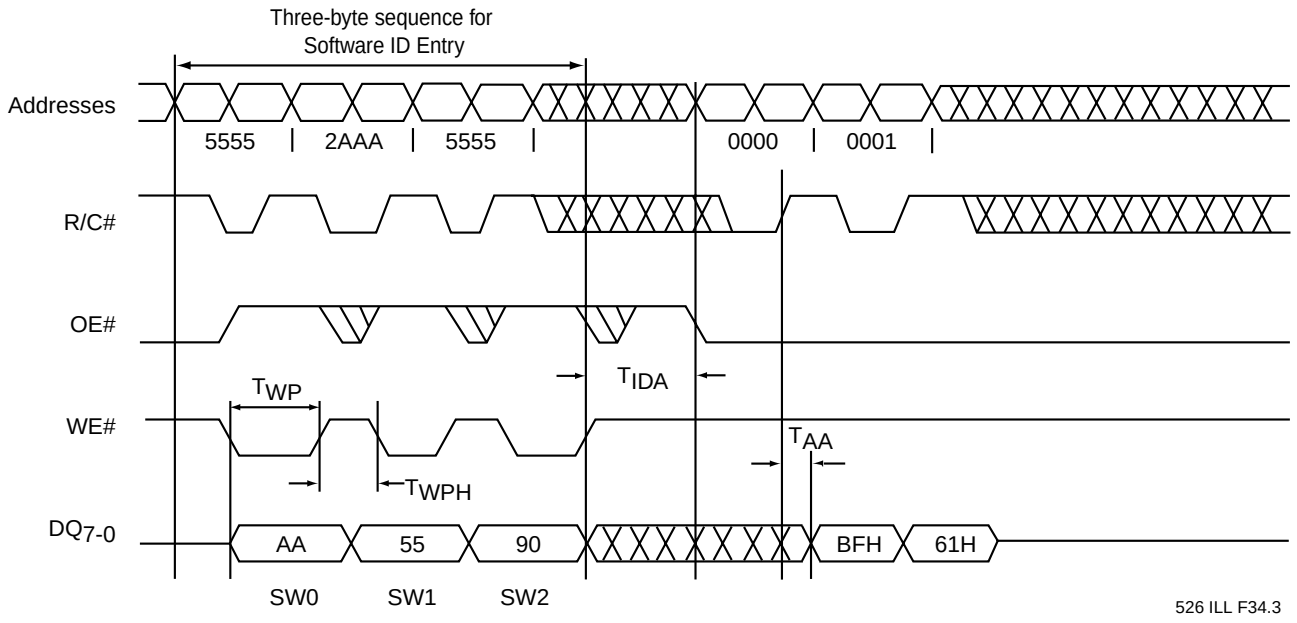


FIGURE 23: SOFTWARE ID ENTRY AND READ (PP MODE)

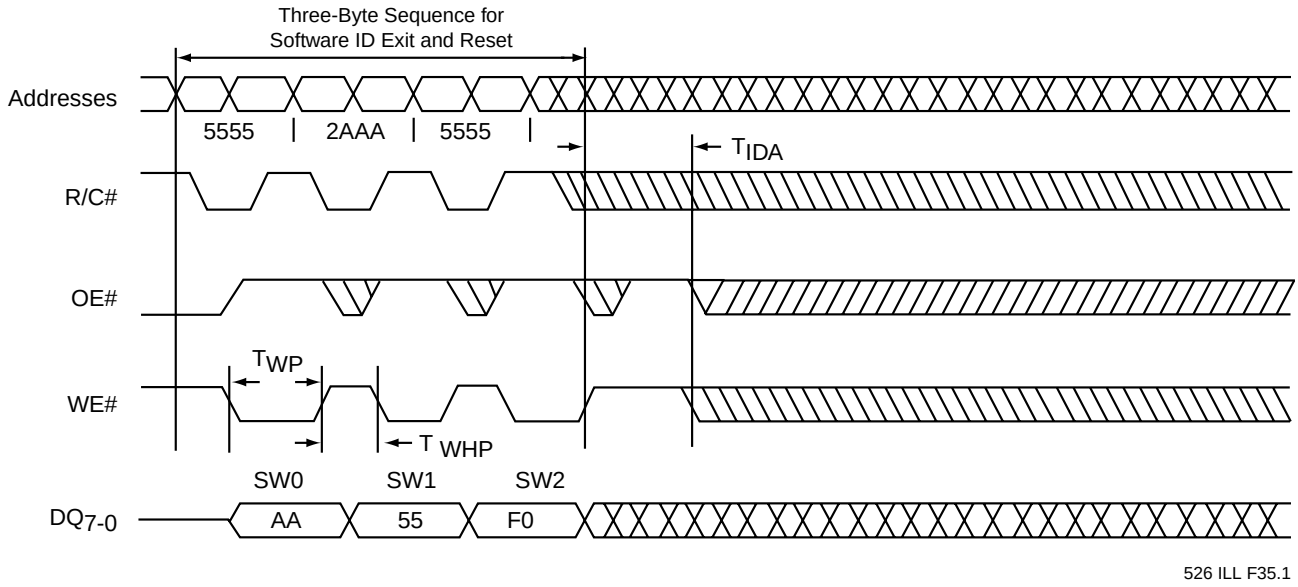
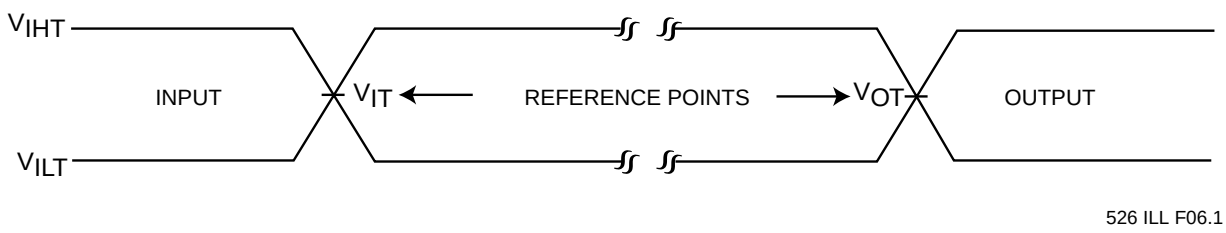


FIGURE 24: SOFTWARE ID EXIT AND RESET (PP MODE)



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.4 V_{DD}) and V_{OT} (0.4 V_{DD}). Input rise and fall times (10% ↔ 90%) are <3 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 25: AC INPUT/OUTPUT REFERENCE WAVEFORMS (PP MODE)

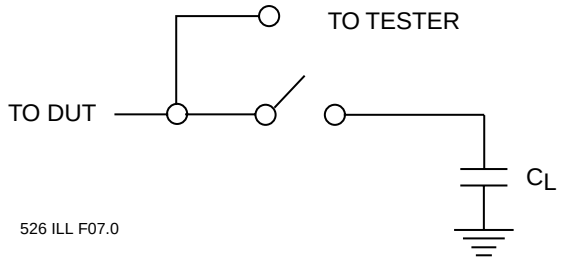


FIGURE 26: A TEST LOAD EXAMPLE

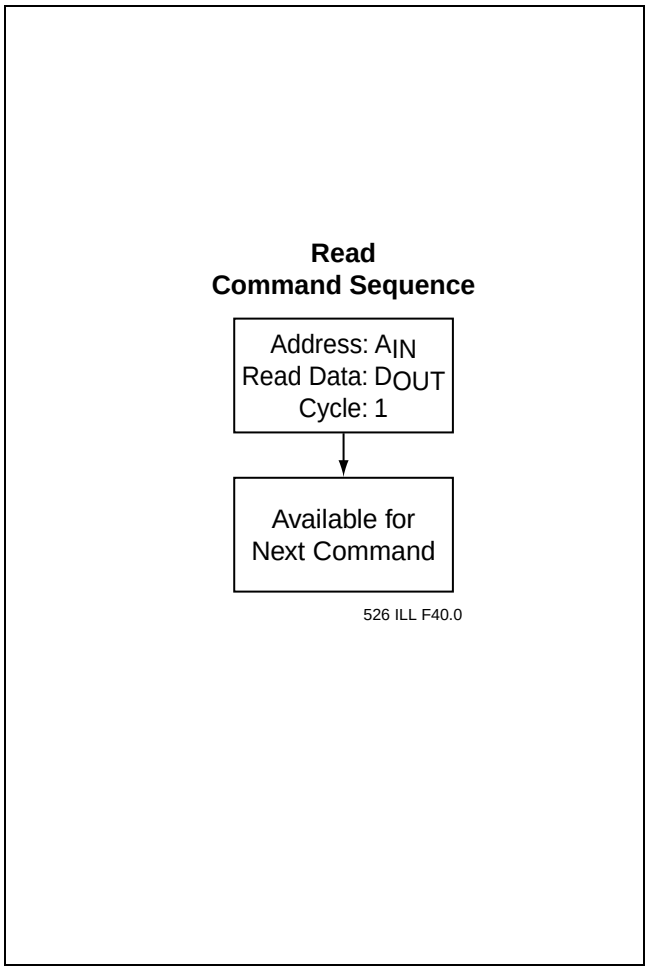


FIGURE 27: READ COMMAND SEQUENCE (LPC MODE)

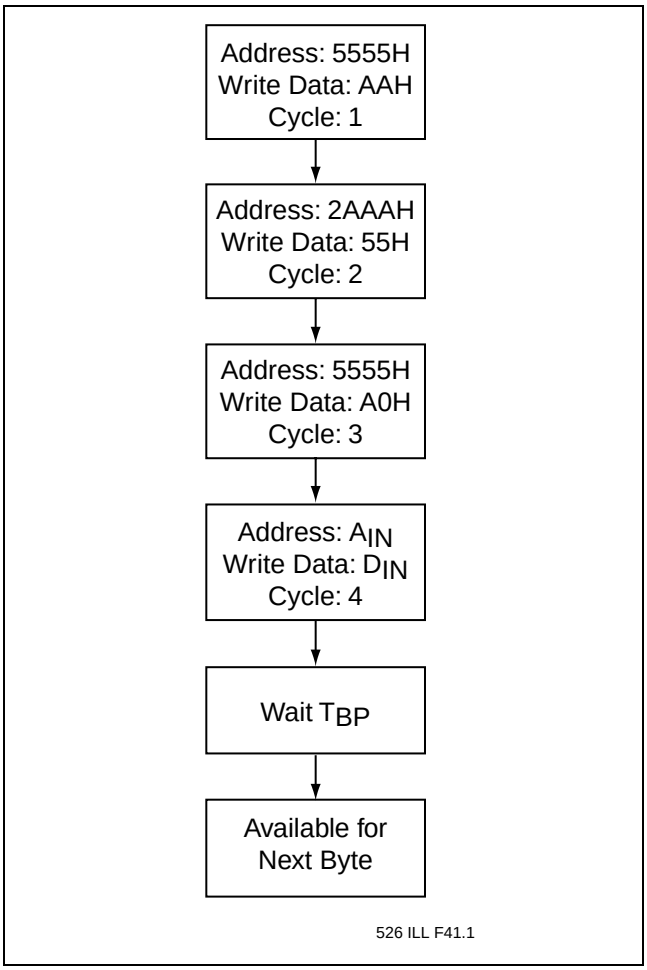


FIGURE 28: BYTE-PROGRAM ALGORITHM (LPC MODE)

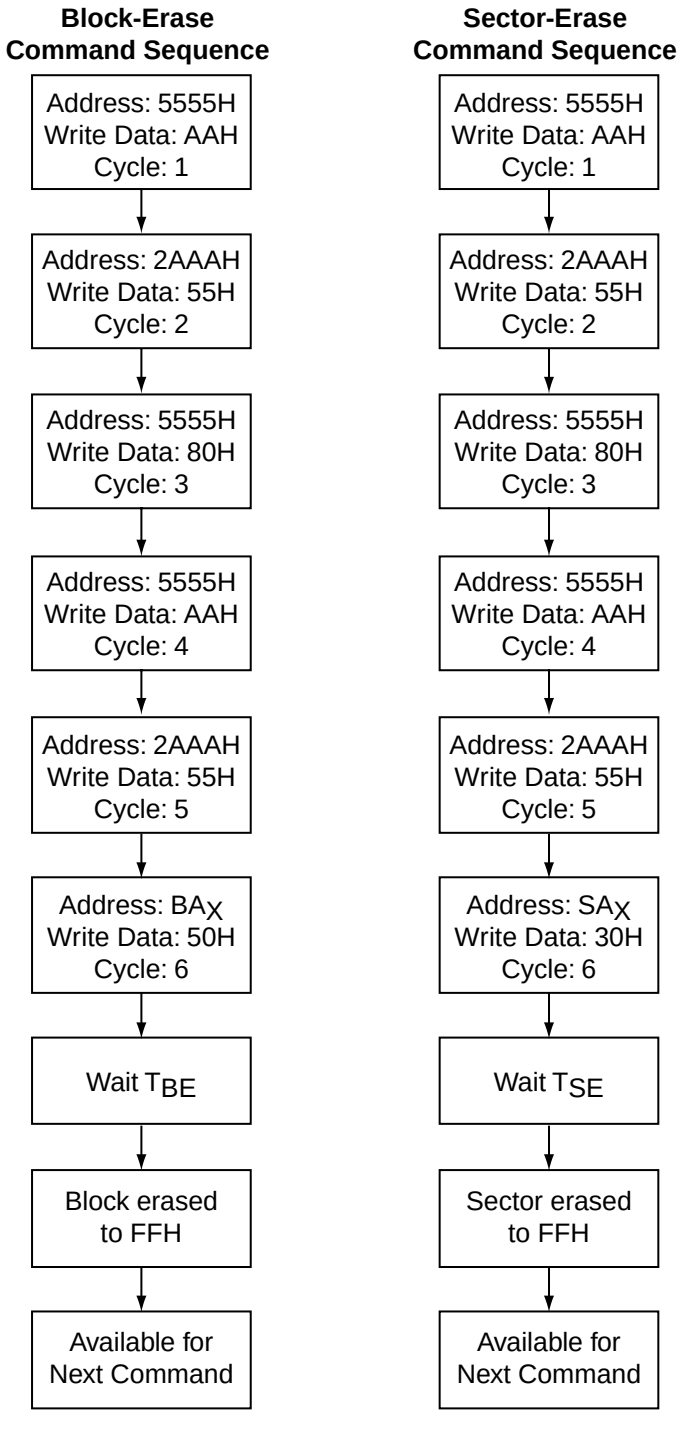


FIGURE 29: ERASE COMMAND SEQUENCES (LPC MODE)

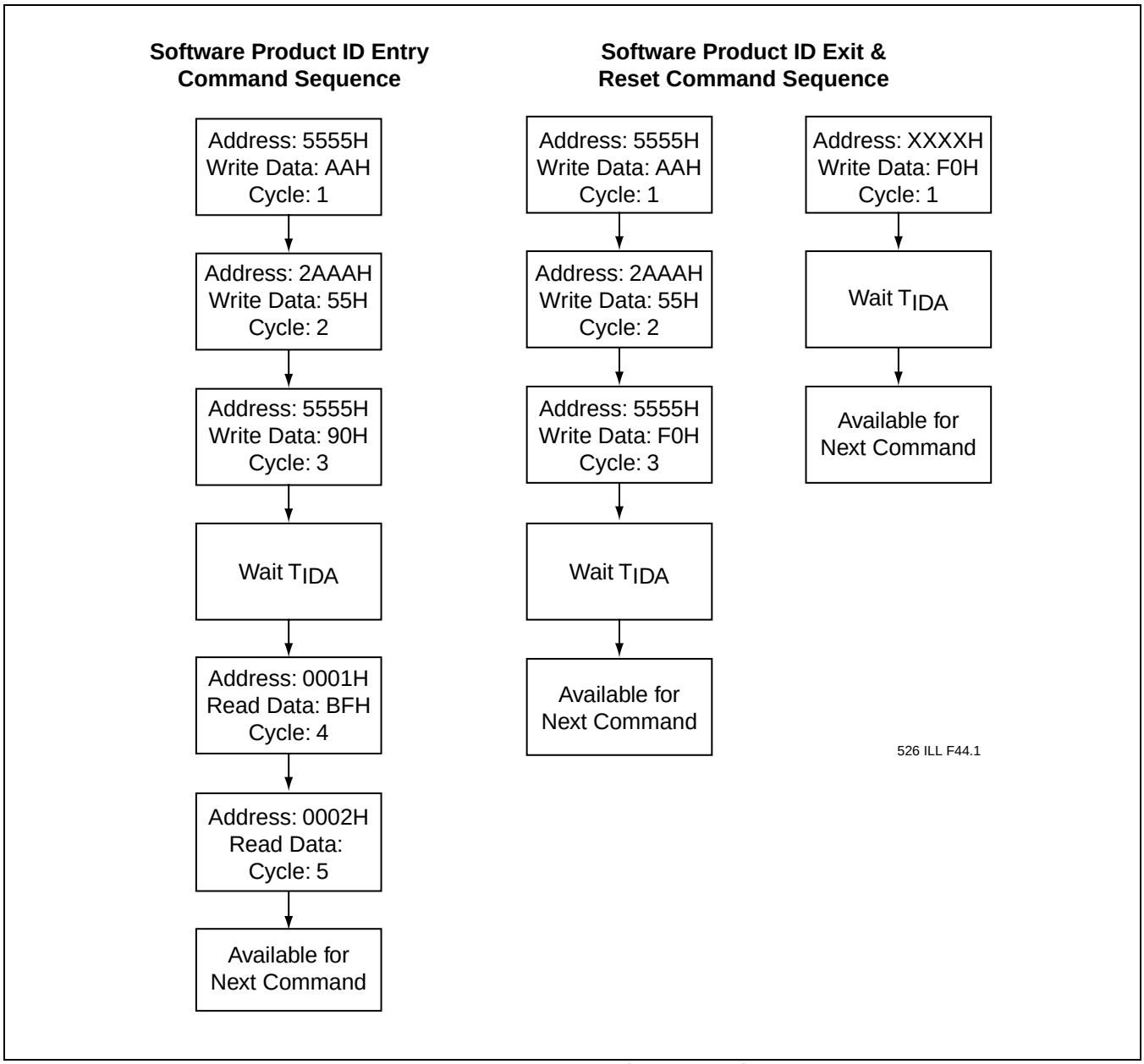


FIGURE 30: SOFTWARE PRODUCT COMMAND FLOWCHARTS (LPC MODE)

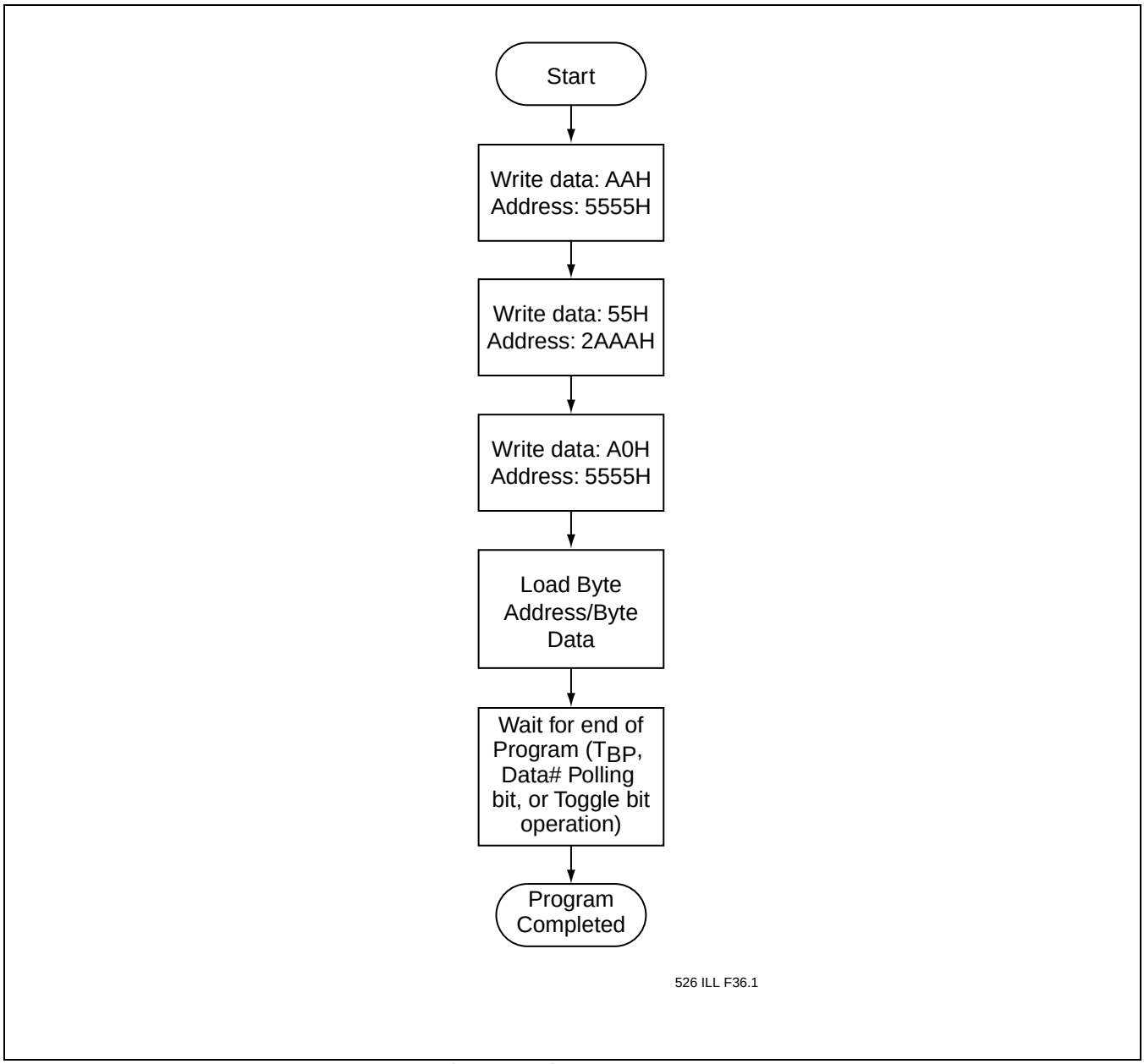


FIGURE 31: BYTE-PROGRAM ALGORITHM (PP MODE)

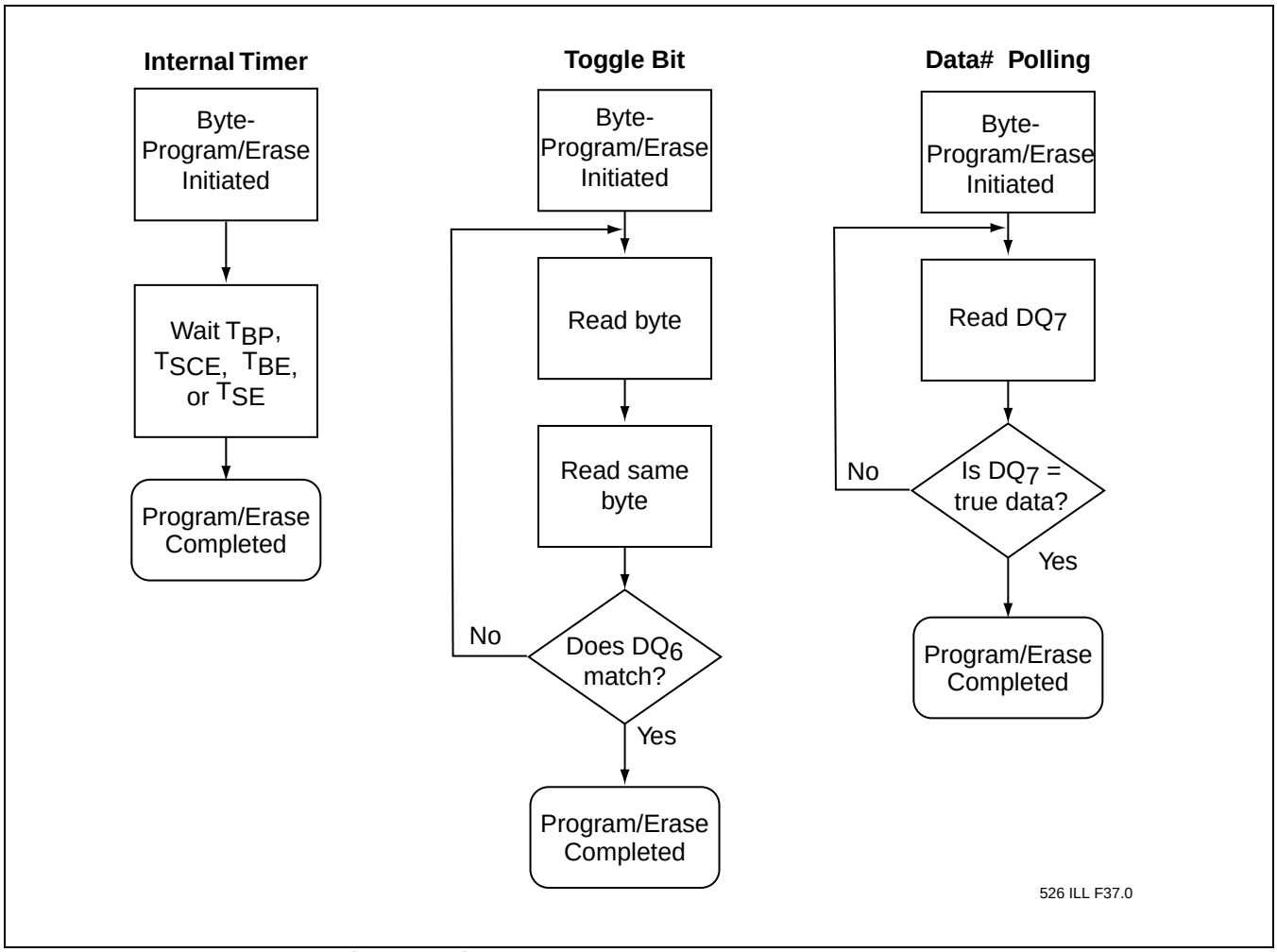


FIGURE 32: WAIT OPTIONS (PP MODE)

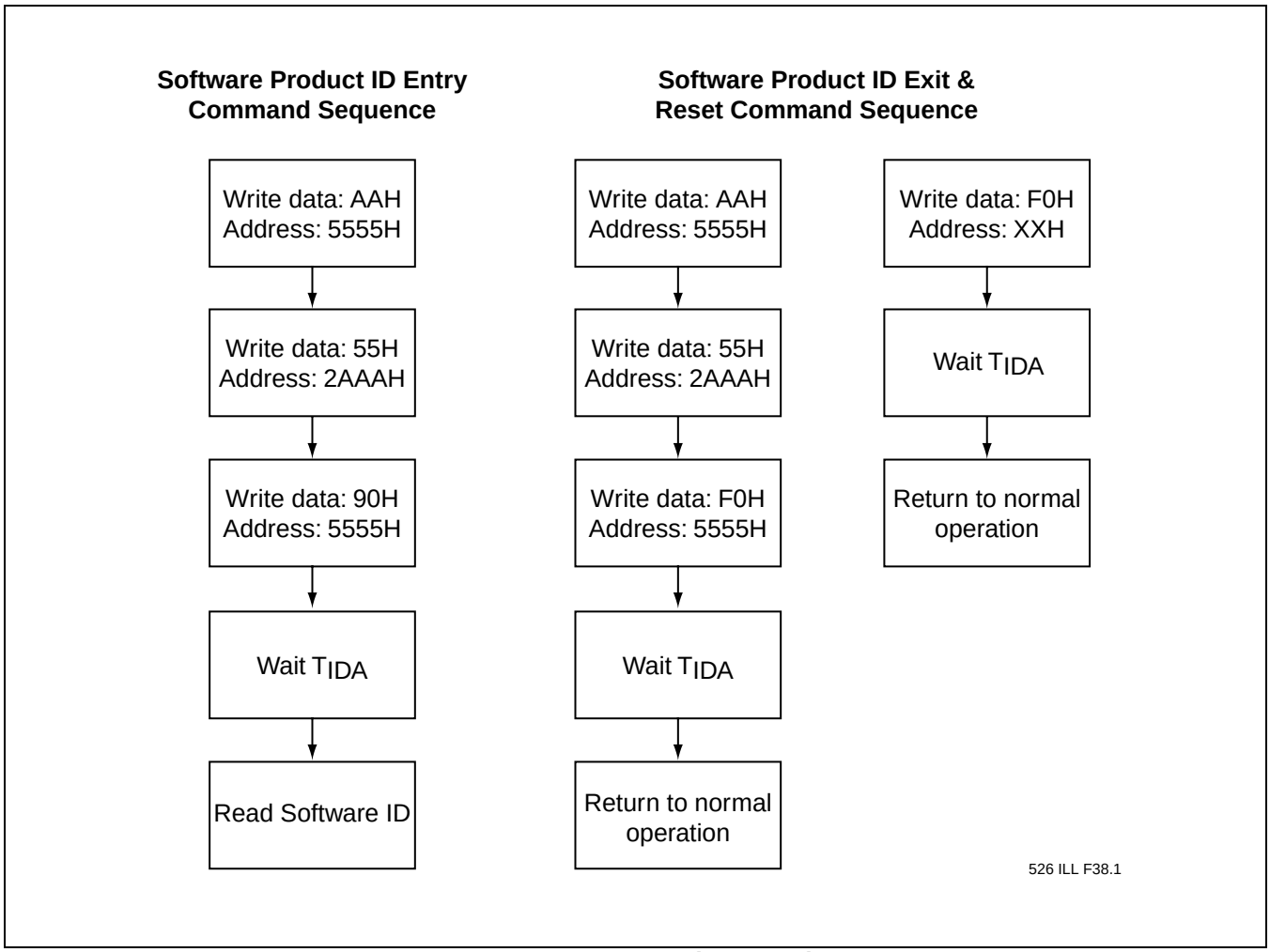


FIGURE 33: SOFTWARE PRODUCT COMMAND FLOWCHARTS (PP MODE)

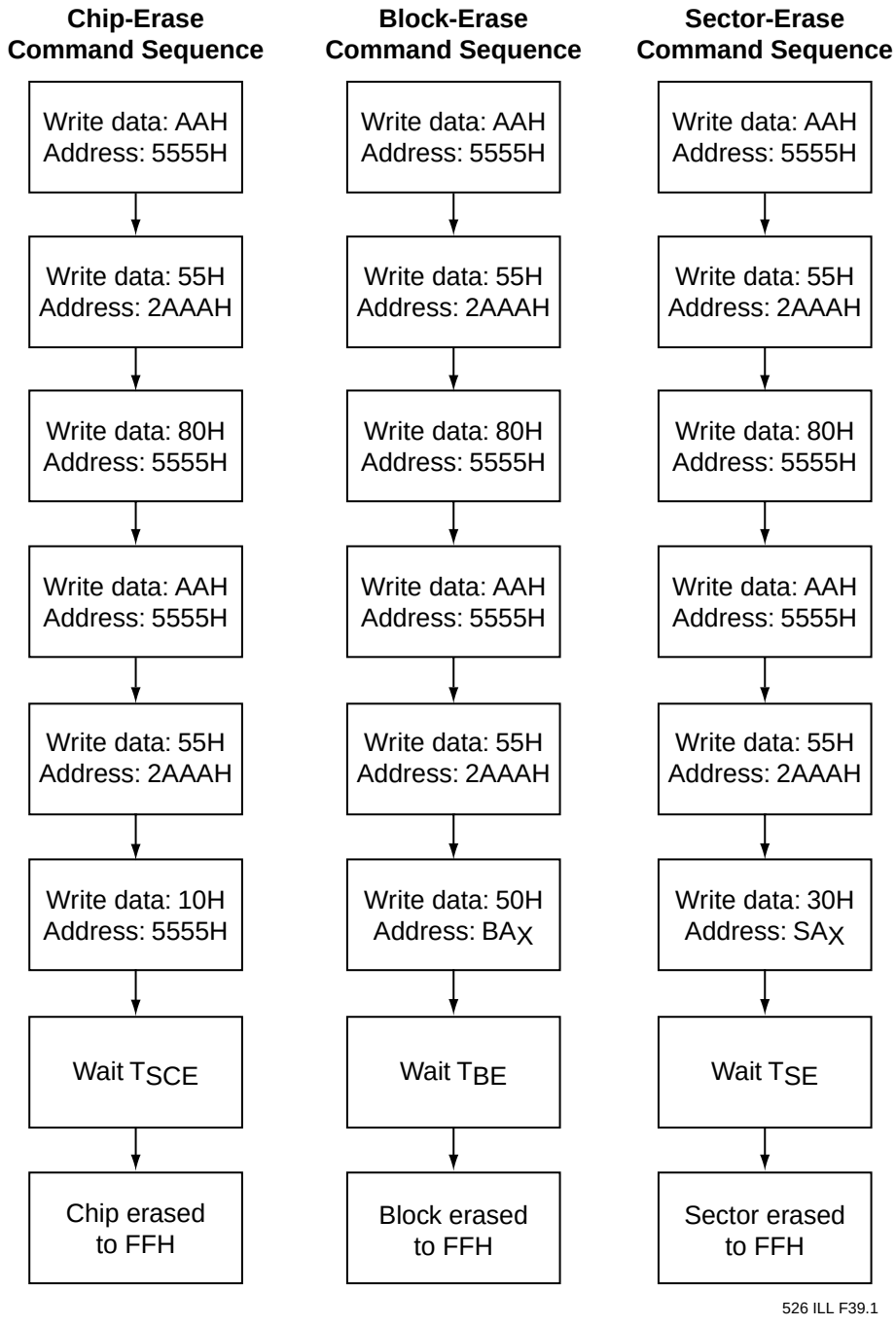
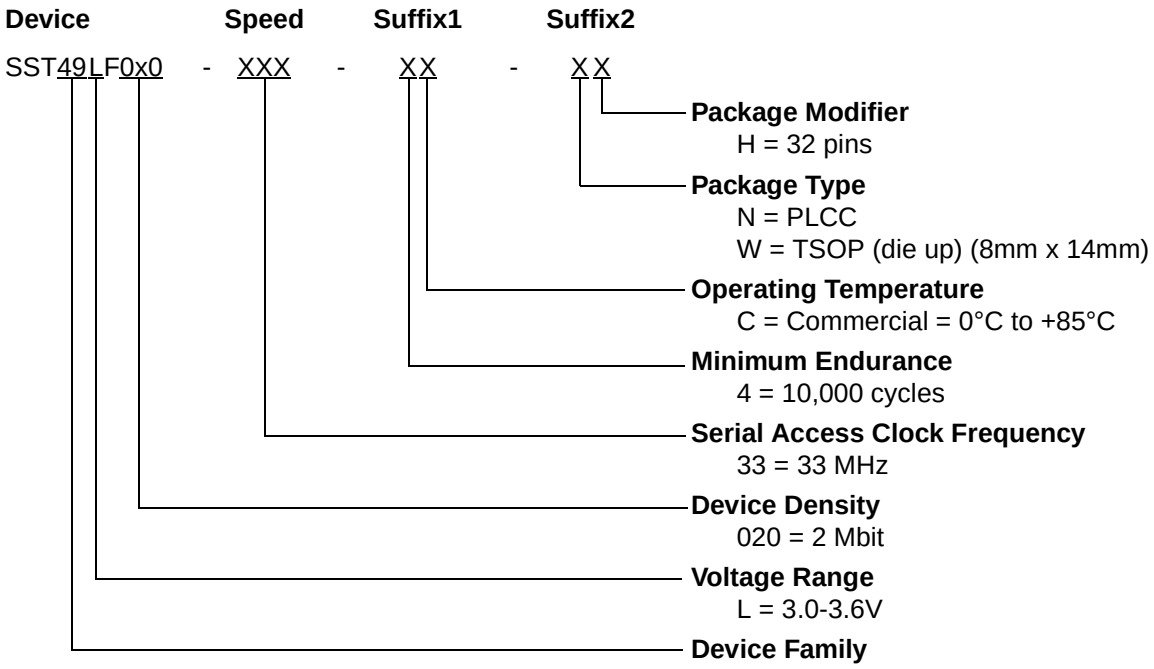


FIGURE 34: ERASE COMMAND SEQUENCE (PP MODE)

PRODUCT ORDERING INFORMATION

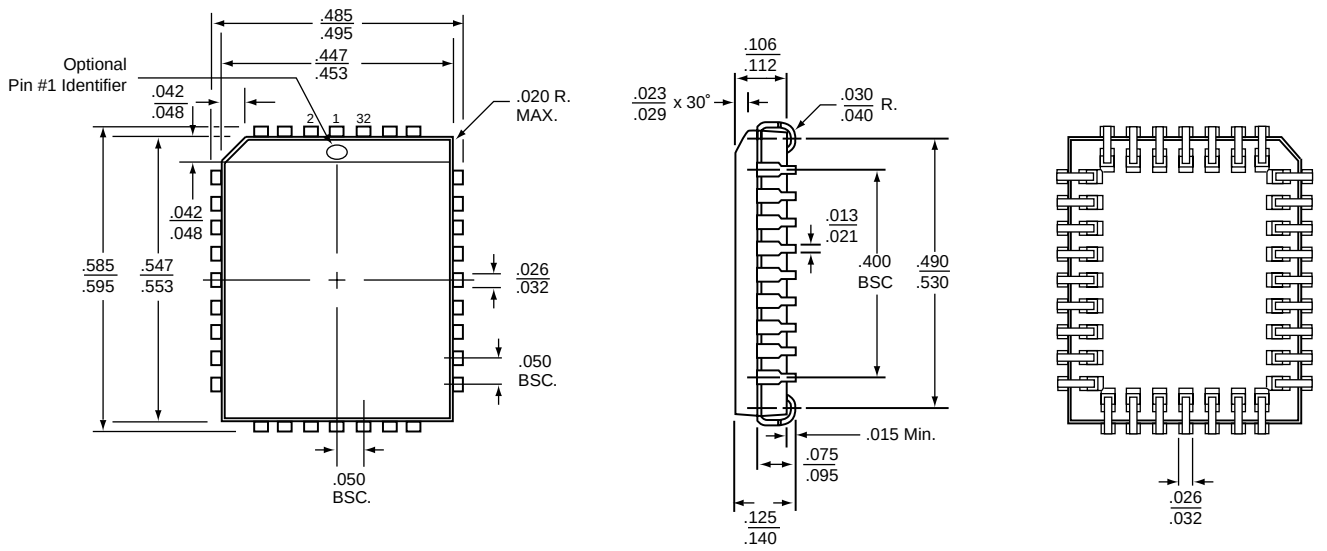


SST49LF020 Valid combinations

SST49LF020-33-4C-WH SST49LF020-33-4C-NH

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

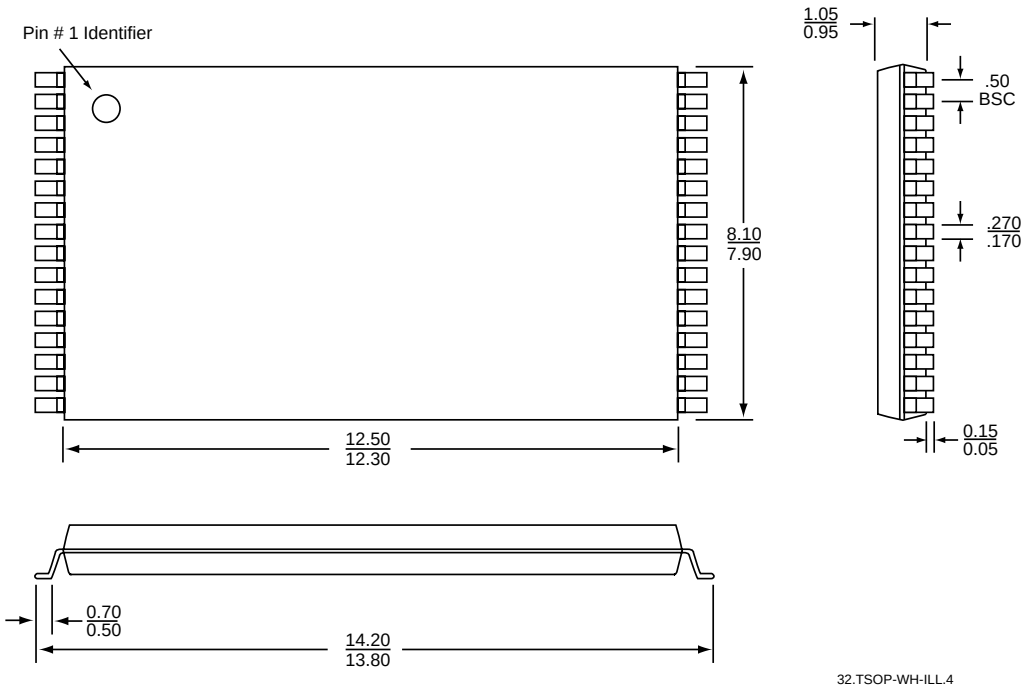
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: 4 mils.

32.PLCC.NH-ILL.2

32-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NH



Note:
1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (min/max).
3. Coplanarity: 0.1 (±.05) mm.
4. Maximum allowable mold flash is 0.15mm at the package ends, and 0.25mm between leads.

32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 14MM
SST PACKAGE CODE: WH

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