SIEMENS

Programmable Timer

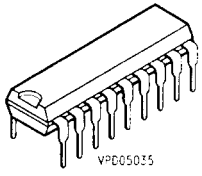
SAE 0530; SAE 0531; SAE 0532

Preliminary Data

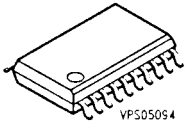
Bipolar IC

Features

- Direct operation from AC line or DC supply
- Time base: 50/60 Hz line frequency or any clock frequency up to 10 kHz
- Triac triggering with voltage synchronization for resistive loads, or with current synchronization for inductive and capacitive loads
- Triac gate trigger current up to 150 mA
- Continuous output current to relay actuation (max. 100 mA)
- Input and output delay can be retriggered
- 8 overlapping timing periods between 1 second and 32.5 hours
- Extended temperature range: – 25 to 85 °C



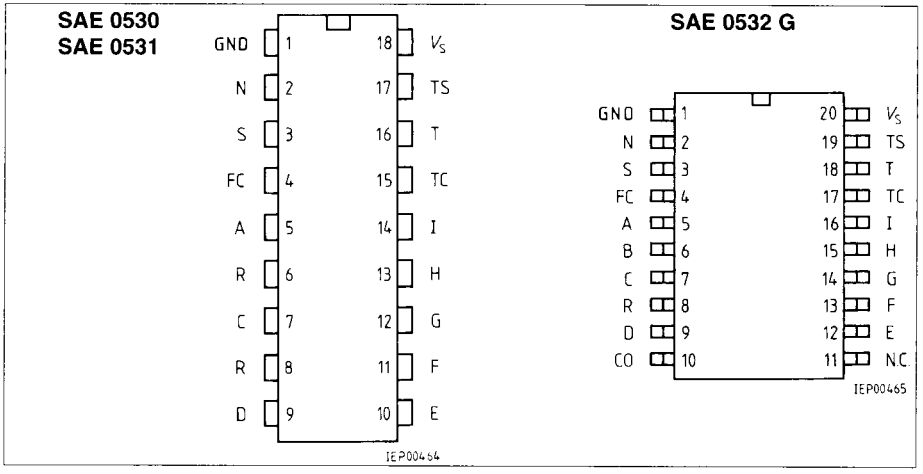
P-DIP-18-1



P-DSO-20-1

Type	Ordering Code	Package	Line Frequency
SAE 0530	Q67000-H8403	P-DIP-18-1	50 Hz
SAE 0531	Q67000-H8431	P-DIP-18-1	60 Hz
SAE 0532 G	Q67000-H8432	P-DSO-20-1 (SMD)	50/60 Hz

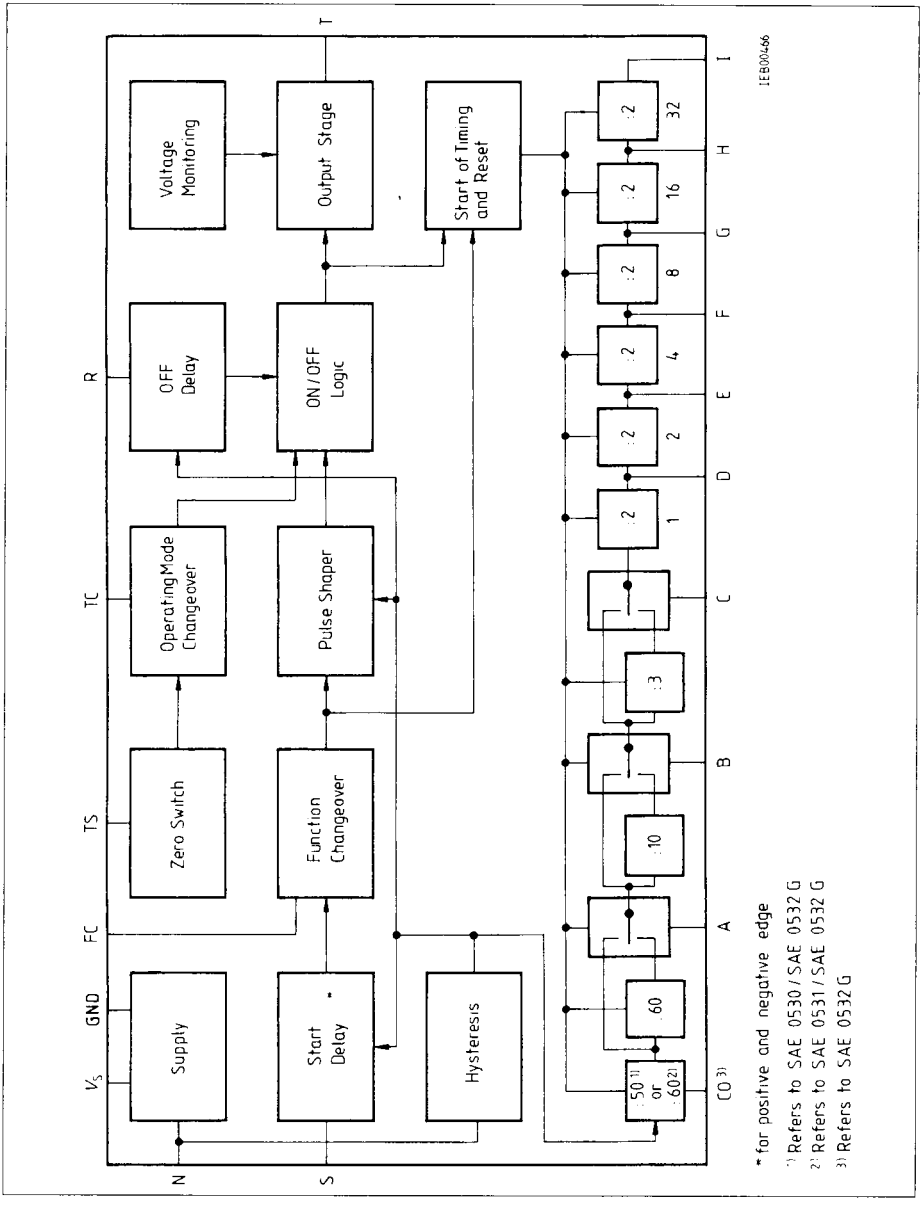
With these programmable timers (50 Hz, 60 Hz, 50/60 Hz, respectively) delay times between 1 second and 31.5 hours can be set. Among other purposes they serve for triggering triacs in an AC line. The power may be supplied either by the AC line or by a DC source. The time base is the line frequency. The versatile programmable timers can be imployed in a great variety of applications, such as electronic timers, cooking equipment control, espresso machines, hand driers, coin changing machines and slot machines, stairwell-light time switches, industrial controls, developing systems for photographic labs, automatic starters (to preheat car engines), and operating-hours counters.



Pin Configurations (top view)

Pin Definitions and Functions

SAE 0530 SAE 0531			SAE 0532 G		
Pin	**Symbol**	**Function**	**Pin**	**Symbol**	**Function**
1	GND	Circuit Ground	1	GND	Circuit Ground
2	N	Line voltage	2	N	Line voltage
3	S	Start	3	S	Start
4	FC	Function changeover	4	FC	Function changeover
5 6 7	A B C	Programming of basic timing unit	5 6 7	A B C	Programming of basic timing unit
8	R	Reset	8	R	Reset
9	D	Basic timing unit × 1	9	D	Basic timing unit × 1
10	E	Basic timing unit × 2	10	CO	50/60 Hz changeover
11	F	Basic timing unit × 4	11	N.C.	not connected
12	G	Basic timing unit × 8	12	E	Basic timing unit × 2
13	H	Basic timing unit × 16	13	F	Basic timing unit × 4
14	I	Basic timing unit × 32	14	G	Basic timing unit × 8
15	TC	Triac op. mode setting	15	H	Basic timing unit × 16
16	T	Triac triggering	16	I	Basic timing unit × 32
17	TS	Triac synchronization	17	TC	Triac op. mode setting
18	V_S	Positive supply voltage	18	T	Triac triggering
			19	TS	Triac synchronization
			20	VS	Positive supply voltage



Block Diagram

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Functional Description

Programming of Delay Times

On input N there is a Schmitt trigger for detecting the clock signal plus rectifier and Z-diodes for deriving the operating voltage from the clock source (e.g. line voltage).

The clock signal is applied to a basic divider (1:50 or 1:60) to generate a seconds clock from the line frequency, three switchable dividers (1:60, 1:10 and 1:3) for setting the basic timing and six 1:2 dividers with open-collector outputs. The set time will have expired when the appropriate outputs go high. The basic-timing dividers are controlled by the wiring of inputs A, B and C (and CO)*. At 50- or 60-Hz clock frequency it is possible to set the following basic timing:

Changeover (SAE 0532 G)

CO	Line Frequency
L	60 Hz
H	50 Hz

Timing Range	A	B	C	Basic Timing	Max. Time
1	L	L	L	1"	1'3"
2	L	L	H	3"	3'9"
3	L	H	L	10"	10'30"
4	L	H	H	30"	31'30"
5	H	L	L	1'	1h3'
6	H	L	H	3'	3h9'
7	H	H	L	10'	10h30'
8	H	H	H	30'	31h30'

L: connected to 0; H: connected to V_S

The basic timing of the set range is doubled in flipflops 1, 2, 4, 8, 16 and 32. The flipflops are connected to pins D, E, F, G, H and I so that the latter adopt a certain value, i.e. 1, 2, 4, 8, 16 and 32. The required delay time on output T (triac driver) is calculated by the following equation: delay = basic timing × value D through I. This time is then produced by connecting the appropriate pins D through I to pin R (reset). If a number of the outputs D through I are connected to R, the times add up.

* Information in parentheses apply to SAE 0532 G.

Output	Period	Contribution to Delay
D	2 × basic timing	1 × basic timing
E	4 × basic timing	2 × basic timing
F	8 × basic timing	4 × basic timing
G	16 × basic timing	8 × basic timing
H	32 × basic timing	16 × basic timing
I	64 × basic timing	32 × basic timing

Example:

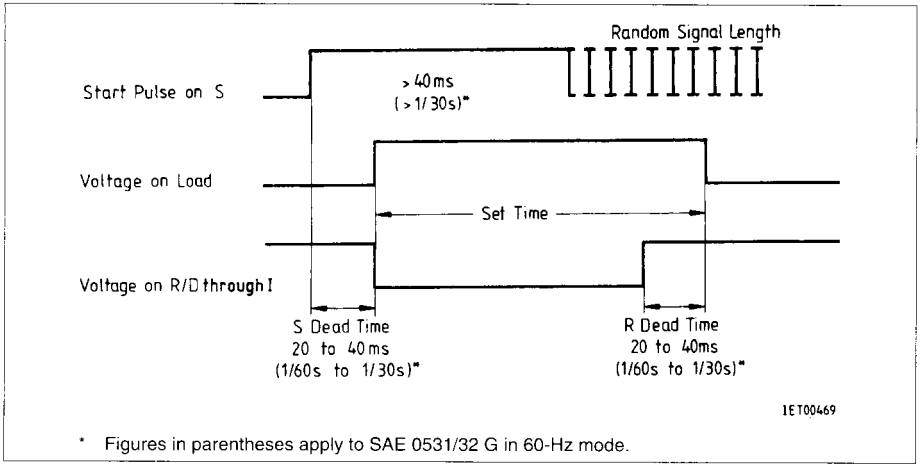
Line frequency 50 Hz (SAE 0530/31G) or 60 Hz (SAE 0531/32); set range 1 (basic timing = 1 s); D, F and I connected to R (value = 37): so the delay is 37 s.

Types of Delay

The circuit permits two different functions, which are selected on pin FC (function changeover). The two functions can be retriggered while the timing is running.

1. Turn-on interval DIN 46120 **(figure 1)**
   The triac connected to T turns on with the rising edge on the start input S and off when the set time has elapsed, and does this independently of the length of the start pulse. The effect of noise pulses on the start input is minimized by the dead times.
2. Dropout delay to DIN 46120 **(figure 2)**
   The triac turns on with the rising edge on S. The falling edge on S triggers the timing. The triac remains turned on until the set time has expired.

FC	Function
L	Turn-ON interval
H	Dropout delay



* Figures in parentheses apply to SAE 0531/32 G in 60-Hz mode.

Figure 1
Turn-ON Interval

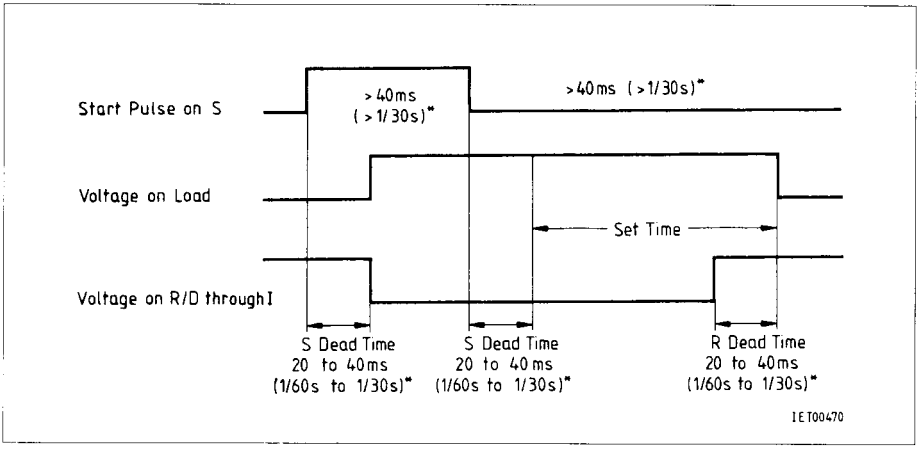


Figure 2
Dropout Delay

Start of Time Measurement (Figure 1, 2)

The frequency divider (and thus the time measurement) is started

- for the turn-on interval function (FC = L) with start input S = H by two negative edges on N,
- for the dropout delay function (FC = H) with S = H during at least two negative edges on N and then S = L by two more negative edges on N.

New Start of Time Measurement and Counter Reset

If, with the reset input R = L, the start input S is toggled (observing the condition: at least two negative edges on N), the time measurement is started again each time (retrigger function). When R = H and there are two negative edges on N, the counter is reset (reset function). This clocked control ensures a large degree of resistance to noise pulses that are coupled in. The reset function is also enabled by turning on the supply voltage, because the IC has a startup circuit. But this only takes effect if the preceding interruption of the supply voltage was long enough (in the region of a few ms). This avoids reset caused by interference on the supply voltage.

Output Stage

The output stage is also controlled by S and R. The open-collector output T is enabled by S = H and disabled by R = H when there are two negative edges on N (and when the supply voltage is turned on).

If start input S and reset input R are high at the same time, the output is enabled by the second negative edge and turned off again by the next positive edge (as long as R has not gone low in the meantime, as is usually the case). If the operating voltage drops below the operating limit of the circuit (approx. 3 V), the output is turned off for this duration.

Triac Modes (Figure 3, 4)

Different modes can be set for the enabled output by appropriate wiring of inputs TC (triac mode) and TS (triac synchronization):

- Mode 1 (TC on V_S) (voltage synchronization)
  Output T is connected to the zero-voltage switch. T conducts when $V_S - 1.3\ V \leq V_{TS} \leq V_S + 1.3\ V$; **see Application Circuit 1** (operation of resistive loads).
- Mode 2 (TC via C_e on GND or open) (current synchronization)
  Output T is connected to the zero-voltage switch via a monoflop. T issues a driving pulse, determined by C_e, when $V_S - 1.3$ V is no longer maintained on TS or $V_S + 1.3$ V is exceeded; **see Application Circuit 2.**
  In the current-synchronization mode, gate-trigger current is supplied to T until the triac has fired. If the triac does not fire because the load current is too small, the trigger current flows permanently, which can lead to a drop in the supply voltage. In this way the current is reduced further and the supply voltage continues to drop until ultimately the output is turned off because the lower limit of the operating voltage is reached. The circuit remains in this state until T is finally disabled by the timing control. This process can be avoided by ensuring that the triac fires in all operating conditions.
- Mode 3 (TC and TS on V_S)
  Output T conducts after the start pulse. This is used for any load in continuous driving of the triac (e.g. at low power levels) or if, instead of the triac, another load is operated; **see Application Circuits 3, 4 and 5.**

Inputs N, S, R, FC, A, B, C (and CO) * have an internal pullup resistor, i.e. they are high if not wired. On start input S there are also clamping diodes to V_S and GND so that it is possible to start with external potential. Reset input R is usually connected to one or more of the open-collector outputs D through I, enabling cutout of the load and resetting of the counter when the set delay has elapsed. These outputs are turned off (R = H) in their basic state (after reset), conduct when the time measurement starts (R = L) and are turned off again (R = H) after the delay **(see Figure 1 and 2)**.

* Figures in parentheses apply to SAE 0532 G.

Operation with Line Voltage

A series resistor R_S and a charging capacitor C_{ch} serve for line voltage supply. If a diode is connected in series with R_S (anode to N), the rms current consumption is halved. The series resistor may also be an RC network **(see Application Circuit 6).**

Operation with DC Voltage

This IC can also be operated with DC voltage or current
(see Application Circuits 4 and 5).

Useful Hints

- To obtain better noise immunity the pins D through I which are not connected are to be applied to GND.
- C_L
  If short-term line failures are to be compensated, C_L has to be accordingly higher.
- **Application Circuit 1** (voltage synchronization for resistive load)
  An average I_{TS} of 0.025 mA was inserted into the formula approximating R_{SYN}. As I_{TS+} and I_{TS-} contain production deviations, utilizing the determined R_{SYN} requires certain tolerances to be taken into account for pulse length Z.
- **Application Circuit 2** (current synchronization)
  In this circuit, an even shorter pulse length than determined for Z is sufficient to trigger the triac. This is possible by the trigger pulse being automatically repeated until the hold current is reached. Overdimensioning of Z for safety reasons is, therefore, not necessary. The disadvantage of multiple trigger pulses, however, is a somewhat larger interference band during the triggering. The noise band and/or the noise amplitude generated also depend on the amount of the gate trigger voltage necessary to trigger the triac after each current zero passage. That voltage is determined by the size of R_{SYN} and should not exceed 20 V.
- **Application Circuit 6**
  To limit the inrush current, R_{SS} has to be $\geq 0.2\ R_S$. Otherwise, the circuit might be destroyed.
- **Application Circuit 9**
  If the delay is made selectable by using a mechanical switch, it should be noted that all inputs, because of the pullup, are high in an unwired condition.
- Brief interruptions can be made ineffective by wiring with a capacitor. On S and R there is extra protection through the clocked control with a decision interval of one to two clock cycles.

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Pulse Diagrams for Triac Operating Modes 1 and 2

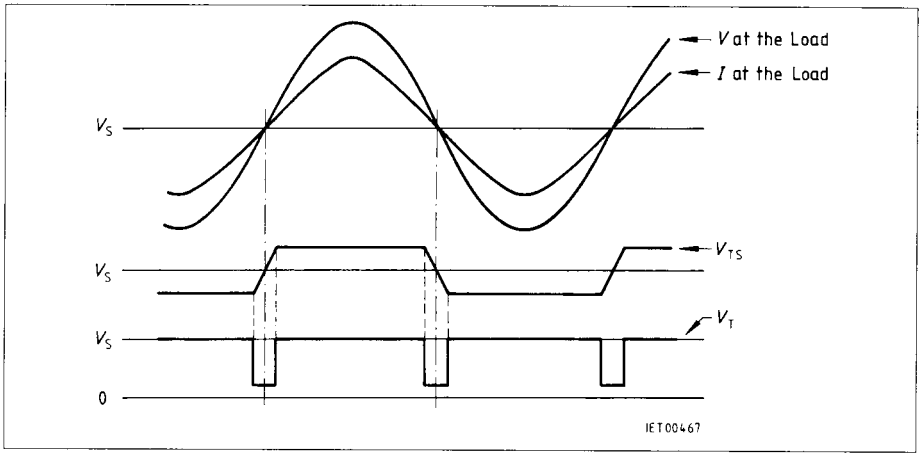


Figure 3
Operating Mode 1: Voltage Synchronization with Resistive Loads (TC at V_S)

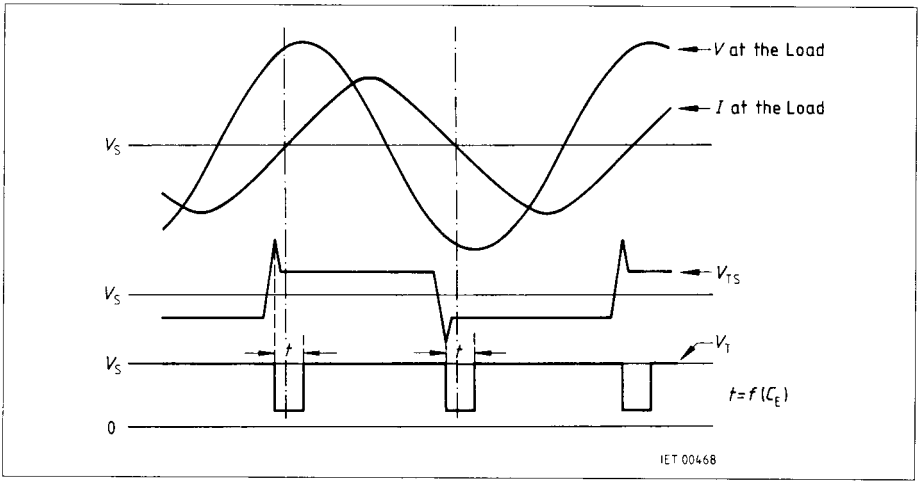


Figure 4
Operating Mode 2: Current Synchronization with Non-Resistive Loads
(Capacitance C_e at TC)

Absolute Maximum Ratings

T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage[1]	V_S	– 0.3	5.5	V	
AC at N[2]	$I_{N\,rms}$		35	mA	RMS value
DC from N[2]	$-I_N$	– 18	18	mA	Average value
Peak current at N[2]	I_{Np}	– 200	200	mA	2 ms, 100 ms interval
Voltage at A, B, C, FC, N, R, S, TC, CO	$V_{A...}$	– 0.3	V_S + 0.3	V	
Voltage at D, E, F, G, H, I, T	$V_{D...}$	– 0.3	20	V	D ... T off-state
Voltage at TS	V_{TS}	V_S – 0.7	V_S + 0.7	V	
Current in D, E, F, G, H, I	$I_{D...}$		0.5	mA	D ... I on-state
Current at S[3]	I_{IS}	– 2	2	mA	
Continuous current in T	I_T		100	mA	T on-state
Peak current in T	I_{Tp}		150	mA	1 ms/10 ms interval
Current at TS	I_{TS}	– 4	4	mA	
Junction temperature	T_j		125	°C	
Storage temperature range	T_{stg}	– 55	125	°C	
Thermal resistance system - air	$R_{th\,SA}$		70	K/W	P-DIP-18-1
	$R_{th\,SA}$		90	K/W	P-DSO-20

Operating Range

Supply voltage[4]	V_S	4.5	5.5	V	
Supply current (DC)[4]	$-I_N$	2.5	18	mA	[5]
Supply current (AC)[4]	$I_{N\,rms}$	5	35	mA	[5]
Ambient temperature	T_A	– 25	85	°C	

Notes

1) with impressed voltage at V_S

2) with impressed current at N

3) with impressed current at S

4) The IC can be operated with impressed voltage or with impressed current. With impressed voltage at V_S the voltage that is applied can be between 0 and $V_{S\,max}$ V (see maximum ratings). With impressed DC or AC at N, V_S is internally limited and thus ranges between 6 and 8.2 V (typ. 7.5 V). Operation, however, is also ensured if V_S falls to 4.5 V.

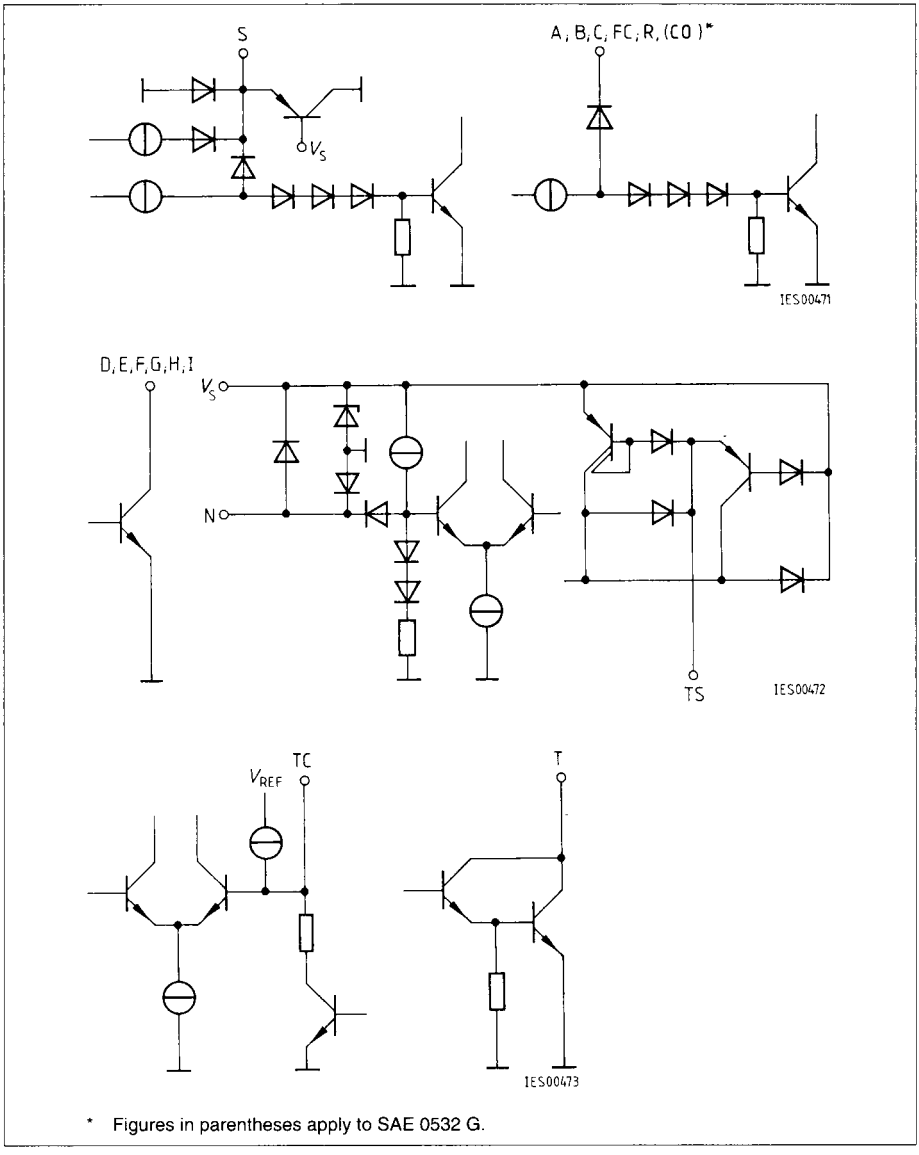
5) Only supply current for I_S, i.e. without triac gate current. The rms gate current additionally flows through N.

Characteristics

V_S = 5.5 V; T_A = 25 °C

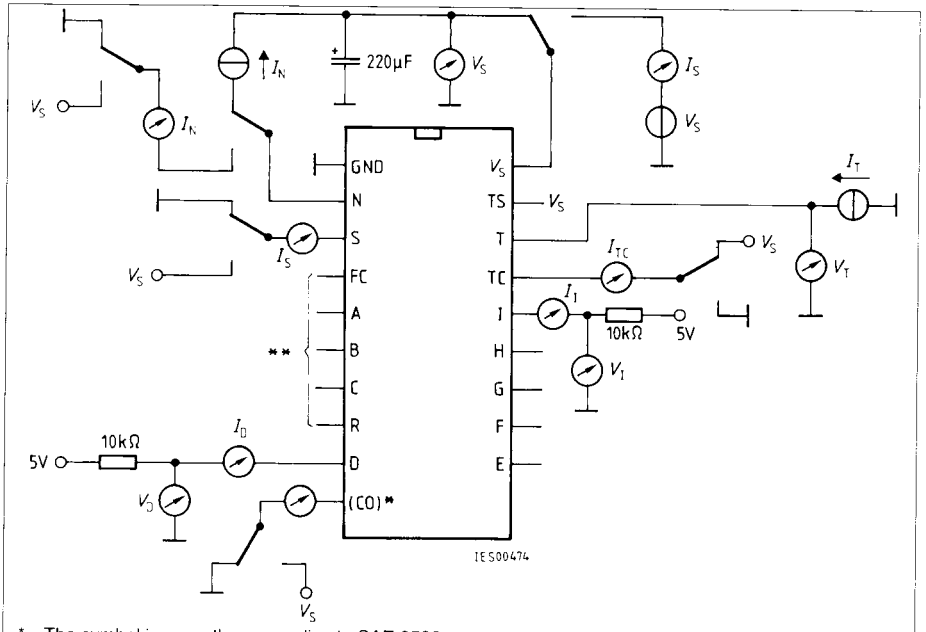
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Supply current [1]	I_S		1.6	2.5	mA	V_{IS} = 0 V	1
V_S (impressed DC) [2]	V_S		7.5	8.0	V	$-I_N$ = 2.5 mA	1
V_S (impressed AC) [2]	V_S		7.5	8.0	V	$I_{N\,rms}$ = 5 mA	1
Voltage at S [3]	V_{IS}		V_S + 0.9	V_S + 1.0	V	I_{IS} = 2 mA	
		−0.9	− 0.8		V	$-I_{IS}$ = 2 mA	
Switching threshold at A, B, C, S, FC, R, CO	$V_{A...}$	1.0	1.8	2.4	V		2
H-switching threshold at N [4]	V_N		1.8	2.4	V		2
L-switching threshold at N [4]	V_N	0.8	1.2		V		2
Switching hysteresis at N [4]	V_N	0.4	0.6	0.9	V		2
Switching threshold at TC (capacitor charge)	V_{TC1}	0.8	1.4	2.2	V		2
Switching threshold at TC	V_{TC2}	2.5	3.3	4.0	V		2
Switching threshold at TS	V_{TS+}		V_S + 1.3		V	$V_{TS} > V_S$	2
	V_{TS-}		V_S − 1.3		V	$V_{TS} < V_S$	2
L-input current at A, B, C, FC, R, CO	$-I_{A...}$		20	35	µA	$V_{A...}$ = 0 V	1
L-input current at S	$-I_{IS}$		60	105	µA	V_{IS} = 0 V	1
L-input current at N [4]	$-I_N$		40	70	µA	V_N = 0 V	1
H-input current at A, B, C, S, FC, R, CO	$I_{A...}$			1	µA	$V_{A...} = V_S$	1
H-input current at N [4]	I_N			1	µA	$V_N = V_S$	1
H-input current at TC	I_{TC}		20	45	µA	$4.5 \le V_{TC} \le V_S$	1
L-input current at TC	I_{TC}		20	45	µA	V_{TC} = 0 V	1
Pos. switch-over current at TS	I_{TS+}	10	25	40	µA	R_{SYN} = 0	2
Pos. switching hysteresis at TS	I_{Hy+}	0.3	1.0	4	µA	R_{SYN} = 0	2
Neg. switch-over current at TS	I_{TS-}	10	25	40	µA	R_{SYN} = 0	2
Neg. switching hysteresis at TS	I_{Hy-}	0.3	1.0	4	µA	R_{SYN} = 0	2
L-voltage at D, E, F, G, H, I	$V_{D...}$		0.15	0.4	V	$I_{D...}$ = 0.5 mA	1
H-reverse current at D, E, F, G, H, I	$I_{D...}$			1	µA		1
L-output voltage at T	V_Q		0.7	1.0	V	I_T = 1 mA	1
	V_Q		0.8	1.2	V	I_T = 10 mA	1
	V_Q		1	1.5	V	I_T = 100 mA	1

[1] with impressed voltage at V_S
[2] with impressed current at N
[3] with impressed current at S
[4] if N is clock input



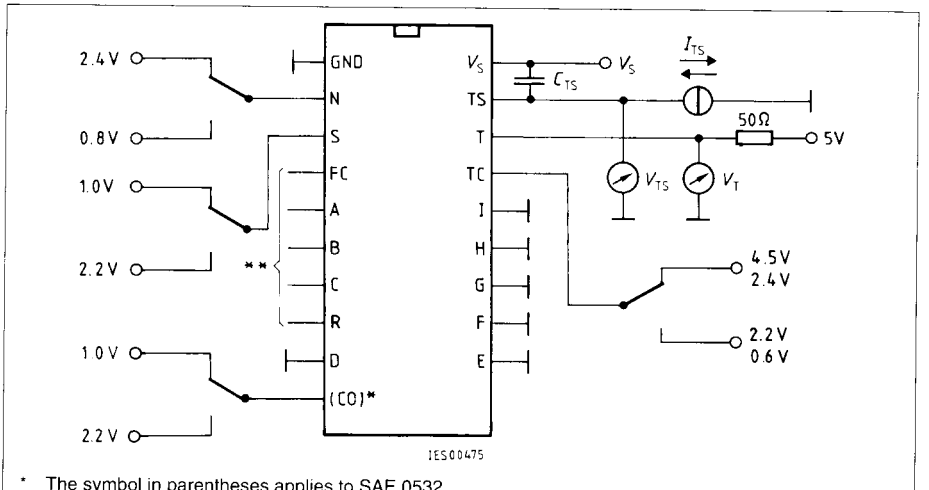
* Figures in parentheses apply to SAE 0532 G.

Internal Wiring of Inputs/Outputs and Supply Pins



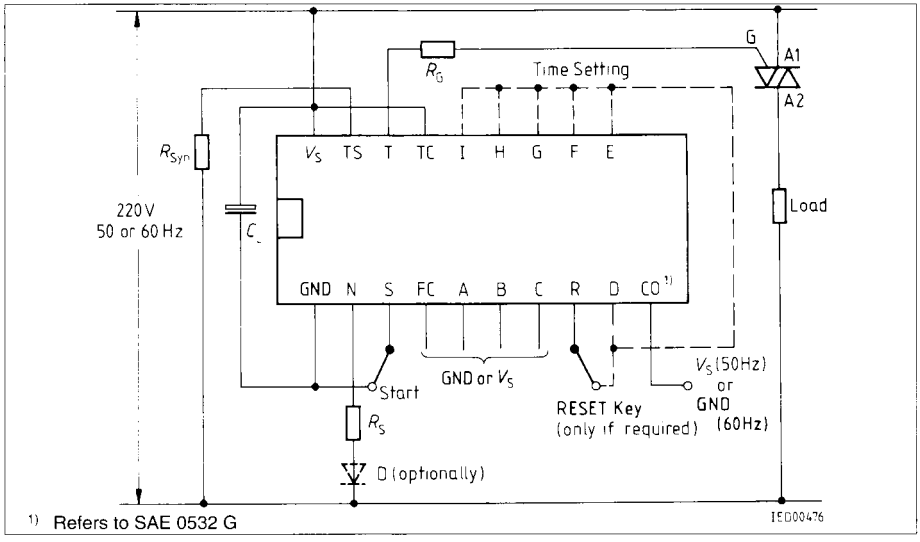
* The symbol in parentheses applies to SAE 0532.
** The external wiring of pins FC to R equals to that of pin S (Test Circuit 1)

Test Circuit 1

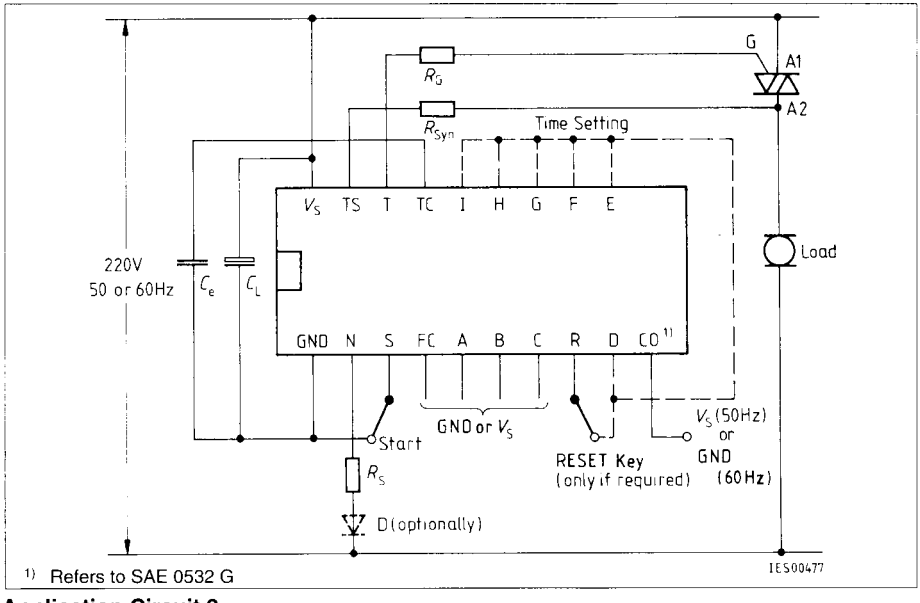


* The symbol in parentheses applies to SAE 0532.
** The external wiring of pins FC to R equals to that of pin S (Test Circuit 2)

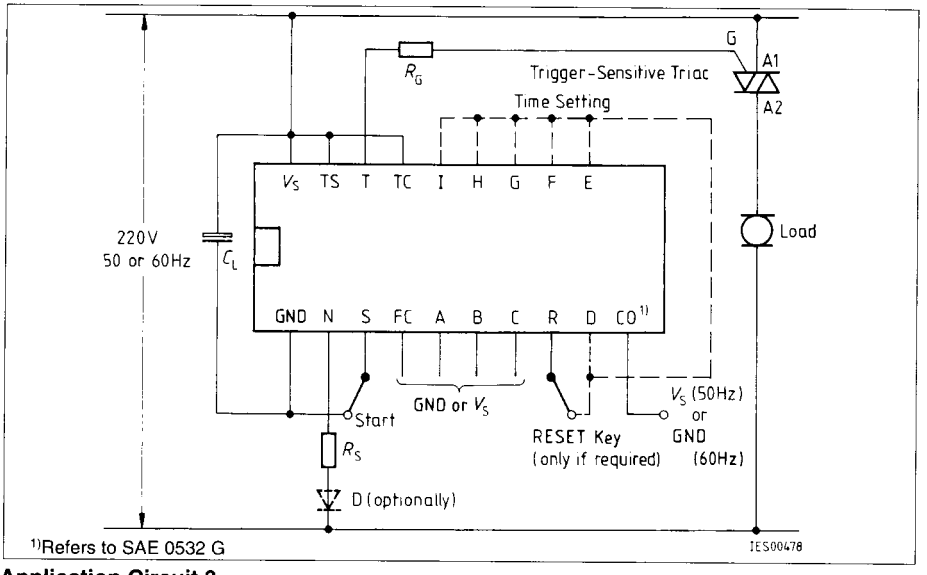
Test Circuit 2



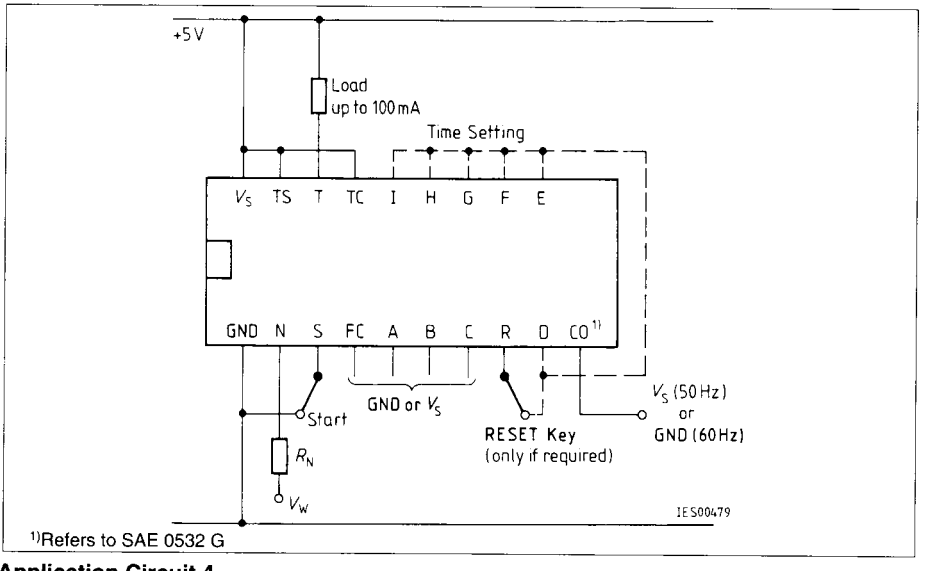
Application Circuit 1
Operation with resistive load



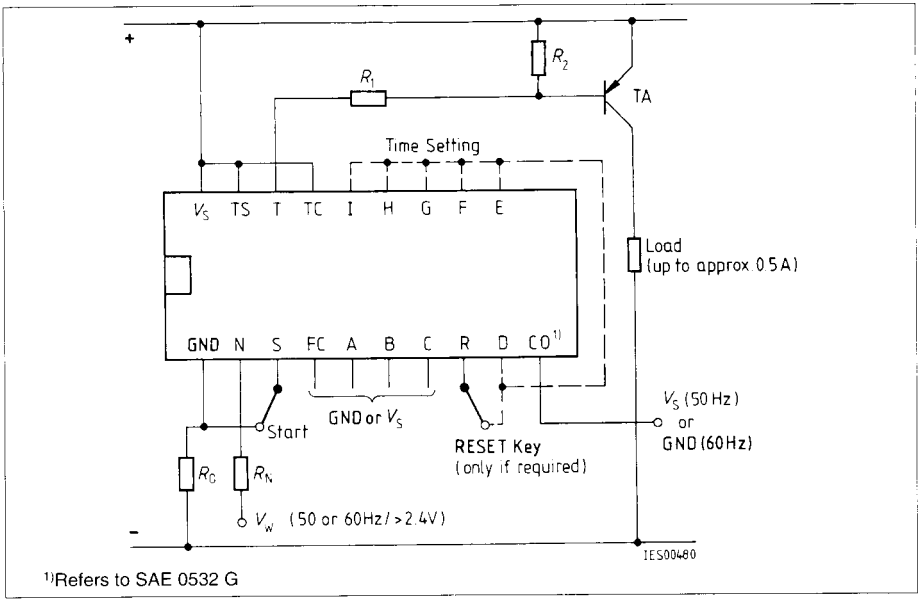
Application Circuit 2
Operation with resistive, capacitive and inductive load



Application Circuit 3
Operation with any load and continuous triac triggering

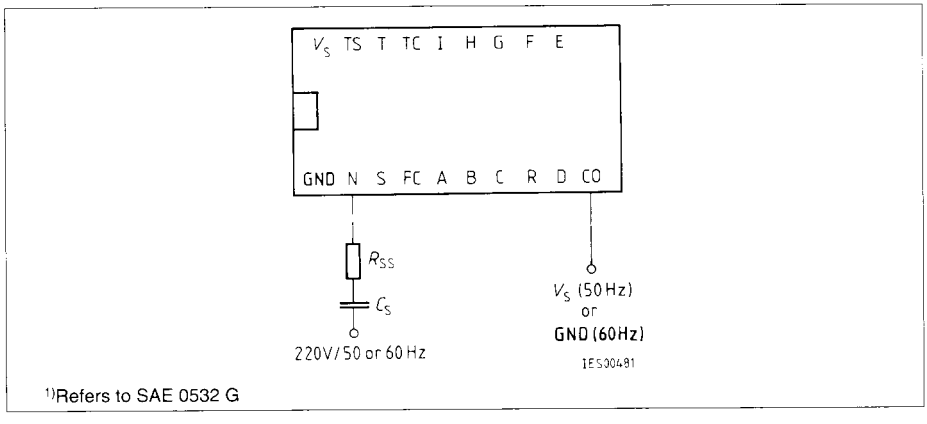


Application Circuit 4
Operation with 5-V DC voltage



[1)]Refers to SAE 0532 G

Application Circuit 5
Operation with DC voltage > 5.5 V



[1)]Refers to SAE 0532 G

Application Circuit 6
Operation with capacitive series resistor

In the application circuits 1 to 3 a series connection of *R* and *C* may be utilized instead of *R*s or *R*s and D.

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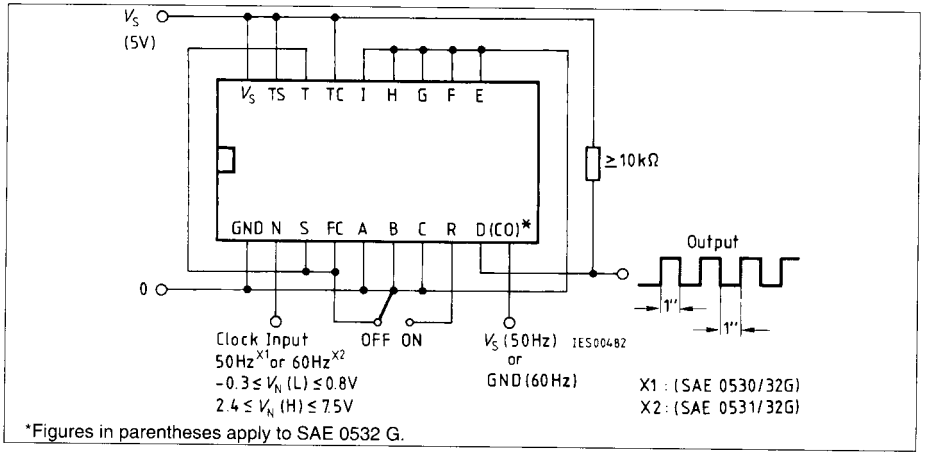
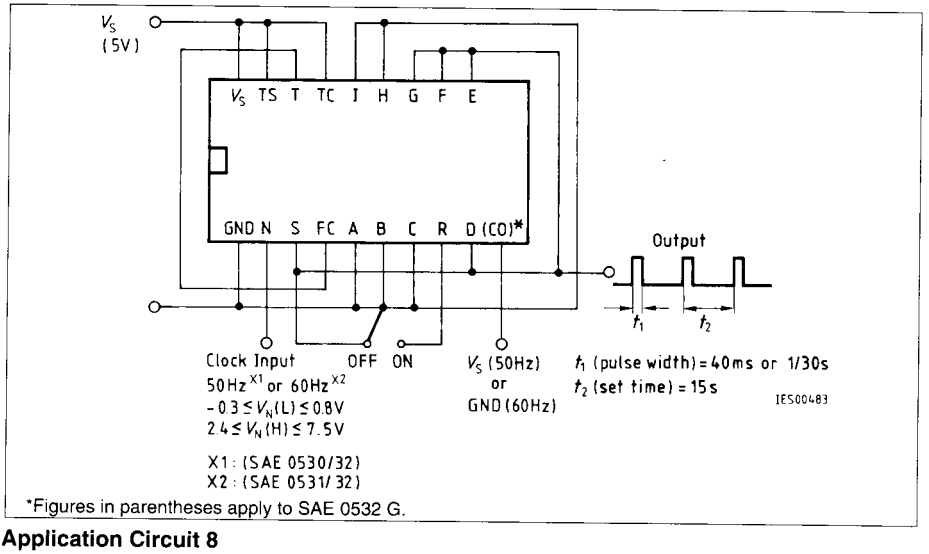


*Figures in parentheses apply to SAE 0532 G.

Application Circuit 7
Squarewave Generator Pulse Generator



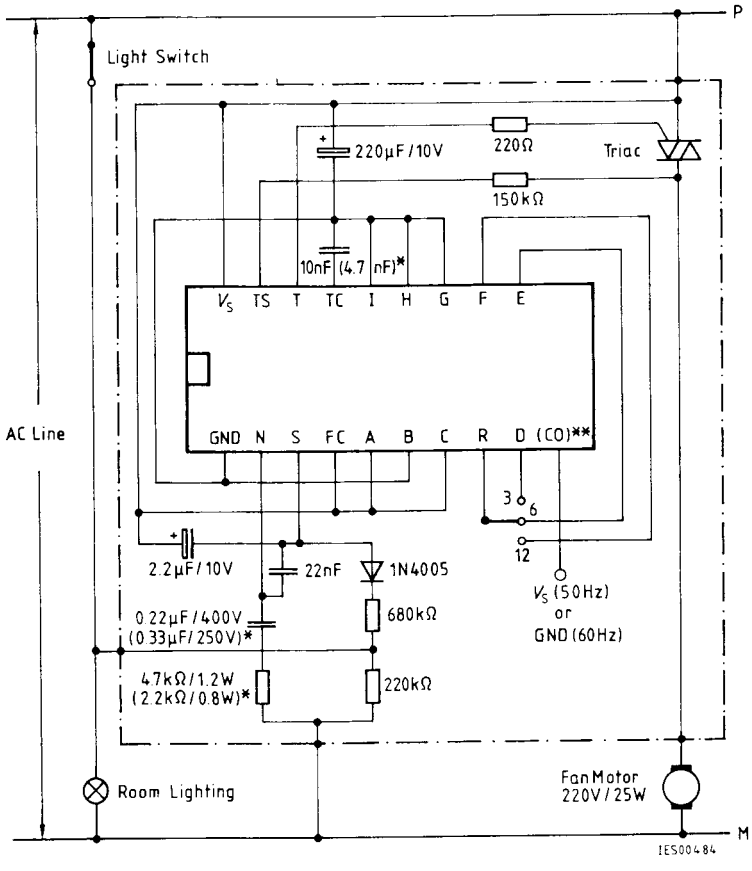
*Figures in parentheses apply to SAE 0532 G.

Application Circuit 8
Pulse Generator

Note:

The pulse width t_1 is determined only by the clock frequency f = 50 Hz (SAE 0530/32 G) or f = 60 Hz (SAE 0531/32 G) on input N: for 50/60 Hz: $t_1 = 2/f = 2/50$ (or 2/60) = 40 ms (or 1/30 s). Immediately after turn-on the first pulse t_1 and accordingly the first cycle t_2 can be up to 20 ms (or 1/60 s) shorter (according to the phase of the 50-Hz or 60-Hz network).

After turn-on output T conducts and stays on L potential throughout operation.



* Figures in parentheses apply to 60-Hz mode (SAE 0531/32 G), all other figures to 50-Hz mode (SAE 0530/32 G).
** Figures in parentheses apply to SAE 0532 G.

Application Circuit 9
Timing Control for Ventilator
(Adjustable to 3, 6 or 12 min follow-up)

Function of Circuit

The fan motor starts up when the room lighting is turned on and switches itself off automatically 3 (6 or 12) ** minutes after the lighting is turned off.

Dimensioning of Application Circuits

The following equations provide guideline values for operation with sinusoidal alternating voltages of 50 Hz (SAE 0530/32 G) or 60 Hz (SAE 0531/32 G). The firing of the triac always occurs in the 2nd and 3rd quadrant (negative trigger current).

$$T\ (\text{trigger-pulse length}) = \frac{5\ (4.18)^{*)} \times \text{holding current}}{\text{rms load current}}\ [\text{ms}]\quad (\text{for } T \leq 1.5\,\text{ms})$$

$$R_G = \frac{V_S - V_{TL} - \text{trigger voltage}}{\text{trigger current}}$$

$$R_V = \frac{0.5 \times \text{rms line voltage} - V_S}{I_S + \text{averaged trigger current}}\quad (\text{with or without diode D})$$

Averaged trigger current = 0.1 (0.12)*) × trigger current × T (T in ms)

$$\text{Dissipation on } R_V \text{ (without diode D)} = \frac{(\text{rms line voltage})^2}{R_V}$$

$$\text{Dissipation on } R_V \text{ (with diode D)} = \frac{0.5 \times (\text{rms line voltage})^2}{R_V}$$

$$C_L = \frac{20\ (17)^{*)} \times \text{rms line voltage}}{R_V}\ [\mu\text{F, V, k}\Omega]\ (\text{residual AC voltage on } V_S \leq 0.5\,V_{pp})^{***)}$$

Application Circuit 1 (voltage synchronization for resistive load)

$$R_{syn} = \frac{0.22\ (0.27)^{*)}\ T \times \text{rms line voltage} - 1.3}{0.025} \geq \frac{\text{peak line voltage}}{4}$$

[kΩ, V, ms] (for $T \leq 1.5$ ms)

Application Circuit 2 (current synchronization)

$$C_e = 16.7 \times T\ [\text{nF, ms}]^{***)}$$

$$R_{syn}{}^{**)} \geq \frac{\text{max. forward voltage} - 1.3}{I_{TSmin}}\ [\text{k}\Omega, \text{V, mA}]$$

$$R_{syn}{}^{**)} \geq \frac{\text{peak line voltage}}{4}\ [\text{k}\Omega, \text{V}]$$

$$R_{syn} \leq \frac{\text{trigger voltage} - 1.3}{I_{TSmax}}\ [\text{k}\Omega, \text{V, mA}]^{***)}$$

*) Figures in parentheses apply to 60-Hz version (SAE 0531/32 G).
**) The larger value applies.
***) See application notes.

Application Circuit 3

See R_G, R_V, C_L

Application Circuit 4

The level of the AC voltage V_{ac} must be greater than 2.4 V_p.
$R_N \approx 5 \times V_{ac} + 5$ [kΩ, V_p]

Application Circuit 5

V_{ac}, R_N: see application circuit 4 (V_{ac} referred to pin 0)

$$R_0 = \frac{V_S - 5.5}{I_S + I_{R1}}$$

$$R_1 = \frac{5.5 - V_{TL} - V_{B\,(TA)}}{I_{R1}}$$

$$R_2 = \frac{V_{B\,(TA)}}{I_{R2}}$$

$I_{R1} = I_{B\,(TA)} + I_{R2}$
$I_{R2} \approx 0.05 \times I_{B\,(TA)}$

Application Circuit 6

$$C_V \approx \frac{4\ (3.3)^{*)}}{R_V}\ [\mu F, k\Omega]$$

$R_{VV} = 0.2 \times R_V$**)

*) Figures in parentheses apply to 60-Hz version (SAE 0531/32 G).
**) See application notes.

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