SIEMENS

ICs for Communications

Quad Framing and Line Interface Component for E1 / T1 / J1
QuadFALC™

PEB 22554 Version 1.1

Preliminary Data Sheet 09.98

DS 1

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Quad Framing and Line Interface Component for E1/T1 QFALC

PEB 22554

CMOS

QuadFALC in E1 Mode

P-TQFP-144

1 Features E1

Quad Line Interface

- High density, generic interface for all E1 / T1 / J1 applications
- Quad analog receive and transmit circuitry for long/ short haul applications
- Data and clock recovery using an integrated digital phase locked loop
- Maximum line attenuation up to -34 dB at 1024 kHz adaptively controlled receive equalization network adjusts up to 4500 feet (PULP 22 AWG) in length, noise - and crosstalk -filter, line attenuation status
- Programmable transmit pulse shapes for E1 signals
- Programmable Line Build-Out according to FTZ221
- Low transmitter output impedances for high transmit return loss
- Tri-state function of the analog transmit line outputs
- Transmit line monitor protecting the device from damage
- Jitter specifications of ITU-T I.431 , G.703 , G.736 and G.823 met
- Crystal-less wander and jitter attenuation/compensation
- Low frequency reference clock: 2.048MHz
- Power down function per channel
- Dual rail or single rail digital inputs and outputs
- Unipolar NRZ or CMI for interfacing fibre optical transmission routes
- Selectable line codes (HDB3, AMI)
- Loss of signal indication with programmable thresholds according to ITU-T G.775 and ETS300233
- Clock generator for jitter free system/ transmit clocks per channel
- Local loop and remote loop for diagnostic purposes
- Ultra low power device , single power supply: 3.3 V

Type	Version	Ordering Code	Package
PEB 22554-HT	V1.1	Q67003H9339	P-TQFP-144(SMD)

Quad Frame Aligner

- Frame alignment/synthesis for 2.048 MBit/s according to ITU-T G.704
- Programmable formats : Doubleframe, CRC Multiframe
  Selectable conditions for recover / loss of frame alignment
- CRC4 to Non-CRC4 Interworking of ITU-T G. 706 Annex B
- Error checking via CRC4 procedures according to ITU-T G. 706
- Alarm and performance monitoring per second
  16 bit counter for CRC-, framing errors, code violations, error monitoring via E bit and SA6 bit, errored blocks, PRBS bit errors
- Insertion and extraction of alarms (AIS, Remote Alarm …)
- IDLE code insertion for selectable channels
- Flexible system clock frequency different for receiver and transmitter
- Supports programmable system data rates: 2048 , 4096, 8192 and 16.384MBit/s with independent receive/transmit offset programming
- Mux of 4 channels into a single rail 8.192 MBit/s data bus and v.v.
  with byte - or bitinterleaved formats
- Elastic store for receive and transmit route clock wander and jitter compensation; controlled slip capability and slip indication;
- Programmable elastic buffer size: 2 frames / 1 frame / short buffer / bypass
- Supports fractional E1 access
- Flexible transparent modes
- Programmable In-Band Loop Code detection and generation
- Channel loop back , line loop back or Payload loop back capabilities
- Pseudo Random Bit Sequence (PRBS) generator and monitor

Quad Signaling Controller

- HDLC controller
  Bit stuffing, CRC check and generation, flag generation, flag and address recognition, handling of bit oriented functions
- CAS controller with last look capability , enhanced CAS- register access and freeze signaling indication
- Provides access to serial signaling data streams
- Multiframe synchronization and synthesis acc. to ITU-T G.732
- Alarm insertion and detection (AIS and LOS in Timeslot 16)
- Transparent Mode
- FIFO buffers (64 bytes deep) for efficient transfer of data packets.
- Time-slot assignment
  Any combination of time slots selectable for data transfer independent of signaling mode.
- Time-slot 0 SA_{8-4} bit handling via FIFOs

- HDLC access to any SA bit combination

MP Interface

- 8/16 bit microprocessor bus interface (Intel or Motorola type)
- All registers directly accessible (byte or word access)
- Multiplexed and non-multiplexed address bus operations
- Hard / software reset options
- Extended interrupt capabilities
- One second timer (internal /external access)

General

- Boundary scan standard IEEE 1149.1
- P-TQFP-144 package (body size 20x20)
- 3.3 V power supply
- Typical power consumption 650 mW

Applications

- Wireless Basestations
- E1/T1/J1ATM Gateways
- E1/T1/J1 Channel & Data Service Units (CSU, DSU)
- ISDN PRI, PBXs
- E1/T1/J1 Internet Access Equipement
- LAN / WAN Router
- SONET/SDH Add/ Drop Mux
- E1/T1/J1 Multiplexer
- Digital Access Cross-Connect Systems (DACS)

1.1 Logic Symboly

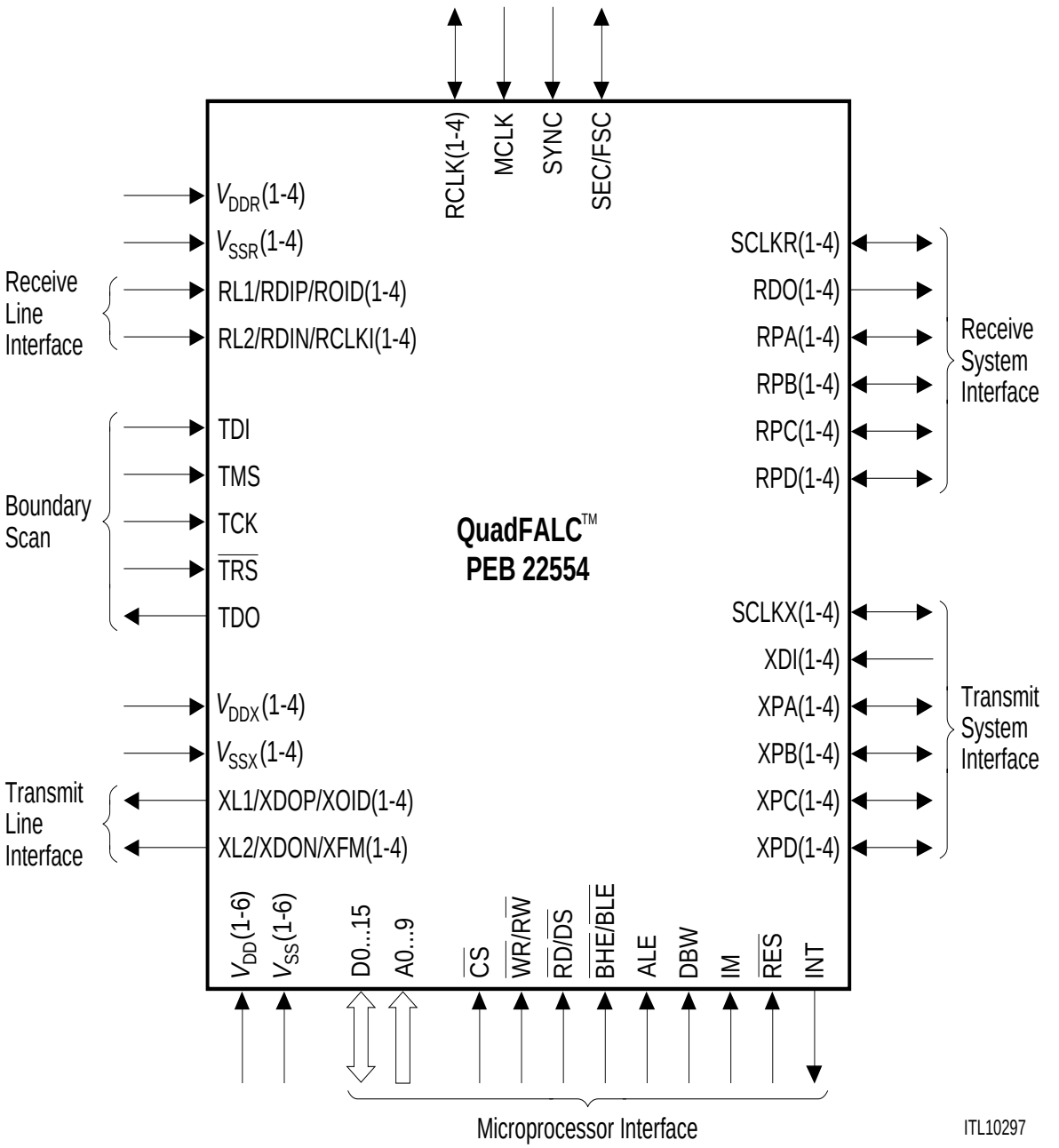


Figure 1
QuadFALC Logic Symbol

1.2 Typical Applications

The figures below show multiple link applications realized with the QuadFALC.

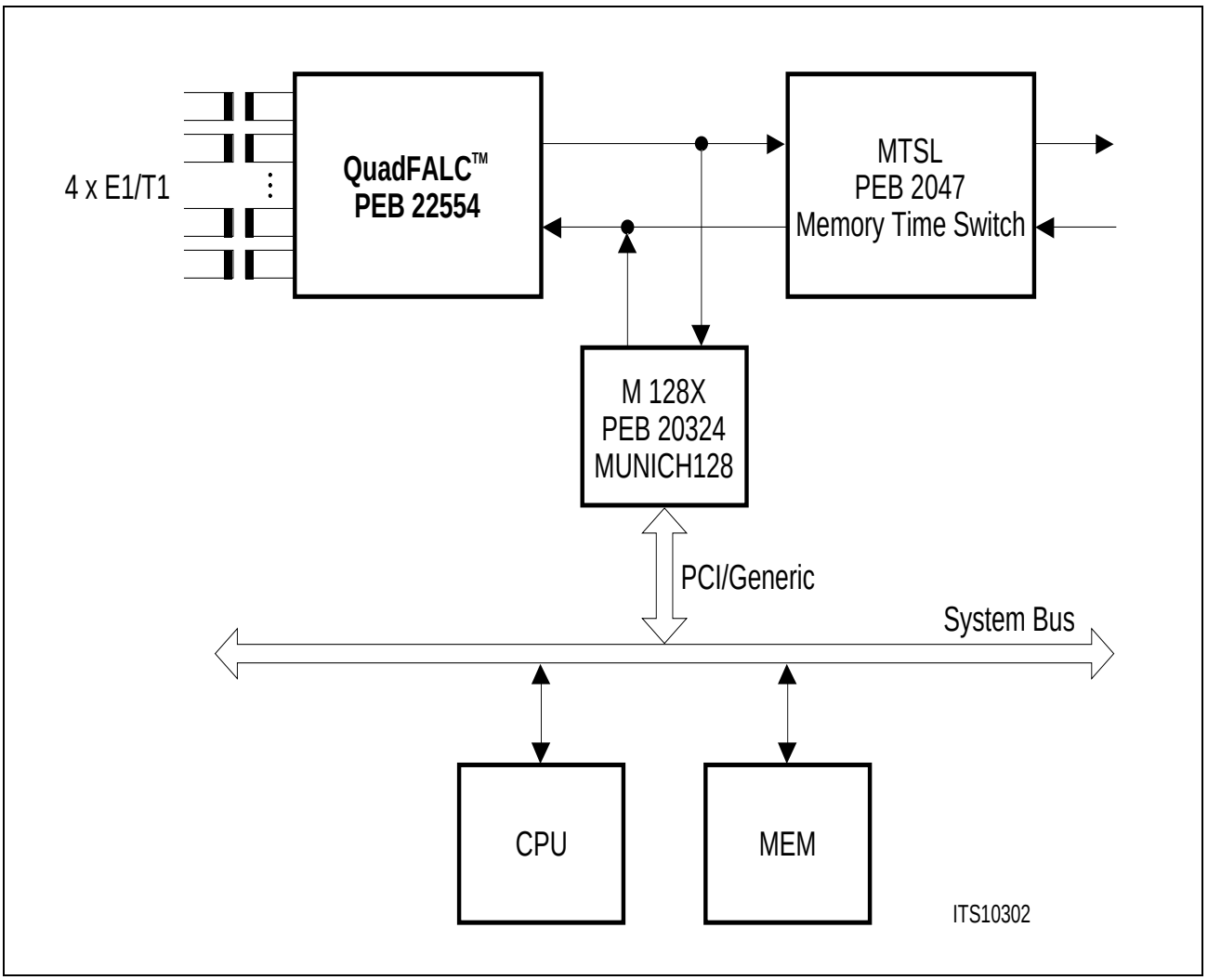


Figure 2
4 Channel E1 Interface for Frame Relay Applications

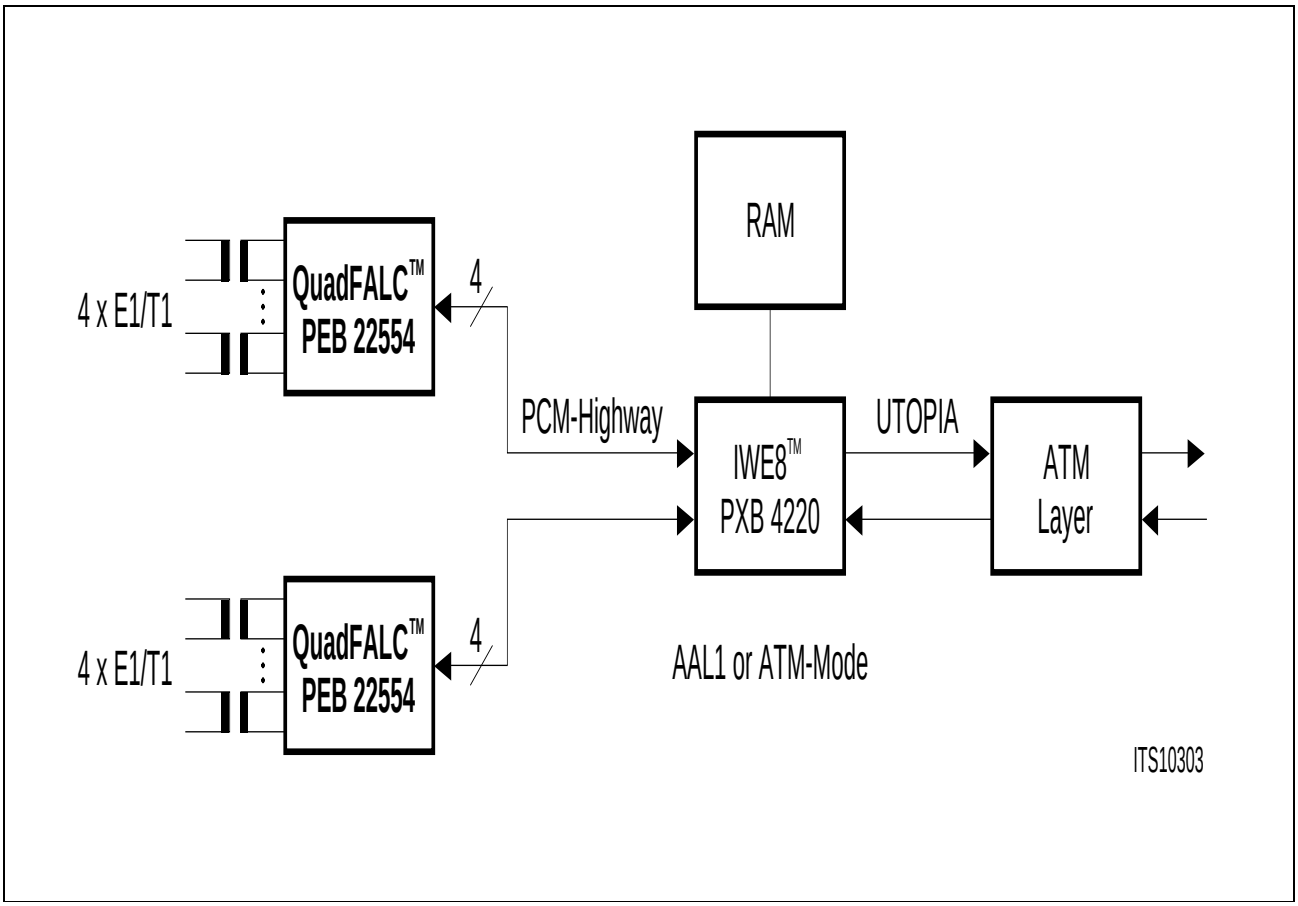


Figure 3
8 Channel E1 Interface to the ATM Layer

2 Pin Descriptions E1

2.1 Pin Diagram

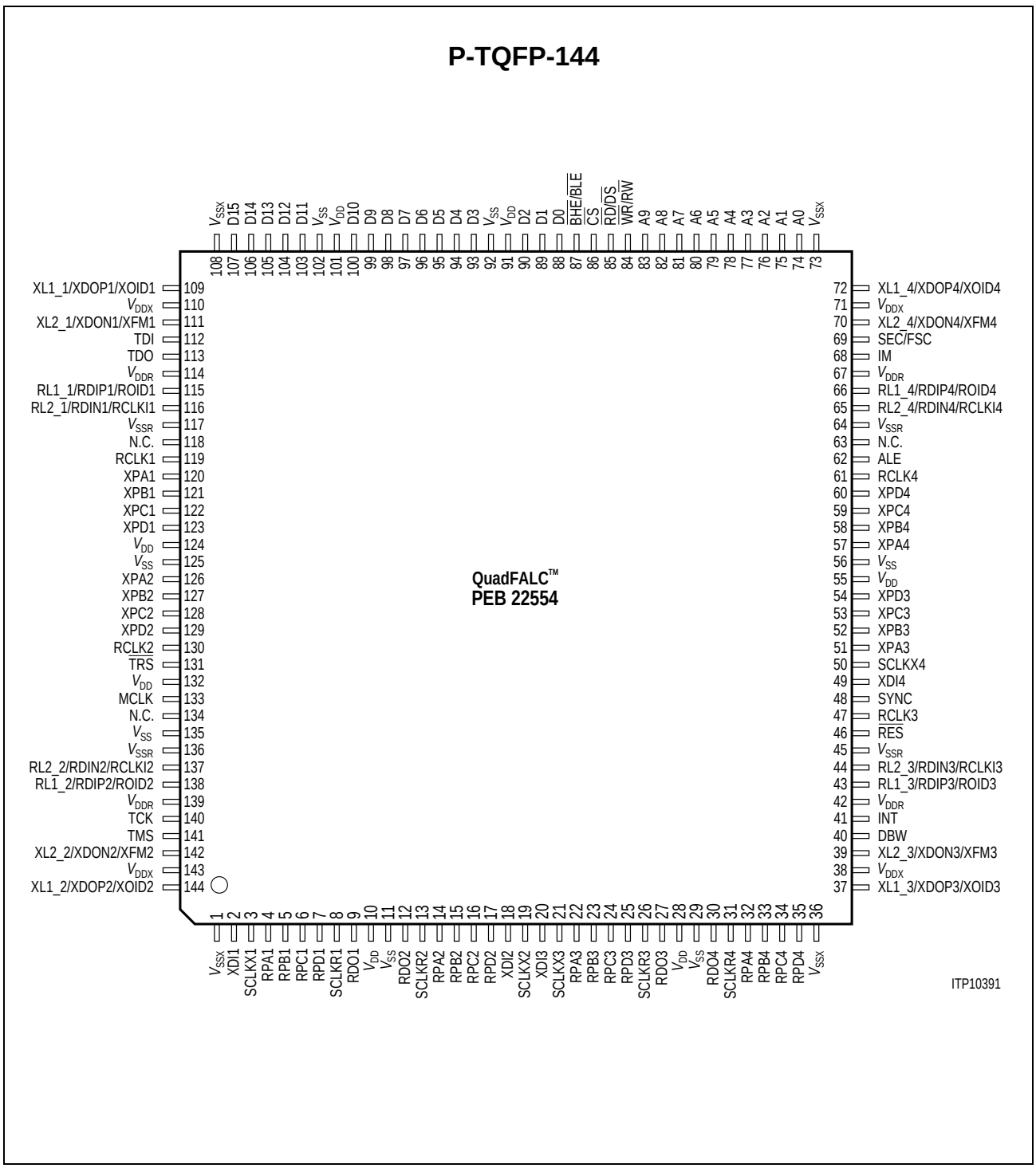


Figure 4 Pin Configuration of QuadFALC

Note: All unused input pins have to be connected to a defined level (V_{SS} / V_{DD}).

2.2 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
83 - 74	A9 … A0	I	**Address Bus** Address bus selects one of the internal registers for read or write.
107 - 103 100 - 93 90 - 88	D15 … D11 D10 … D3 D2 … D0	I/O	**Data Bus** Bi-directional three-state data lines which interface with the system's data bus. Their configuration is controlled by the level of pin DBW: – 8-bit mode (DBW = 0): D0 … D7 are active. D8 … D15 are in high impedance and have to be connected to V_{DD} or V_{SS}. – 16-bit mode (DBW = 1): D0 … D15 are active. In case of byte transfers, the active half of the bus is determined by A0 and $\overline{BHE}$/$\overline{BLE}$ and the selected bus interface mode (via pin IM). The unused half is in high impedance.
62	ALE	I	**Address Latch Enable** A high on this line indicates an address on the external address/data bus. The address information provided on lines A0 … A9 is internally latched with the falling edge of ALE. This function allows the QuadFALC to be directly connected to a multiplexed address/data bus. In this case, pins A0 … A9 must be externally connected to the Data Bus pins. In case of demultiplexed mode this pin has to be connected directly to ground or V_{DD}.

Note: All unused input pins have to be connected to a defined level (V_{SS} / V_{DD})

Note: PU = If not connected an internal pull-up transistor ensure high input level.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
85	$\overline{RD}/\overline{DS}$	I	**Read Enable** (Siemens/Intel bus mode) This signal indicates a read operation. When the QuadFALC is selected via $\overline{CS}$ the $\overline{RD}$ signal enables the bus drivers to output data from an internal register addressed via A0 … A9 on to Data Bus. **Data Strobe** (Motorola bus mode) This pin serves as input to control read/write operations.
84	$\overline{WR}/R\overline{W}$	I	**Write Enable** (Siemens/Intel bus mode) This signal indicates a write operation. When $\overline{CS}$ is active the QuadFALC loads an internal register with data provided via the Data Bus. **Read/Write Enable** (Motorola bus mode) This signal distinguishes between read and write operation.
86	$\overline{CS}$	I	**Chip Select** A low signal selects the QuadFALC for read/ write operations.
46	$\overline{RES}$	I	**Reset** A low signal on this pin forces the QuadFALC into reset state. During Reset the QuadFALC needs an active clock on pin MCLK. During Reset all bi-directional output stages (data bus) arein high-impedance state if signal $\overline{RD}$ is "high".

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
87	$\overline{\text{BHE}}$/$\overline{\text{BLE}}$	I	**Bus High Enable** (Siemens/Intel bus mode) If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the upper byte of the data bus (D8 … D15). In 8-bit bus interface mode this signal has no function and should be tied to V_{DD}. **Bus Low Enable** (Motorola bus mode) If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the lower byte of the data bus (D0 … D7). In 8-bit bus interface mode this signal has no function and should be tied to V_{DD}.
40	DBW	I	**Data Bus Width** (Bus Interface Mode) A low signal on this input selects the 8-bit bus interface mode. A high signal on this input selects the 16-bit bus interface mode. In this case word transfer to/from the internal registers is enabled. Byte transfers are implemented by using A0 and $\overline{\text{BHE}}$/$\overline{\text{BLE}}$.
41	INT	O/oD	**Interrupt Request** INT serves as general interrupt request which may include all interrupt sources. These interrupt sources can be masked via registers IMR0 … 5. Interrupt status is reported via registers GIS (Global Interrupt Status) and ISR0 …5. Output characteristics (push-pull active low/ high, open drain) are determined by programming the IPC register.
68	IM	I	**Interface Mode** The level at this pin defines the bus interface mode: A low signal on this input selects the INTEL interface mode. A high signal on this input selects the Motorola interface mode.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
115, 138, 43, 66	RL1(1-4)	I	**Line Receiver 1** Analog Input from the external transformer. Selected if LIM1.DRS = 0.
	RDIP(1-4)	I	**Receive Data Input Positive** Digital input for received dual rail PCM(+) route signal which will be latched with the internal generated Receive Route Clock. An internal DPLL will extract the Receive Route Clock from the incoming data pulse. The duty cycle of the receiving signal has to be closely to 50 %. The Dual Rail mode is selected if LIM1.DRS = 1 and FMR0.RC1 = 1. Input sense is selected by bit RC0.RDIS (after Reset: active low).
	ROID(1-4)	I	**Receive Optical Interface Data** Unipolar data received from fibre optical interface with 2.048 MBit/s. Latching of data is done with the falling edge of RCLKI. Input sense is selected by bit RC0.RDIS. The Single Rail mode is selected if LIM1.DRS = 1 and FMR0.RC1 = 0.
116, 137, 44, 65	RL2(1-4)	I	**Line Receiver** 2 Analog Input from the external transformer. Selected if LIM1.DRS = 0.
	RDIN(1-4)	I	**Receive Data Input Negative** Input for received dual rail PCM(-) route signal which will be latched with the internal generated Receive Route Clock. An internal DPLL will extract the Receive Route Clock from the incoming data pulse. The duty cycle of the receiving signal has to be closely to 50 %. The dual rail mode is selected if LIM1.DRS = 1 and FMR0.RC1 = 1. Input sense is selected by bit RC0.RDIS (after Reset: active low).
	RCLKI(1-4)	I	**Receive Clock Input** Receive clock input for the optical interface if LIM1.DRS = 1 and FMR0.RC1/0 = 00. Clock frequency: 2048 kHz

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
42, 67, 114, 132, 139	V_{DDR}	I	**Positive Power Supply** for the analog receiver.
45, 64, 117,135, 136	V_{SSR}	I	**Power Supply Ground** for the analog receiver
111, 142, 39, 70	XL2(1-4)	O	**Transmit Line 2** Analog output for the external transformer. Selected if LIM1.DRS = 0. After Reset this pin is in a high impedance state until register FMR0.XC1 is set to one.
	XDON(1-4)	O	**Transmit Data Output Negative** This digital output for transmitted dual rail PCM(-) route signals can provide – half bauded signals with 50% duty cycle (LIM0.XFB = 0) or – full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data will be clocked off on the positive transitions of XCLK in both cases. Output sense is selected by bit LIM0.XDOS (after Reset: active low). The dual rail mode is selected if LIM1.DRS = 1 and FMR0.XC1 = 1. After Reset this pin is in a high impedance state until register LIM1.DRS is set to one.
	XFM(1-4)	O	**Transmit Frame Marker** This digital output marks the first bit of every frame. This function is only available in the optical interface mode LIM1.DRS=1 and FMR0.XC1 = 0. The data will be clocked off on the positive transitions of XCLK. After Reset this pin is in a high impedance state until register LIM1.DRS is set to one. In remote loop configuration the XFM marker is not valid.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
109, 144, 37, 72	XL1(1-4)	O	**Transmit Line 1** Analog output for the external transformer. Selected if LIM1.DRS = 0. After Reset this pin is in a high impedance state until register FMR0.XC1 is set to one.
	XDOP(1-4)	O	**Transmit Data Output Positive** This digital output for transmitted dual rail PCM(+) route signals can provide – half bauded signals with 50% duty cycle (LIM0.XFB = 0) or – full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data will be clocked off on the positive transitions of XCLK in both cases. Output sense is selected by bit LIM0.XDOS (after Reset: active low). The dual rail mode is selected if LIM1.DRS = 1 and FMR0.XC1 = 1. After Reset this pin is in a high impedance state until register LIM1.DRS is set to one.
	XOID(1-4)	O	**Transmit Optical Interface Data** Unipolar data sent to fibre optical interface with 2.048 MBit/s which will be clocked off on the positive transitions of XCLK. Clocking off data in NRZ code is done with 100 % duty cycle. Data in CMI code are shifted out with 50 % or 100 % duty cycle according to the CMI coding. Output sense is selected by bit LIM0.XDOS (after Reset: data is sent active high). The single rail mode is selected if LIM1.DRS = 1 and FMR0.XC1 = 0. After Reset this pin is in a high impedance state until register LIM1.DRS is set to one.
38, 71, 110, 143	V_{DDX}	I	**Positive Power Supply** for analog transmitter
1, 36, 73, 108	V_{SSX}	I	**Power Supply Ground** for analog transmitter

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
133	MCLK	I	**Reference Clock 2.048 MHz** A reference clock of 2.048 MHz +/- 50 ppm must be provided to this pin.
134	NC		**Not connected**
48	SYNC	I + PU	**Clock Synchronization** If a clock is detected at the SYNC pin the DCO-Rs of the QuadFALC synchronize to this 2.048 MHz clock. This pin has an integrated pull up resistor.
69	SEC	I + PU	**Second Timer Input** A pulse with logical one for at least two 2.048MHz cycles will trigger the internal second timer.
	FSC	O	Enabled with GPC1.FSS2-0 an **8-kHz Frame Synchronization Pulse** is output via this pin. The synchronization pulse is active high / low for one 2 MHz cycle (pulse width = 488 ns).
	SEC	O	**Second Timer Output** Activated high every second for two 2.048 MHz clock cycles. Enabled with GPC1.CSFP1-0.
119, 130, 47, 61	RCLK(1-4)	I/O + PU	**Receive Clock** After Reset this port is configured to an input. Setting of bit PC5.CRP will switch this port to an output. Input function not defined. Output function: CMR1.RS1/0 = 00: Receive Clock extracted from the incoming data pulses. Frequency: 2048 kHz CMR1.RS1/0 = 01: RCLK is set high in case of loss of signal (FRS0.LOS=1). Optional one of the dejittered system clocks sourced by DCO-R is clocked out. Clock frequency: 2048 or 8192 kHz . Selected by CMR1.RS1/0. Wih GPC1.R1S1/0 one of the four RCLK(1-4) is output on RCLK1.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
8, 13, 26, 31	SCLKR (1-4)	I/O + PU	**System Clock Receive** Working clock for the receive system interface with a frequency of 16.384 / 8.192 / 4.096 / 2.048 MHz. If the receive elastic store is bypassed SIC1.RBS1/0 the clock supplied on this pin is ignored. If SCLKR is configured to an output, the internal working clock of the receive system interface sourced by DCO-R or RCLK is output. In system interface multiplex mode a 16.384 or 8.192 MHz clock has to be provided on SCLKR1, which is a common clock for all 4 rec. system interfaces.
9, 12, 27, 30	RDO(1-4)	O	**Receive Data Out** Received data which is sent to the system highway. Clocking off data is done with the rising or falling edge (SIC3.RESR) of SCLKR(1-4) or RCLK(1-4) if the receive elastic store is bypassed. The delay between the beginning of time-slot 0 and the initial edge of SCLKR(1-4) (after $\overline{\text{SYPR}}$ goes active) is determined by the values of registers RC1 and RC0. If received data is shifted out with higher data rates, the active channel phase is defined by bits SIC2.SICS2-0. In system interface multiplex mode all 4 received datastreams are merged into a single datastream byte or bit interleaved on RDO1.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
4 -7, 14 -17, 22 - 25, 32 - 35	RP(A-D)1 RP(A-D)2 RP(A-D)3 RP(A-D)4	I/O + PU	**Receive Multifunction Port A-D** Depending on programming of bits PC(1-4).RPC(2-0) this multifunction ports carries information to the system interface or from the system to the QuadFALC. After Reset these ports are configured to inputs. With the selection of the pinfunction the in/output configuration is also achieved. Depending on bit SIC3.RESR all outputs / inputs of the receive system interface are updated / sampled with the rising or falling edge of SCLKR.
		I + PU	**Synchronous Pulse Receive ($\overline{\text{SYPR}}$)** Defines the beginning of time-slot 0 at system highway port RDO in conjunction with the values of registers RC0/1. In system interface multiplex mode $\overline{\text{SYPR}}$ has to be provided at port RPA1 for all 4 channels and defines the beginning of time-slot 0 on port RDO1/RSIG1. Enabled with PC(1-4).RPC(2-0) = 000 (reset configuration). Pulse Cycle: Integer multiple of 125 µs.
		O	**Receive Frame Marker (RFM)** Enabled with PC(1-4).RPC(2-0) = 001. CMR2.IRSP = 0: The receive frame marker could be active high for a 2.048 MHz period during any bit position of the current frame. IProgramming is done with registers RC1/0. CMR2.IRSP = 1: Internal generated frame synchronization pulse generated by the DCO-R circuitry. Together with registers RC1/0 the frame begin on the receive system interface is defined. This frame synchronization pulse is active low 2.048 MHz period.
		O	**Receive Multiframe Begin (RMFB)** Enabled with PC(1-4).RPC(2-0) = 010. RMFB marks the beginning of every received multiframe (RDO). Optionally the time-slot 16 CAS multiframe begin could be marked (SIC3.CASMF). Active high for one 2.048 MBit/s period.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
4 -7, 14 -17, 22 - 25, 32 - 35	RP(A-D)1 RP(A-D)2 RP(A-D)3 RP(A-D)4	O	**Receive Signaling Marker (RSIGM)** Enabled with PC(1-4).RPC(2-0) = 011. Marks the time-slots which are defined by register RTR1-4 of every frame on port RDO.
		O	**Receive Signaling Data (RSIG)** Enabled with PC(1-4).RPC(2-0) = 100. The received CAS signaling data is sourced by this pin. Time-slots on RSIG correlates directly to the time-slot assignment on RDO. In system interface multiplex mode all four received signaling datastreams are merged into a single datastream byte or bit interleaved and is transmitted on port RPB1.
		O	**Data Link Bit Receive (DLR)** Enabled with PC(1-4).RPC(2-0) = 101. Marks the SA8-4 bits within the data stream on RDO. The SA8-4 bit positions in time-slot 0 of every frame not containing the frame alignment signal are selected by register XC0.
		O	**Freeze Signaling (FREEZE)** Enabled with PC(1-4).RPC(2-0) = 110. The freeze signaling status is active high by detecting a Loss of Signal alarm, or a Loss of CAS Frame Alignment or a receive slip (pos. or neg.). It will hold high for at least one complete multiframe after the alarm disappears. Setting SIC2.FFS enforces a high on pin FREEZE.
		O	**Frame Synchronous Pulse ($\overline{\text{RFSP}}$)** Enabled with PC(1-4).RPC(2-0) = 111. Active low framing pulse derived from the received PCM route signal. During loss of synchronization (bit FRS0.LFA), this pulse is suppressed (not influenced during alarm simulation). Pulse frequency: 8 kHz, Pulse width: 488 ns

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
3, 19, 21, 50	SCLKX (1-4)	I/O + PU	**System Clock Transmit** Working clock for the transmit system interface with a frequency of 16.384 / 8.192 / 4.096 / 2.048 MHz. In system interface multiplex mode a 16.384 or 8.192 MHz clock has to be provided on SCLKX1, which is a common clock for all 4 transmit system interfaces.
2, 18, 20, 49	XDI(1-4)	I	**Transmit Data In** Transmit data received from the system highway. Latching of data is done with rising or falling transitions of SCLKX according to bit SIC3.RESX. The delay between the beginning of time-slot 0 and the initial edge of SCLKX (after $\overline{\text{SYPX}}$ goes active) is determined by the registers XC1/0. In system interface multiplex mode latching of datastream containing the 4 frames is done byte or bit interleaved on port XDI1. In higher data rates sampling of data is defined by bits SIC2.SICS2-0.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
120 - 123 126 - 129 51 - 54 57 - 60	XP(A-D)1 XP(A-D)2 XP(A-D)3 XP(A-D)4	I/O + PU	**Transmit Multifunction Port A-D** Depending on programming of bits PC(1-4).XPC(2-0) this multifunction ports carries information to the system interface or from the system to the QuadFALC. After Reset these ports are configured to inputs. With the selection of the pinfunction the in/output configuration is also achieved. Depending on bit SIC3.RESX all outputs / inputs of the transmit system interface are updated / sampled with the rising or falling edge of SCLKX
		I + PU	**Synchronous Pulse Transmit ($\overline{\text{SYPX}}$)** Defines the beginning of time-slot 0 at system highway port XDI in conjunction with the values of registers XC0/1. In system interface multiplex mode $\overline{\text{SYPX}}$ has to be provided at port XPA1 for all 4 channels and defines the beginning of time-slot 0 on port XDI1/XSIG1. Enabled with PC(1-4).XPC(2-0) = 000 (reset configuration). Pulse Cycle: Integer multiple of 125 µs.
		I + PU	**Transmit Multiframe Synchronization (XMFS)** Enabled with PC(1-4).XPC(2-0) = 001 this port defines the frame and multiframe begin on the transmit system interface ports XDI and XSIG. Depending on PC5.CXMFS the signal on XMFS is active high or low. For correct operation of XMFS no $\overline{\text{SYPX}}$ pin function should be selected for the remaining multifunction ports of the same channel. In system interface multiplex mode XMFS has to be provided at port XPB1 for all 4 channels. ***Note:*** *A new multiframe position has been settled at least one multiframe after pulse XMFS has been supplied.*

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
120 - 123 126 - 129 51 - 54 57 - 60	XP(A-D)1 XP(A-D)2 XP(A-D)3 XP(A-D)4	I + PU	**Transmit Signaling Data (XSIG)** Enabled with PC(1-4).XPC(2-0) = 010. Input for transmit signaling data received from the signaling highway. Optionally (SIC3.TTRF) sampling of XSIG data is controlled by the active high XSIGM marker. In higher data rates sampling of data is defined by bits SIC2.SICS2-0. In system interface multiplex mode latching of the datastream containing the 4 signaling multiframes is done byte or bit interleaved on port XPC1.
		I + PU	**Transmit Clock (TCLK)** Enabled with PC(1-4).XPC(2-0) = 011. A 2.048 / 8.192 MHz clock has to be sourced by the system if the internal generated transmit clock (DCO-X) should not be used. Optional this input functions as a synchronization clock for the DCO-X circuitry with a frequency of 2.048 MHz clock.
		O	**Transmit Multiframe Begin (XMFB)** XMFB marks the beginning of every transmitted multiframe (XDI). Active high for one 2.048 MBit/s period. Enabled with PC(1-4).XPC(2-0) = 100.
		O	**Transmit Signaling Marker (XSIGM)** Marks the transmit time-slots which are defined by register TTR1-4 of every frame transmitted via port XDI. Enabled with PC(1-4).XPC(2-0) = 101.
		O	**Data Link Bit Transmit (DLX)** Marks the SA8-4 bits within the data stream on XDI. The SA8-4 bit positions in time-slot 0 of every frame not containing the frame alignment signal are selected by register XC0.SA8E-SA4E. Enabled with PC(1-4).XPC(2-0) = 110.
		O	**Transmit Clock (XCLK)** Transmit line clock, frequency: 2.048 MHz Derived from SCLKX/R, RCLK or internally generated by the DCO-X circuitry. Enabled with PC(1-4).XPC(2-0) = 111.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
11, 29, 56, 92, 102, 125,	V_{SS}	I	**Power Ground** Supply for digital subcircuits (0 V) For correct operation, all six pins have to be connected to ground.
10, 28, 55, 91, 101, 124,	V_{DD}	I	**Positive Power Supply** for the digital subcircuits (3.3 V) For correct operation, all six pins have to be connected to positive power supply.
112	TDI	I + PU	**Test Data Input** for Boundary Scan acc. to IEEE Std. 1149.1
113	TDO	O	**Test Data Output** for Boundary Scan
141	TMS	I + PU	**Test Mode Select** for Boundary Scan
140	TCK	I + PU	**Test Clock** for Boundary Scan
131	$\overline{\text{TRS}}$	I + PU	**Test Reset** for Boundary Scan (active low) If the JTAG Boundary Scan is not used this pin can be connected to pin $\overline{\text{RES}}$ or VSS.
63, 118	RSVD	I/O + PU	**Reserved**

3 Functional Description E1

3.1 Functional Block Diagram

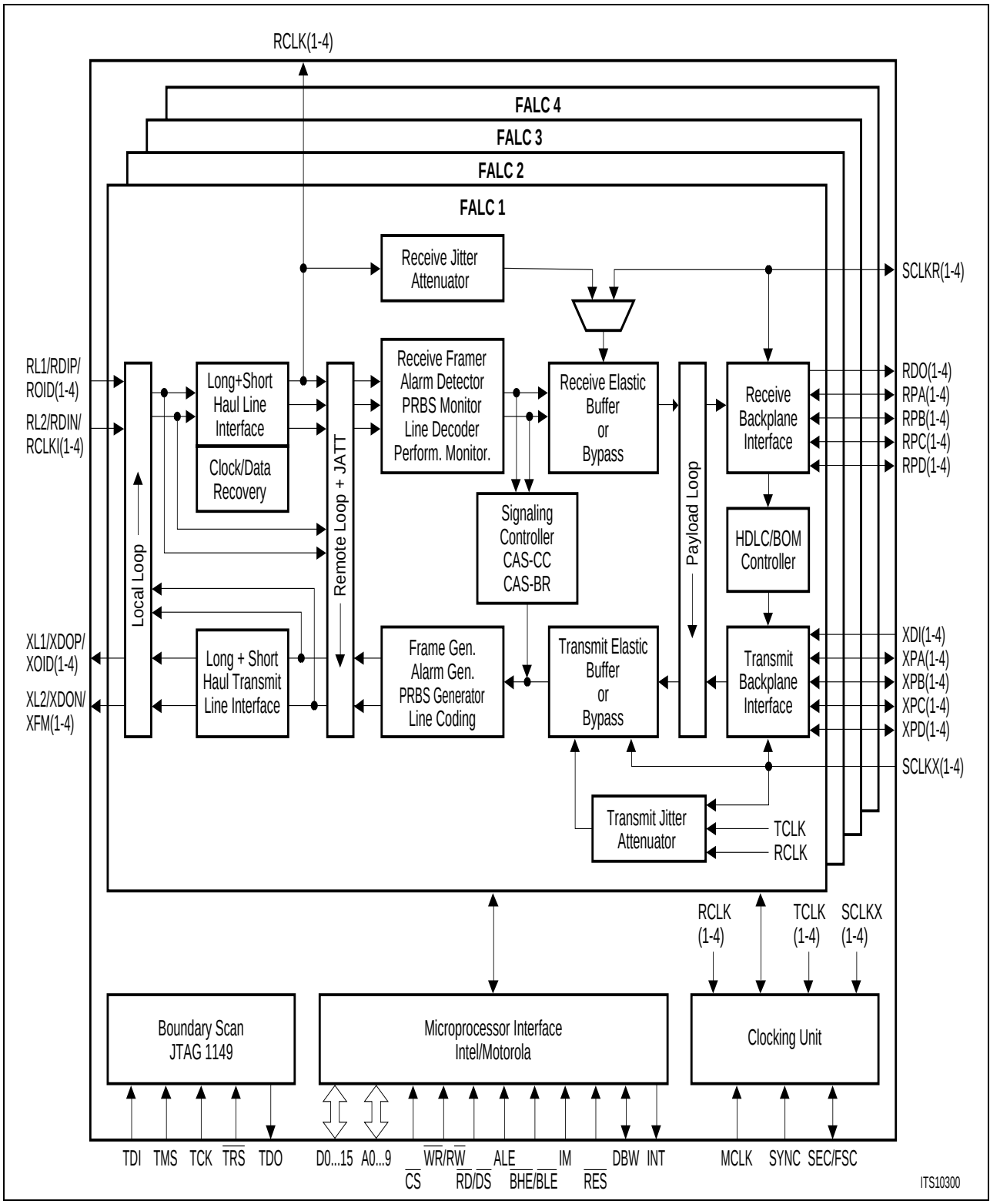


Figure 5Functional Block Diagram PEB 22554

3.2 Microprocessor Interface

The communication between the CPU and the QuadFALC is done via a set of directly accessible registers. The interface may be configured as Siemens/Intel or Motorola type with a selectable data bus width of 8 or 16 bits.

The CPU transfers data to/from the QuadFALC (via 64 byte deep FIFOs per direction and channel), sets the operating modes, controls function sequences, and gets status information by writing or reading control/status registers. All accesses can be done as byte or word accesses if enabled. If 16-bit bus width is selected, access to lower/upper part of the data bus is determined by address line A0 and signal $\overline{BHE}$/$\overline{BLE}$ as shown in **table 1** and **2**.

In **table 3** is shown how the ALE (address latch enable) line is used to control the bus structure and interface type. The switching of ALE allows the QuadFALC to be directly connected to a multiplexed address/data bus.

Mixed Byte/Word Access to the FIFOs

Reading from or writing to the internal FIFOs (RFIFO and XFIFO of each channel) can be done using a 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. Randomly mixed byte/word access to the FIFOs is allowed without any restrictions.

Table 1
Data Bus Access (16-Bit Intel Mode)

$\overline{BHE}$	A0	Register Access	QuadFALC Data Pins Used
0	0	FIFO word access Register word access (even addresses)	D0 – D15
0	1	Register byte access (odd addresses)	D8 – D15
1	0	Register byte access (even addresses)	D0 – D7
1	1	No transfer performed	None

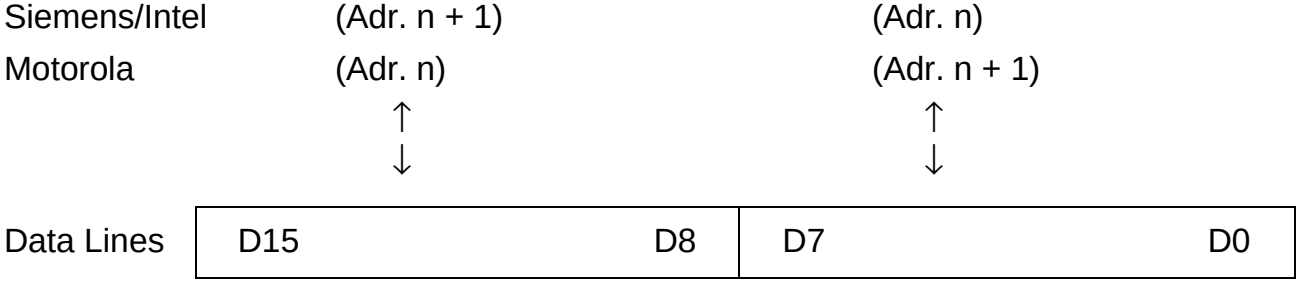
Table 2
Data Bus Access (16-Bit Motorola Mode)

$\overline{BLE}$	A0	Register Access	QuadFALC Data Pins Used
0	0	FIFO word access Register word access (even addresses)	D0 – D15
0	1	Register byte access (odd addresses)	D0 – D7
1	0	Register byte access (even addresses)	D8 – D15
1	1	No transfer performed	None

Table 3
Selectable Bus and Microprocessor Interface Configuration

ALE	IM	Microprocessor interface	Bus Structure
GND/VDD	1	Motorola	demultiplexed
GND/VDD	0	Intel	demultiplexed
switching	0	Intel	multiplexed

The assignment of registers with even/odd addresses to the data lines in case of 16-bit register access depends on the selected microprocessor interface mode:



n: even address

Complete information concerning register functions is provided in – Detailed Register Description.

FIFO Structure

In transmit and receive direction of the signaling controller 64-byte deep FIFOs for each channel are provided for the intermediate storage of data between the system internal highway and the CPU interface. The FIFOs are divided into two halves of 32-bytes. Only one half is accessible to the CPU at any time.

In case 16-bit data bus width is selected by fixing pin DBW to logical ‘1’ word access to the FIFOs is enabled. Data output to bus lines D0-D15 as a function of the selected interface mode is shown in **figure 6** and **7**. Of course, byte access is also allowed.The effective length of the accessible part of RFIFO can be changed from 32 bytes (RESET value) down to 2 bytes independent for each channel.

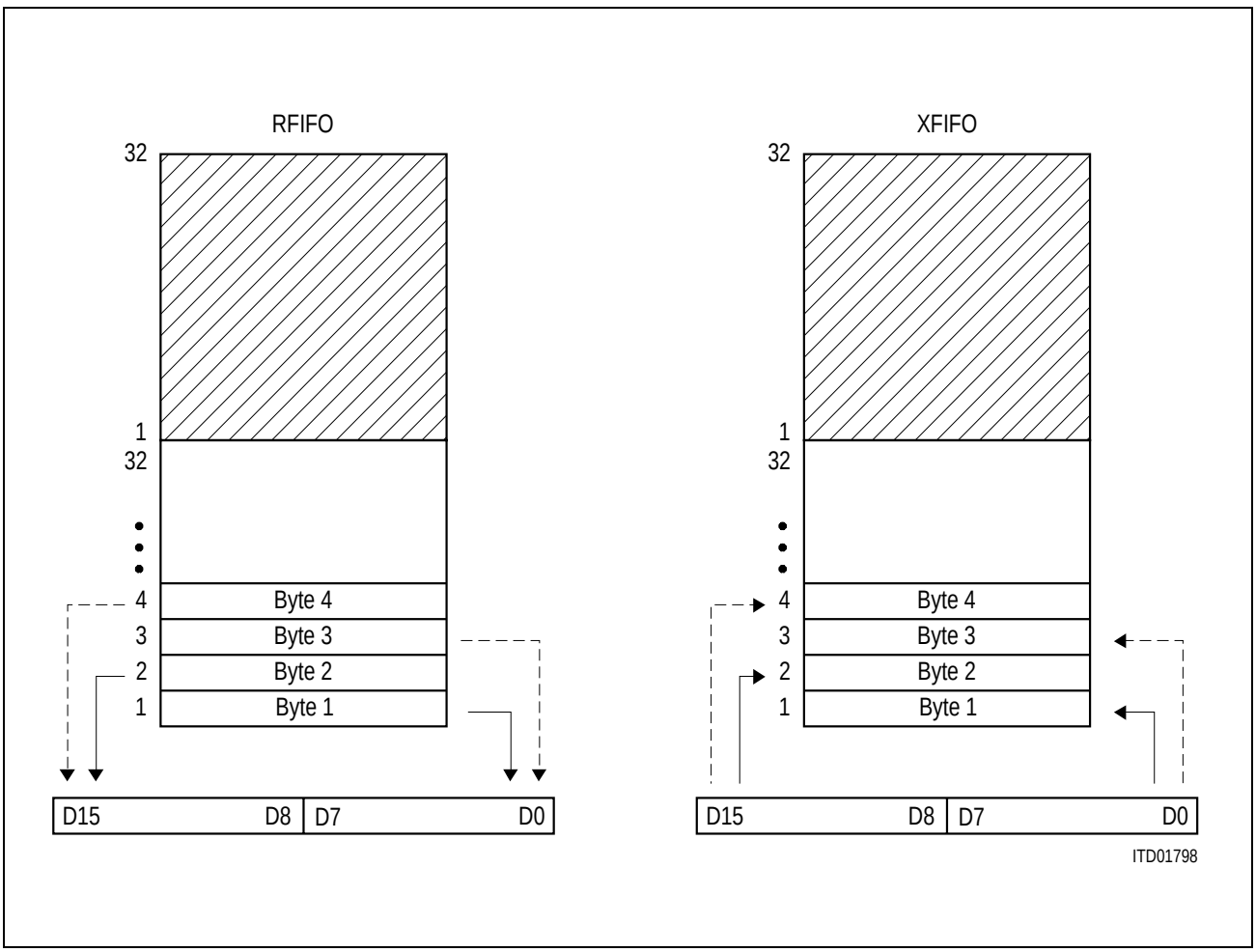


Figure 6
FIFO Word Access (Intel Mode)

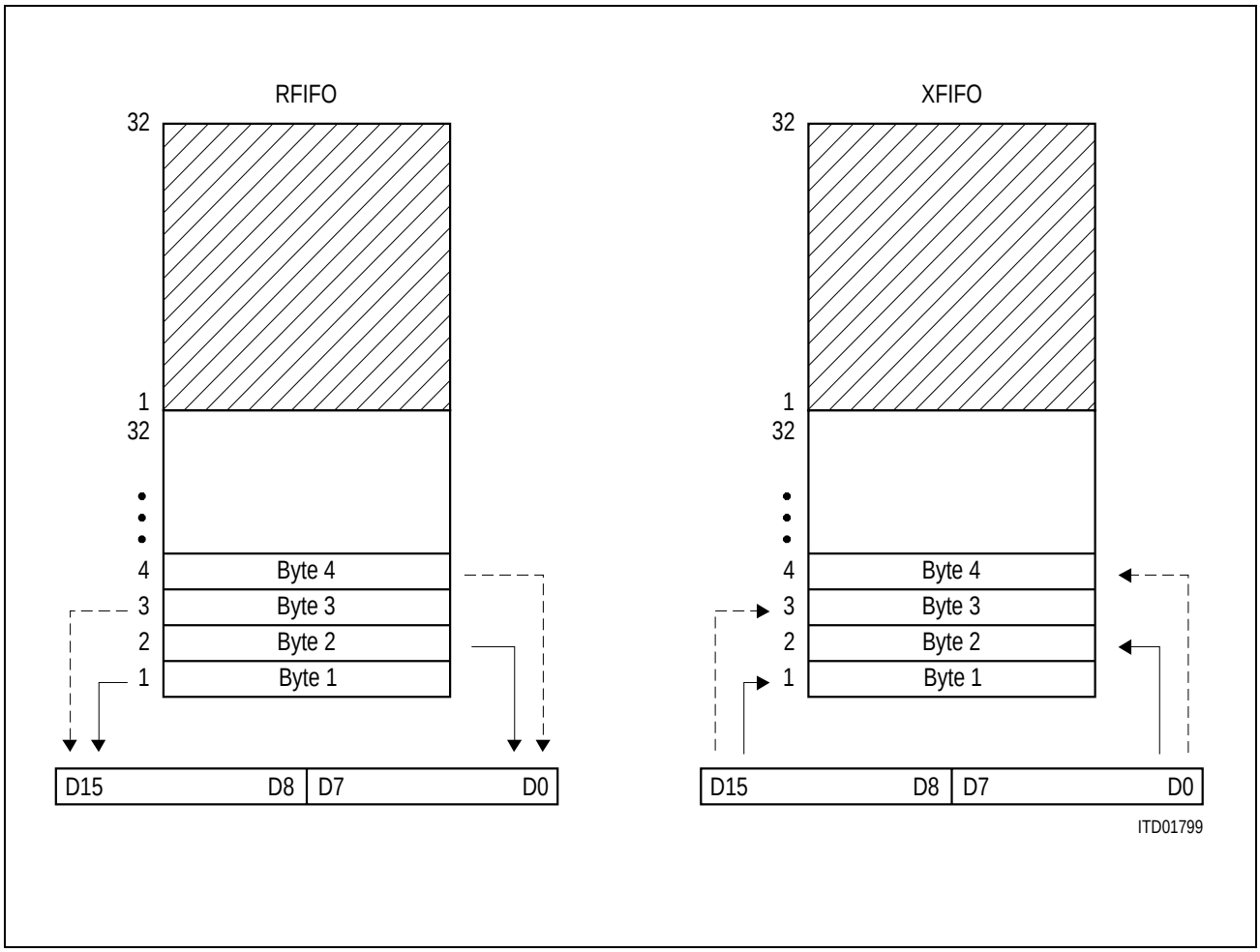


Figure 7
FIFO Word Access (Motorola Mode)

Interrupt Interface

Special events in the QuadFALC are indicated by means of a single interrupt output with programmable characteristics (open drain, push-pull; IPC register), which requests the CPU to read status information from the QuadFALC, or to transfer data from/to QuadFALC.

Since only one INT request output is provided, the cause of an interrupt must be determined by the CPU by reading the QuadFALC's interrupt status registers (CIS, GIS, ISR0-4) that means the interrupt on pin INT and the interrupt status bits are reset by reading the interrupt status registers. Register ISR0-4 are from type "Clear on Read".

The structure of the interrupt status registers is shown in **figure 8**.

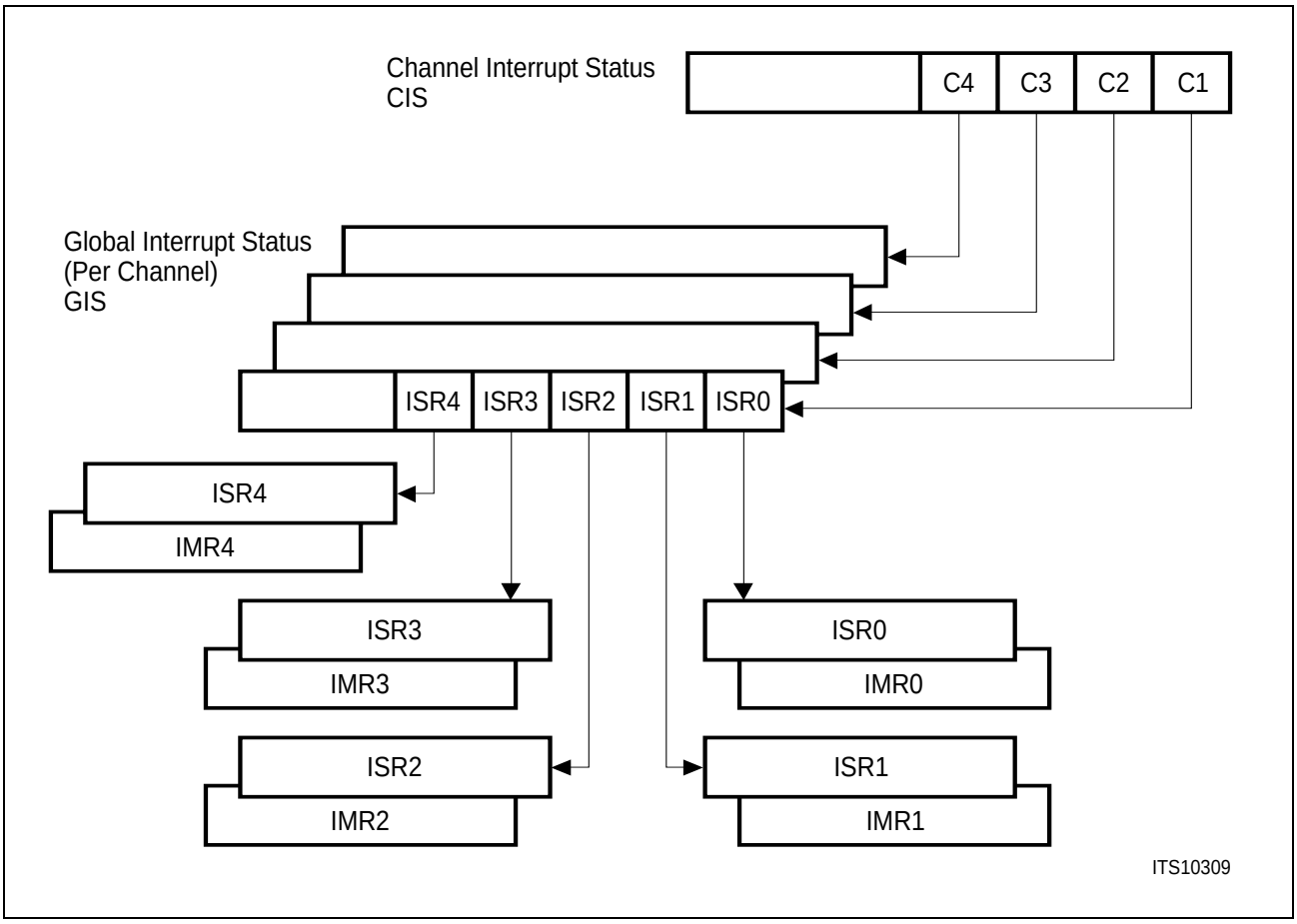


Figure 8
QuadFALC Interrupt Status Register Structure

Each interrupt indication of registers ISR0-4 can be selectively masked by setting the corresponding bit in the corresponding mask registers IMR0-4. If the interrupt status bits are masked, they neither generate an interrupt at INT nor are they visible in ISR0-4.

CIS, the non-maskable Channel Interrupt Status Register, serves as a pointer to pending channel related global interrupt status registers. After the QuadFALC has requested an interrupt by activating its INT pin, the CPU should first read the Channel Interrupt Status

register CIS to identify the requesting channel. The global interrupt status register serves itself as a pointer to pending interrupt status registers ISR0 -4 for each channel. After reading the assigned global interrupt status register and the assigned interrupt status registers ISR0- 4, the pointer in the GIS and CIS registers are cleared or updated if another interrupt requires service.

If **all** pending interrupts are acknowledged by reading (CIS and GIS are reset), pin INT goes inactive.

Updating of interrupt status registers ISR0…4 , GIS and CIS is only prohibited during read access.

Masked Interrupts Visible in Status Registers

The channel and global interrupt status registers indicates those interrupt status registers with active interrupt indications.

An additional mode may be selected via bit IPC.VIS.

In this mode, masked interrupt status bits neither generate an interrupt on pin INT nor are they visible in CIS and GIS, **but are displayed in the respective interrupt status register(s) ISR0..4**.

This mode is useful when some interrupt status bits are to be polled in the individual interrupt status registers.

Notes:

- *In the visible mode, all active interrupt status bits, whether the corresponding actual interrupt is masked or not, are reset when the interrupt status register is read. Thus, when polling of some interrupt status bits is desired, care must be taken that unmasked interrupts are not lost in the process.*
- *All unmasked interrupt statuses are treated as before.*

Please note that whenever polling is used, all interrupt status registers concerned have to be polled individually (no “hierarchical” polling possible), since GIS only contains information on actually generated - i.e. unmasked-interrupts.

3.3 Boundary Scan Interface

Identification Register:	32 bit
Version:	1 H
Part Number:	004D H
Manufacturer:	083 H

In QuadFALC a Test Access Port (TAP) controller is implemented. The essential part of the TAP is a finite state machine (16 states) controlling the different operational modes

of the boundary scan. Both, TAP controller and boundary scan, meet the requirements given by the JTAG standard: IEEE 1149.1. **Figure 9** gives an overview.

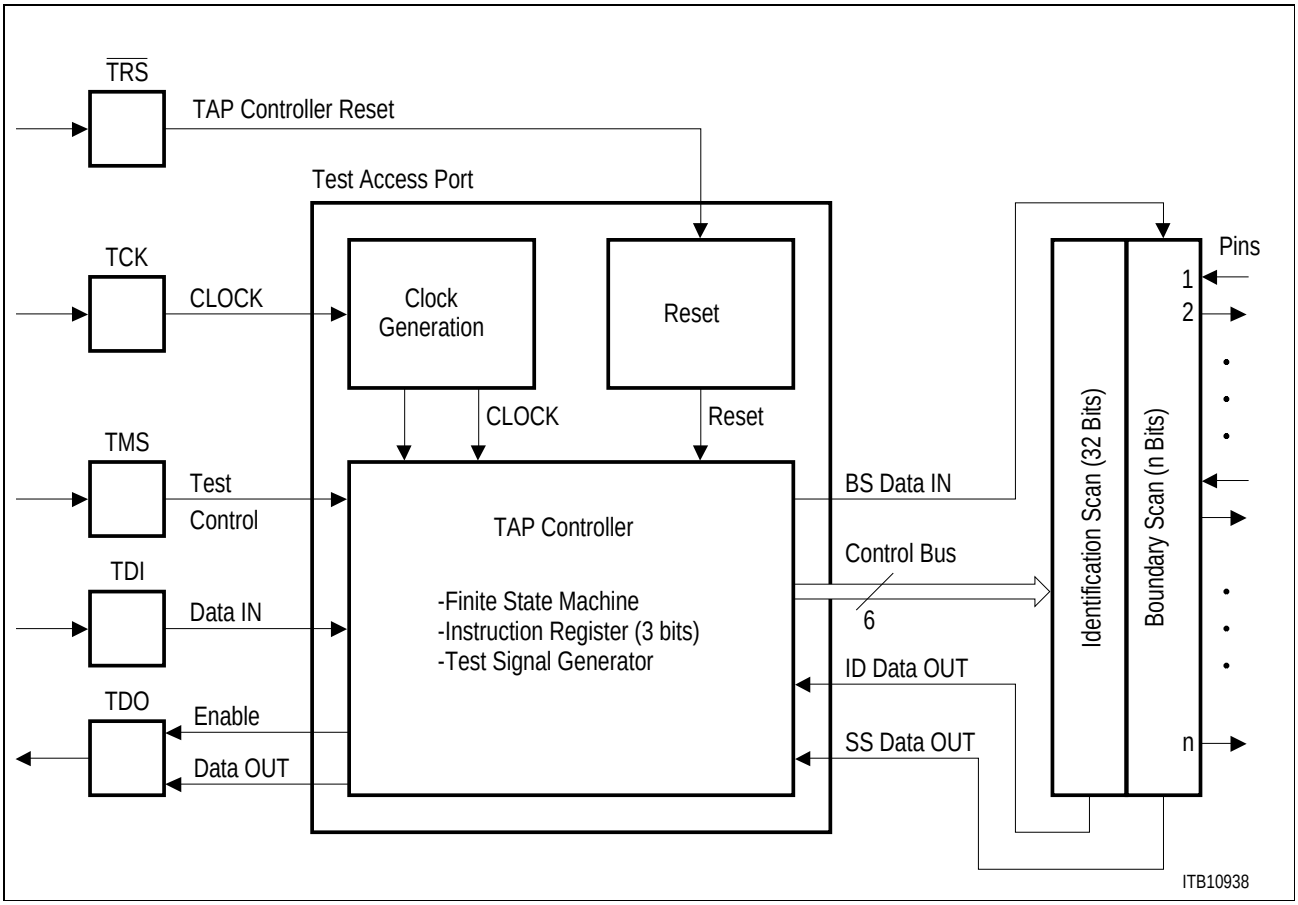


Figure 9
Block Diagram of Test Access Port and Boundary Scan

Test handling is performed via the pins TCK (Test Clock), TMS (Test Mode Select), TDI (Test Data Input) and TDO (Test Data Output). Test data at TDI are loaded with a 4-MHz clock signal connected to TCK. ‘1’ or ‘0’ on TMS causes a transition from one controller state to an other; constant ’1’ on TMS leads to normal operation of the chip.

If no boundary scan testing is planned TMS and TDI do not need to be connected since pull-up transistors ensure high input levels in this case. Nevertheless it would be a good practice to put the unused inputs to defined levels. In this case, if the JTAG is not used: TMS = TCK = ‘1’.

After switching on the device (V_{DD} = 0 to 3.3 V) pin $\overline{\text{TRS}}$ has to reset which forces the TAP controller into test logic reset state.

3.4 Receive Path

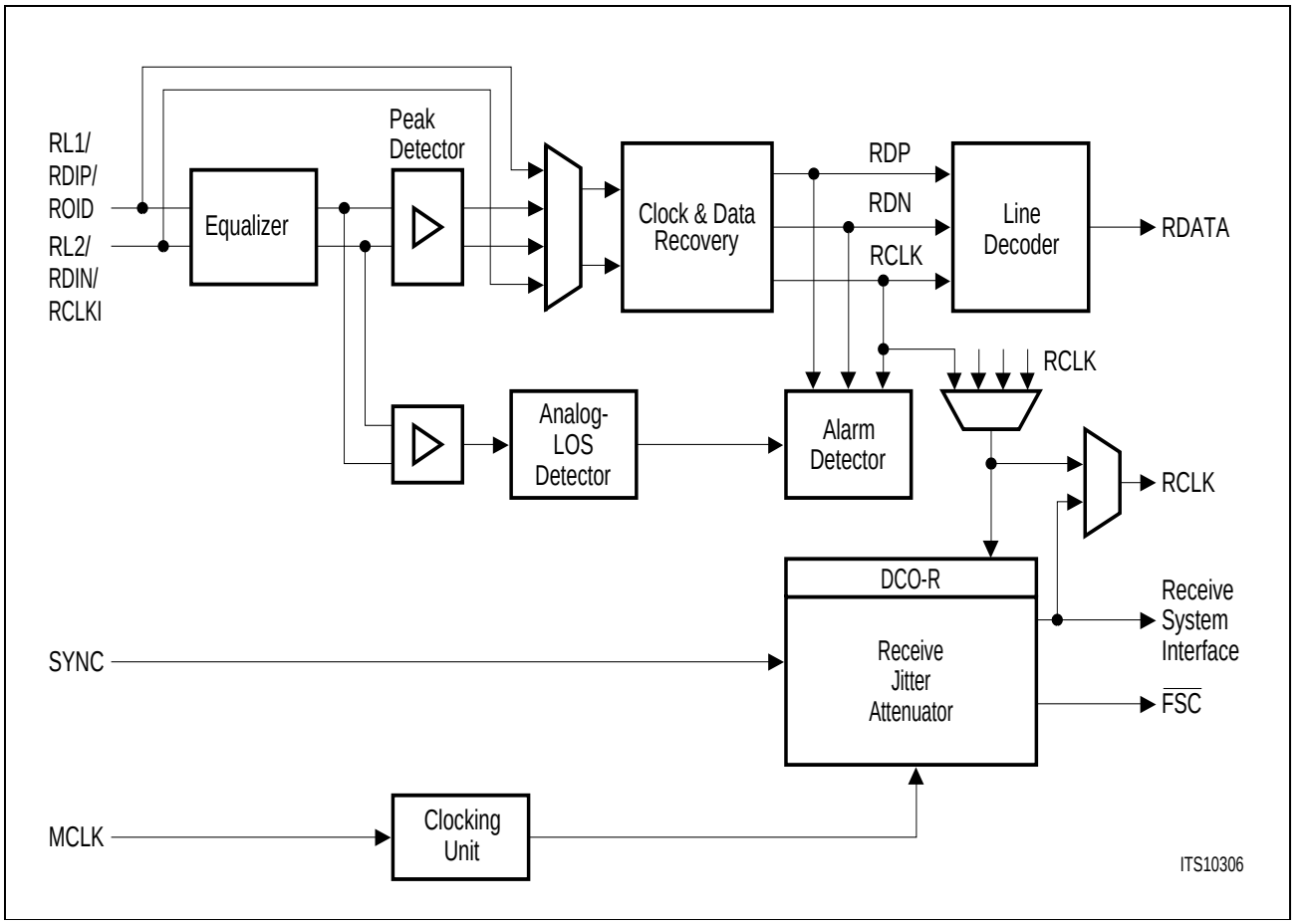


Figure 10
Receive Clock System

Receive Line Interface

For data input, three different data types are supported:

- Ternary coded signals received at multifunction ports RL1 and RL2 from a -34 dB ternary interface. The ternary interface is selected if LIM1.DRS is reset.
- Digital dual rail signals received at ports RDIP and RDIN. The dual rail interface is selected if LIM1.DRS and FMR0.RC1 is set.
- Unipolar data at port ROID received from a fibre optical interface. The optical interface is selected if LIM1.DRS is set and FMR0.RC1 is reset.

Long Haul Interface

The QuadFALC has an integrated short- and long- haul line interface, comprising a receive equalization network and noise filtering.

Receive Equalization Network

The QuadFALC automatically recovers the signals received on pins RL1/2 in a range of up to -34 dB. The maximum reachable length with a 22 AWG twisted-pair cable is 1500 m. After Reset the QuadFALC is in „Short Haul“ mode, received signals are recovered up to -10 dB of cable attenuation. Switching in „Long Haul“ mode is done by setting of register LIM0.EQON.
The integrated receive equalization network recovers signals with up to -34 dB of cable attenuation. Noise filters eliminate the higher frequency part of the received signals. The incoming data is peak detected and sliced at 55% of the peak value to produce the digital data stream. The received data is then forwarded to the clock & data recovery unit.

Receive Line Attenuation Indication

Status register RES reports the current receive line attenuation in a range from 0 to -34 dB in 25 steps of approximately 1.4 dB each. The least significant 5 bits of this register indicate the cable attenuation in dB. These 5 bits are only valid in conjunction with the most significant two bits (RES.EV1/0 = 01) .

Receive Clock and Data Recovery

The analog received signal at port RL1/2 is equalized and then peak-detected to produce a digital signal. The digital received signal at port RDIP/N is directly forwarded to the DPLL. The receive clock and data recovery extracts the route clock RCLK from the data stream received at the RL1/2, RDIP/RDIN or ROID lines and converts the data stream into a single rail, unipolar bit stream. The clock and data recovery works with the internally generated high frequency clock based on MCLK. Normally the clock that is output via pin RCLK is the recovered clock from the signal provided by RL1/2 or RDIP/N has a duty cycle close to 50 %. The free run frequency is defined by MCLK = 2.048 MHz in periods with no signal. The intrinsic jitter generated in the absence of any input jitter is not more than 0.035 UI. In digital bipolar line interface mode the clock and data recovery will accept only HDB3 coded signals with 50 % duty cycle.

Receive Line Coding

The HDB3 line code or the AMI coding is provided for the data received from the ternary or the dual rail interface. In case of the optical interface a selection between the NRZ code and the CMI Code (1T2B) with HDB3 postprocessing is provided. If CMI code (1T2B) is selected the receive route clock will be recovered from the data stream. The 1T2B decoder does not correct any errors. In case of NRZ coding data will be latched with the falling edge of pin RCLKI. The HDB3 code is used along with double violation detection or extended code violation detection (selectable). In AMI code all code violations will be detected.
The detected errors increment the code violation counter (16 bits length).

When using the optical interface with NRZ coding, the decoder is by-passed and no code violations will be detected.

The signal at the ternary interface is received at both ends of a transformer.

The operating modes 75 or 120 Ω are selectable by switching resistors in parallel. This selection does not require changing transformers.

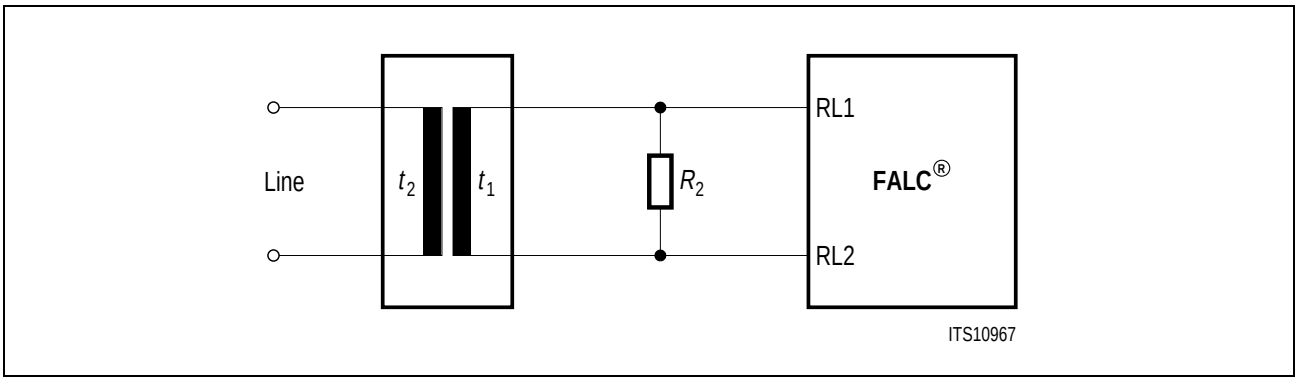


Figure 11
Receiver Configuration

Recommended Receiver Configuration Values

Parameter	Characteristic Impedance [Ω]	
	120	**75**
R_1 (± 1 %) [Ω]	100-120	75
$t_2 : t_1$	1 : 1	1 : 1

Loss of Signal Detection

There are different definitions for detecting Loss of Signal (LOS) alarms in the ITU-T G.775 and ETS 300233. The QuadFALC covers all these standards. The LOS indication is performed by generating an interrupt (if not masked) and activating a status bit. Additionally a LOS status change interrupt is programmable via register IPC.SCI.

- Detection:
  An alarm will be generated if the incoming data stream has no pulses (no transitions) for a certain number (N) of consecutive pulse periods. “No pulse” in the digital receive interface means a logical zero on pins RDIP/RDIN/ROID. A pulse with an amplitude less than Q dB below nominal is the criteria for “no pulse” in the analog receive interface (LIM1.DRS=0). The receive signal level Q is programmable via three control bits LIM1.RIL2-0 in a range of about 900 to 50 mV differential voltage between pins RL1/2. The number N can be set via an 8 bit register PCD. The contents of the PCD register will be multiplied by 16, which results in the number of pulse periods or better, the time which has to suspend until the alarm has to be detected. The range results

therefore from 16 to 4096 pulse periods. ETS300233 requires detection intervals of at least 1 ms. This time period results always in a LFA (Loss of Frame Alignment) before a LOS will be detected.

- Recovery:
  In general the recovery procedure starts after detecting a logical ‘one’ (digital receive interface) or a pulse (analog receive interface) with an amplitude more than Q dB (defined by LIM1.RIL2-0) of the nominal pulse. The value in the 8 bit register PCR defines the number of pulses (1 to 255) to clear the LOS alarm. Additional recovery conditions may be programmed by register LIM2.

Receive Jitter Attenuator

The receive jitter attenuator is placed for each channel in the receive path. The working clock is an internally generated high frequency clock based on the clock provided on pin MCLK (2.048 MHz). The jitter attenuator meets the requirements of ITU-T I.431, G. 736-739, G.823 and ETSI TBR12/13.

The internal PLL circuitry DCO-R generates an „jitterfree“ output clock which is directly dependent on the phase difference of the incoming clock and the jitter attenuated clock.The receive jitter attenuator could be either synchronized to the extracted receive clock RCLK or to a 2.048 MHz clock provided on pin SYNC. The received data is written into the receive elastic buffer with RCLK and are read out with the dejittered clock sourced by DCO-R. The jitter attenuated clock could be output via pins RCLK or SCLKR. Optionally a 8 kHz clock is provided on pin SEC/FSC.

The DCO-R circuitry attenuates the incoming jittered clock starting at 2 Hz jitter frequency with 20 dB per decade fall off. Wander with a jitter frequency below 2 Hz will be passed unattenuated. The intrinsic jitter in the absence of any input jitter is < 0.02 UI.

For some applications it might be useful starting of jitter attenuation at lower frequencies. Therefore the corner frequency is switchable by the factor of ten downto 0.2 Hz (LIM2.SCF).

The DCO-R circuitry is automatically centered to the nominal bit rate if the reference clock on pin SYNC / RCLK is missed for two 2.048 MHz clock periods. This center function of DCO-R may be optionally disabled (CMR2.DCF = 1) in order to accept a gapped reference clock. In analog line interface mode the RCLK is always running. Only in digital line interface mode with single rail data a gapped clock may occur.

The receive jitter attenuator works in two different modes:

- Slave mode
  In Slave mode (LIM0.MAS = 0) the DCO-R will be synchronized to the recovered route clock. In case of LOS the DCO-R switches automatically to Master mode. If bit CMR1.DCS is set automatic switching from RCLK to SYNC is disabled.
- Master mode
  In Master mode (LIM0.MAS = 1) the jitter attenuator is in free running mode if no clock on pin SYNC is supplied. If a c2.048 MHz clock at the SYNC input is applied the DCO-R will synchronize to this input.

The following table shows the clock modes with the corresponding synchronization sources.

Mode	Internal LOS Active	SYNC Input	System Clocks generated by DCO-R
Master	independent	Fixed to VDD	DCO-R centered, if CMR2.DCF =0. (CMR2.DCF should not be set)
Master	independent	2 MHz	Synchronized on SYNC input (external 2 MHz)
Slave	no	Fixed to VDD	Synchronized on Line RCLK1-4 , selected by CMR1.DRSS1/0
Slave	no	2 MHz	Synchronized on Line RCLK1-4 , selected by CMR1.DRSS1/0
Slave	yes	Fixed to VDD	CMR1.DCS = 0: DCO-R is centered, if CMR2.DCF = 0. (CMR2.DCF should not be set)
			CMR1.DCS = 1: Synchronized on Line RCLK1-4, selected by CMR1.DRSS1/0
Slave	yes	2 MHz	CMR1.DCS = 0: Synchronized on SYNC input (external 2.048 MHz)
			CMR1.DCS = 1: Synchronized on Line RCLK1-4, selected by CMR1.DRSS1/0

The jitter attenuator meets the jitter transfer requirements of the Rec. I.431 and G.735-739 (refer to **figure 12**).

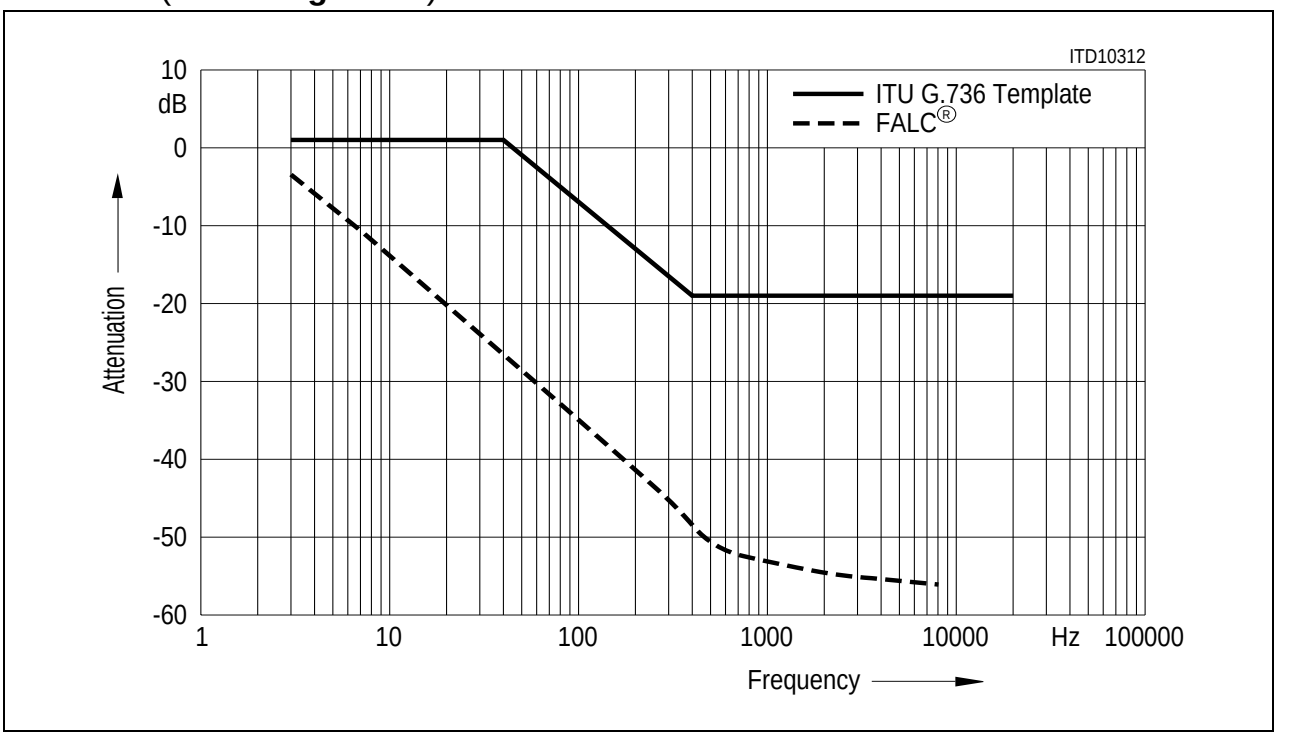


Figure 12
Jitter Attenuation Performance

Also the requirements of ETSI TBR12/13 will be satisfied. Insuring adequate margin against TBR12/13 output jitter limit with 15 UI input at 20 Hz the DCO-R circuitry will start jitter attenuation at nearly 2 Hz.

Jitter Tolerance

The QuadFALC receiver's tolerance to input jitter complies to ITU for CEPT application.

Figure 13 shows the curves of different input jitter specifications stated below as well as the QuadFALC performance.

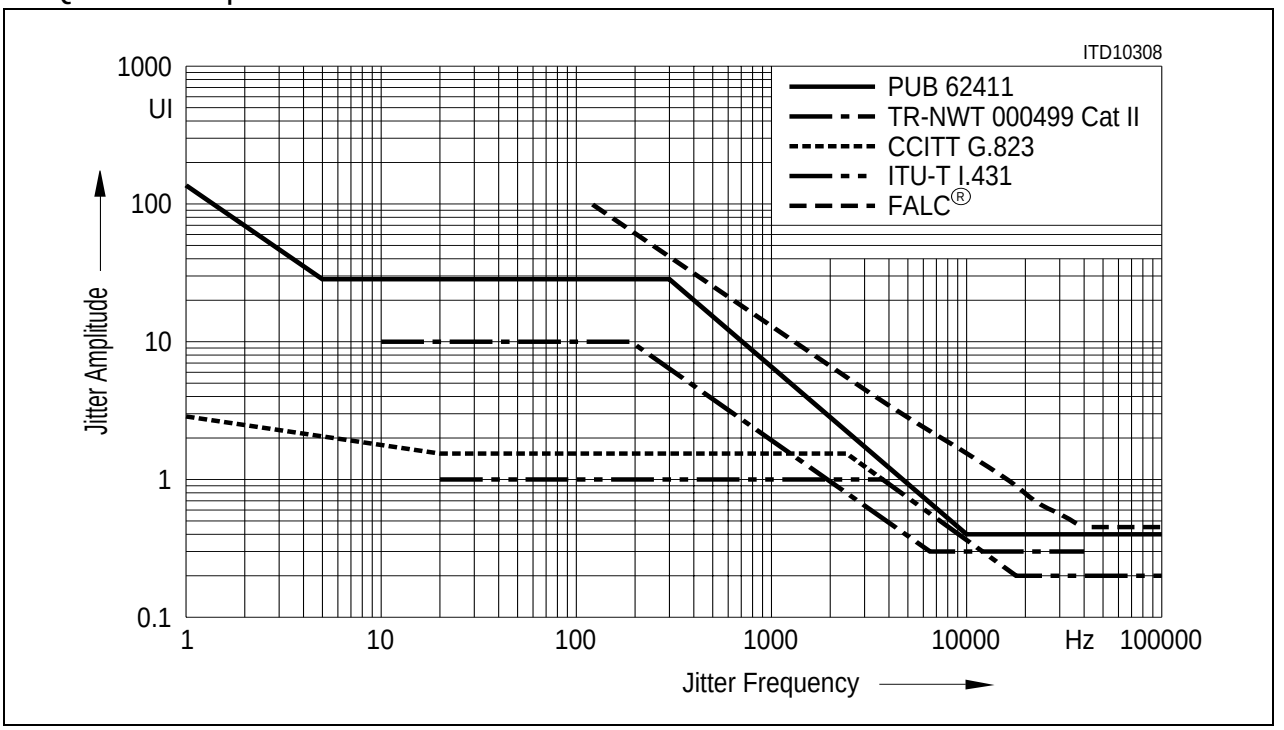


Figure 13
Jitter Tolerance

Output Jitter

In the absence of any input jitter the QuadFALC generates the output jitter, which is specified in the table below..

Specification	Measurement Filter Bandwidth		Output Jitter (UI peak to peak)
	Lower Cutoff	Upper Cutoff	
ITU-T I.431	20 Hz	100 kHz	< 0.015
	700 Hz	100 kHz	< 0.015

Transmit jitter attenuator

The transmit jitter attenuator DCO-X circuitry generates a „jitterfree" transmit clock for each channel and meets the following requirements: ITU-T I.431, G. 703, G. 736-739, G.823 and ETSI TBR12/13. The DCO-X circuitry works internally with the same high frequency clock as the receive jitter attenuator it does. It synchronizes either to the working clock of the transmit backplane interface or the clock provided by pin TCLK or

the receive clock RCLK (remote loop / loop-timed). The DCO-X attenuates the incoming clock jitter starting at 2 Hz with 20 dB per decade fall off. With the jitter attenuated clock, which is directly dependent on the phase difference of the incoming clock and the jitter attenuated clock, data is read from the transmit elastic buffer (2 frames) or from the JATT buffer (2 frames, remote loop) Wander with a jitter frequency below 2 Hz are passed transparently.

The DCO-X accepts gapped clocks which are used in ATM or SDH/SONET applications. The jitter attenuated clock is output by pin XCLK.

The transmit jitter attenuator could be disabled. In that case data is read from the transmit elastic buffer with the clock sourced by pin TCLK (2.048 or 8.192 MHz). Synchronization between SCLKX and TCLK has to done externally.

In the loop-timed clock configuration (LIM2.ELT) the DCO-X circuitry generates a transmit clock which is frequency synchronized to RCLK. In this configuration the transmit elastic buffer has to be enabled.

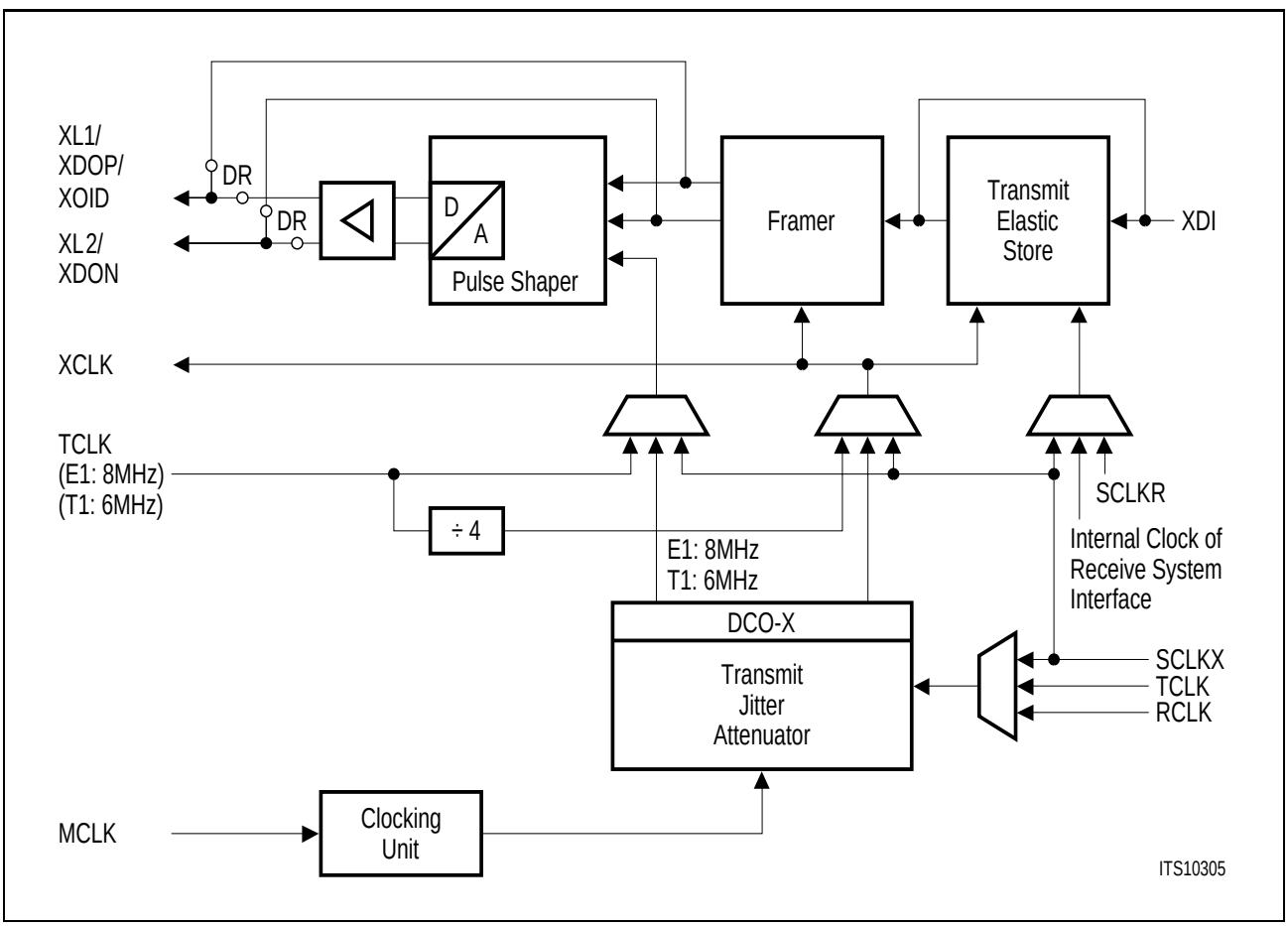


Figure 14
Transmit Clock System

Note: DR = Dual Rail Interface
DCO-X Digital Controlled Oscillator Transmit

Framer/Synchronizer

The following functions are performed:

- Synchronization on pulse frame and multiframe
- Error indication when synchronization is lost. In this case, AIS is automatically sent to the system side and Remote Alarm to the remote end if en/disabled.
- Initiating and controlling of resynchronization after reaching the asynchronous state. This may be automatically done by the QuadFALC, or user controlled via the microprocessor interface.
- Detection of remote alarm indication from the incoming data stream.
- Separation of service bits and data link bits. This information is stored in status registers.
- Generation of various maskable interrupt statuses of the receiver functions.
- Generation of control signals to synchronize the CRC checker, and the receive elastic buffer.

If programmed and applicable to the selected multiframe format, CRC checking of the incoming data stream is done by generating check bits for a CRC submultiframe according to the CRC 4 procedure (**refer to ITU-T Rec. G704**). These bits are compared with those check bits that are received during the next CRC submultiframe. If there is at least one mismatch, the CRC error counter (16 bit) will be incremented.

Receive Elastic Buffer

The received bit stream is stored in the receive elastic buffer. The memory is organized as a two-frame elastic buffer with a maximum size of 64 $\times$ 8 bit. The size of the elastic buffer can be independently configured for the receive and transmit direction. Programming of the receive buffer size is done by SIC1.RBS1/0 :

- RBS1/0 = 00 : two frame buffer or 512 bits
  Maximum of wander amplitude (peak-to-peak): 190 UI (1 UI = 488 ns)
  average delay after performing a slip: 1 frame or 256 bits
- RBS1/0 = 01 : one frame buffer or 256 bits
  Max. wander amplitude: 100 UI
  average delay after performing a slip: 128 bits, ($\overline{\text{SYPR}}$ = output)
- RBS1/0 = 10 : short buffer or 96 bits :
  Max. wander amplitude: 38 UI
  average delay after performing a slip: 48 bits, ($\overline{\text{SYPR}}$ = output)
- RBS1/0 = 11 : Bypass of the receive elastic buffer

The functions are:

- Clock adaption between system clock (SCLKR) and internally generated route clock (RCLK).
- Compensation of input wander and jitter.
- Frame alignment between system frame and receive route frame

- Reporting and controlling of slips

Controlled by special signals generated by the receiver, the unipolar bit stream is converted into bit-parallel data which is circularly written to the elastic buffer using internally generated Receive Route Clock (RCLK).

Reading of stored data is controlled by the System Clock sourced by SCLKR or by the receive jitter attenuator and the Synchronous Pulse ($\overline{\text{SYPR}}$) in conjunction with the programmed offset values for the receive time-slot/clock-slot counters. After conversion into a serial data stream, the data is given out via port RDO. If the receive buffer is bypassed programming of the time-slot offset is disabled and data is clocked off with RCLK instead of SCLKR.

In one frame or short buffer mode the delay through the receive buffer is reduced to an average delay of 128 or 46 bits. In bypass mode the time-slot assigner is disabled. In this case $\overline{\text{SYPR}}$ programmed as input is ignored. Slips will be performed in all buffer modes except the bypass mode. After a slip is detected the read pointer is adjusted to one half of the current buffer size.

The following table gives an overview of the receive buffer operating mode .

Buffer Size (SIC1.RBS1/0)	**TS Offset program.** (RC1/0) + $\overline{\text{SYPR}}$ = input	**Slip perform.**
bypass[1)]	disabled recom. $\overline{\text{SYPR}}$ = output	no
short buffer	not recommended, recom. $\overline{\text{SYPR}}$ = output	yes
1 frame	not recommended, recom. $\overline{\text{SYPR}}$ = output	yes
2 frames	enabled	yes

1) In bypass mode the clock provided on pin SCLKR is ignored. Clocking is done with RCLK.

In single frame mode (SIC1. RBS) , values of receive time-slot offset (RC1/0) have to be specified great enough to prevent too great approach of frame begin (line side) and frame begin (system side).

Figure 15 gives an idea of operation of the receive elastic buffer:
A slip condition is detected when the write pointer (W) and the read pointer (R) of the memory are nearly coincident, i.e. the read pointer is within the slip limits (S +, S –). If a slip condition is detected, a negative slip (one frame or one half of the current buffer size is skipped) or a positive slip (one frame or one half of the current buffer size is read out twice) is performed at the system interface, depending on the difference between RCLK and the current working clock of the receive backplane interface. i.e. on the position of

pointer R and W within the memory. A positive / negative slip is indicated in the interrupt status bits ISR3.RSP and ISR3.RSN.

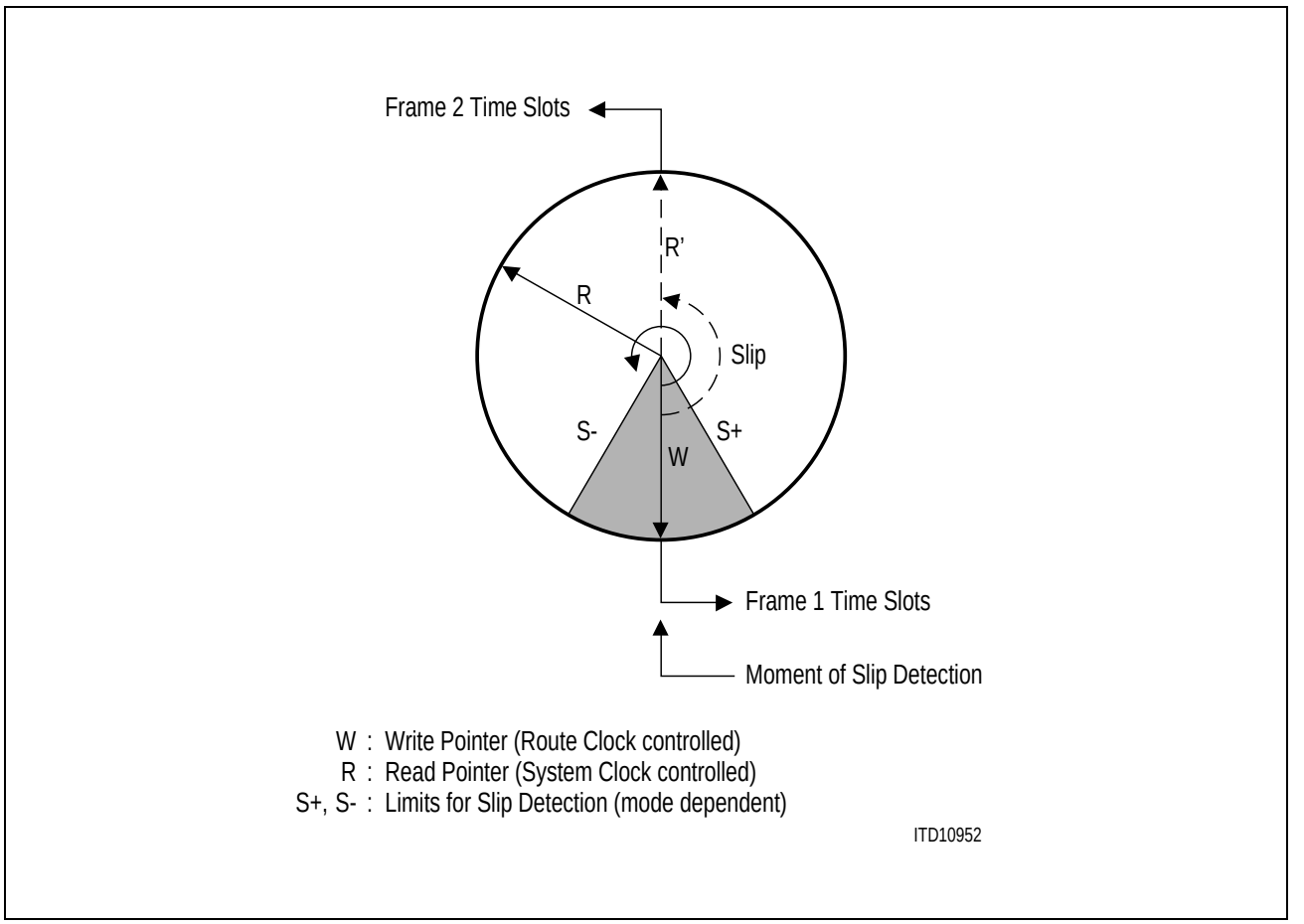


Figure 15
The Receive Elastic Buffer as Circularly Organized Memory

Receive Signaling Controller

Each of the four signaling controller can be programmed to operate in various signaling modes. The QuadFALC will perform the following signaling and data link methods:

- **HDLC or LAPD access**
  In case of common channel signaling the signaling procedure HDLC/SDLC or LAPD according to Q.921 will be supported. The signaling controller of the QuadFALC performs the FLAG detection , CRC checking, address comparisson and zero bit-removing. The received data flow and the address recognition features can be performed in very flexible way, to satisfy almost any practical requirements. Depending on the selected address mode, the QuadFALC performs a 1 or 2 byte address recognition. If a 2-byte address field is selected, the high address byte is compared with the fixed value FEH or FCH (group address) as well as with two individually programmable values in RAH1 and RAH2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address will be interpreted as COMMAND/RESPONSE bit (C/R) and will be excluded from the address comparison. Buffering of receive data is done in a 64 byte deep RFIFO. Refer also to **chapter 4.1**.
  In signaling controller transparent mode, fully transparent data reception without HDLC framing is performed, i.e. without FLAG recognition, CRC checking or bit-stuffing. This allows user specific protocol variations.
  The QuadFALC offers the flexibility to extract data during certain time-slots. Any combination of time-slots may be programmed independently for the receive and transmit direction.
- **S_a bit Access**
  The QuadFALC supports the S_a bit signaling of time-slot 0 of every other frame as follows:
  - the access via registers RSW
  - the access via registers RSA4-8, capable of storing the information for a complete multiframe
  - the access via the 64 byte deep receive FIFO of the signaling controller. This S_a bit access gives the opportunity to receive a transparent bit stream as well as HDLC frames where the signaling controller automatically processes the HDLC protocol. Any combination of S_a bits which should be extracted and stored in the RFIFO may be selected by XC0.SA8-4. The access to the RFIFO is supported by ISR0.RME / RPF.
- **Channel Associated Signaling CAS**
  The signaling information is carried in time-slot 16 (TS16). Receive data is stored in registers RS1-16 on the CAS multiframe boundary. The signaling controller samples the bit stream either on the receive line side or if external signaling is enabled on the receive system side. External signaling is enabled by selecting the RSIG pinfunction via register PC1-4.
  Optionally the complete CAS multiframe may be transmitted on pin RSIG. The signaling data is clocked out with the working clock of the receive highway (SCLKR) in conjunction with the rec. synchron. pulse ($\overline{\text{SYPR}}$). Data on RSIG will be transmitted

in the last 4 bits per time-slot and are aligned to the data on RDO. The first 4 bits per time-slot could be optionally fixed high or low, except time-slot 0 and 16. In time-slot 0 the FAS / NFAS word is transmitted, in time-slot 16 the CAS multiframe pattern. Data on RSIG are only valid if the freeze signaling status is inactive. With FMR1.SAIS an all ones may be transmitted on RDO and RSIG.

The signaling procedure will be done as it is described in ITU-T G.704 and G.732.
The main functions are:
- Synchronization to a CAS multiframe
- Detection of AIS and Remote Alarm in CAS multiframes
- Separation of CAS Service bits X1-X3
- Storing of received signaling data in registers RS1-16 with last look capability

Updating of the received signaling information is controlled by the freeze signaling status. The freeze signaling status is automatically activated if a Loss of Signal, or a Loss of CAS Multiframe Alignment or a receive slip occurs. The current freeze status is output on port FREEZ (RPA-D) and indicated by register SIS.SFS. If SIS.SFS is active updating of the registers 1-16 is disabled. Optionally automatic freeze signaling may be disabled by setting bit SIC3.DAF.
To relieve the µP load from always reading the complete RS1-16 buffer every 2 msec the QuadFALC notifies the µP via interrupt ISR0.CASC only when signaling changes from one multiframe to the next. Additionally the QuadFALC generates a receive signaling data change pointer (RSP1/2) which directly points to the updated RS1-16 register .

3.5 System Interface

The QuadFALC offers a flexible feature for system designers where for transmit and receive direction different system clocks and system pulses are necessary. The interface to the receive system highway is realized by two data buses, one for the data RDO and one for the signaling data RSIG. The receive highway is clocked via pin SCLKR, while the interface to the transmit system highway is independently clocked via pin SCLKX. The frequency of these working clocks and the data rate of 2.048 / 4.096 / 8.192 / 16.384 MBit/s for the receive and transmit system interface is programmable by SIC1.SSC1/0 , and SIC1.SSD1, FMR1.SSD0. Selectable system clock and data rates and their valid combinations are shown in the table below

Table 4
System Clocking and Data Rates

System Data Rate	Clock Rate 2.048 MHz	Clock Rate 4.096 MHz	Clock Rate 8.192 MHz	Clock Rate 16.384 MHz
2.048 MBit/s	x	x	x	x
4.096 MBit/s	--	x	x	x
8.192 MBit/s	--	--	x	x
16.384 MBit/s	--	--	--	x

x = valid , -- = invalid

Generally the data or marker on the system interface are clocked off or latched on the rising or falling edge (SIC3.RESR/X) of the SCLKR/X clock. Some clocking rates allow transmitting of time-slots in different channel- phases. Each channel-phase which should be active on ports RDO, XDI, RP(A-D) and XP(A-D) is programmable by SIC2.SICS2-0, the remaining channel-phases are cleared or ignored.
The signals on pin $\overline{\text{SYPR}}$ in conjunction with the assigned timeslot offset in register RC0 and RC1 will define the beginning of a frame on the receive system highway.The signal on pin $\overline{\text{SYPX}}$ in conjunction with the assigned timeslot offset in register XC0 and XC1 will define the beginning of a frame on the transmit system highway.

Adjusting the frame begin (time-slot 0, bit 0) relative to $\overline{\text{SYPR/X}}$ is possible in the range of 0 - 125 µsec. The minimum shift of varying the time-slot 0 begin could be programmed between 1 bit and 1/8 bit depending of the system clocking and data rate. e.g. with a clocking / data rate of 2.048 MHz shifting is done bitwise, while running the QuadFALC with 16.384 MHz and 2.048 MBit/s data rate it is done by 1/8 bit.

A receive frame marker RFM could be activated during any bit position of the entire frame. Programming is done with registers RC1/0. The pin function RFM is selected by PC(1-4).RPC(2-0) = 001. The RFM selection disables the internal time-slot assigner, no offset programming is performed. The receive frame marker is active high for one

2.048 MHz cycle and is clocked off with the rising or falling edge of the clock which is in/output on port SCLKR.

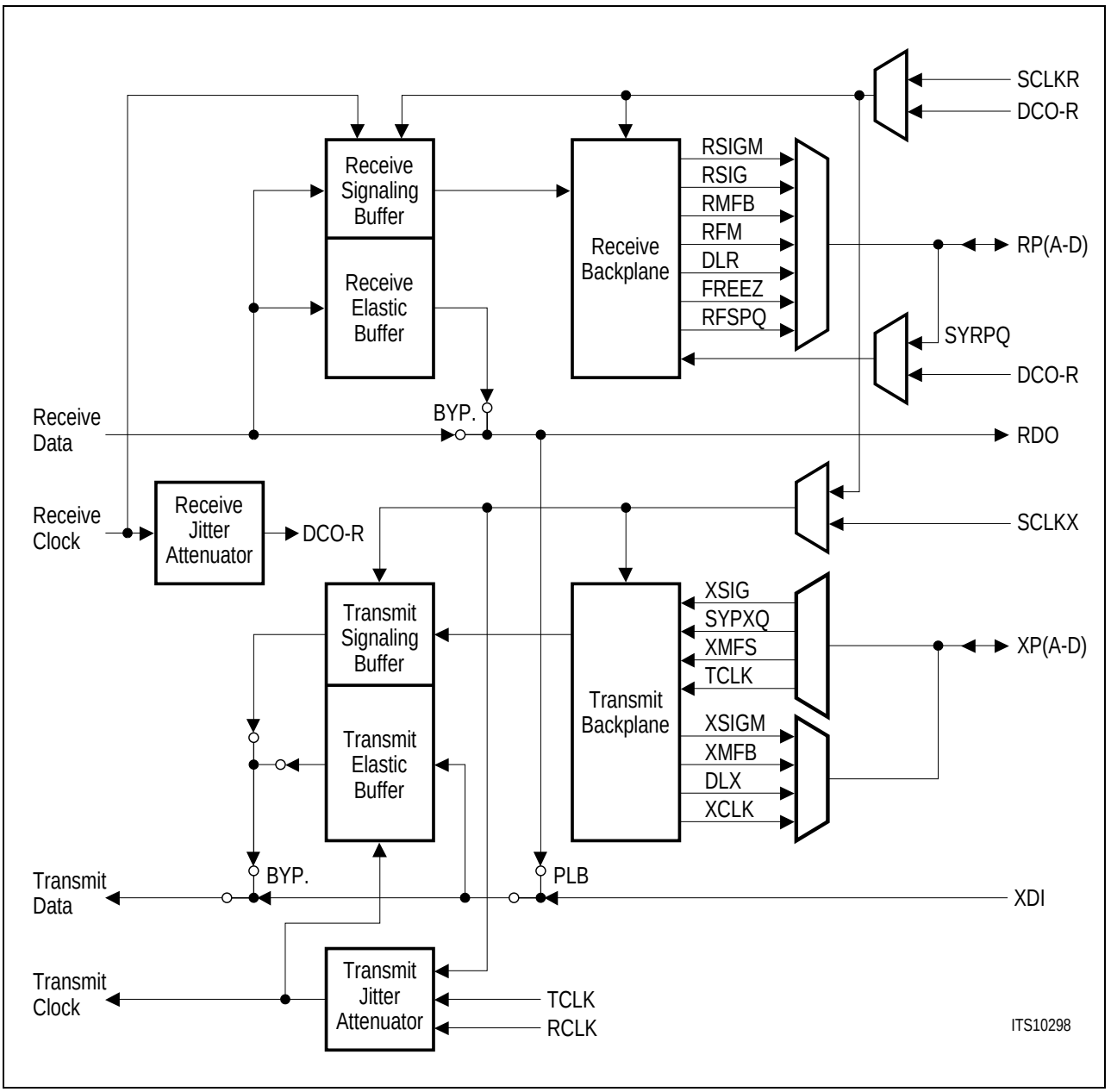


Figure 16
System Interface

System Interface Multiplex Mode

Setting this bit enables a single rail data stream of 16.384 or 8.192 MBit/s containg all four E1 frames. The receive system interface for all four channels is running with the clock provided on SCLKR1 and the frame sync pulse provided on $\overline{\text{SYPR1}}$. The transmit system interface is running with SCLKX1 and $\overline{\text{SYPX1}}$. Data will be transmitted / accepted

in a byte or bit interleaved format. Bit interleaving is valid with the 16.384 or 8.192 MHz clocking rates. All four single channel FALCs(1-4) have to be configured equally with the following parameters:

- clocking rate : 16.384 / 8.192 MHz , SIC1.SSC1/0
- data rate : 16.384 / 8.192 MBit/s, SIC1.SSD1, FMR1.SSD0
- time-slot offset programming : RC1/0 , XC1/0
- receive buffer size : SIC1.RBS1/0 = 00 (2 frames)

The multiplexed data stream is internal logically ored. Therefore the selection of the active channel phase have to be configured different for each single channel FALC. Programming is done with SIC2.SICS2-0.

In system interface multiplex mode signals on RDO2-4 and RSIG2-4 are undefined, while signals on SCLKR2-4, $\overline{\text{SYPR}}$2-4, SCLKX2-4, $\overline{\text{SYPX}}$2-4, XDI2-4 and XSIG2-4 are ignored.

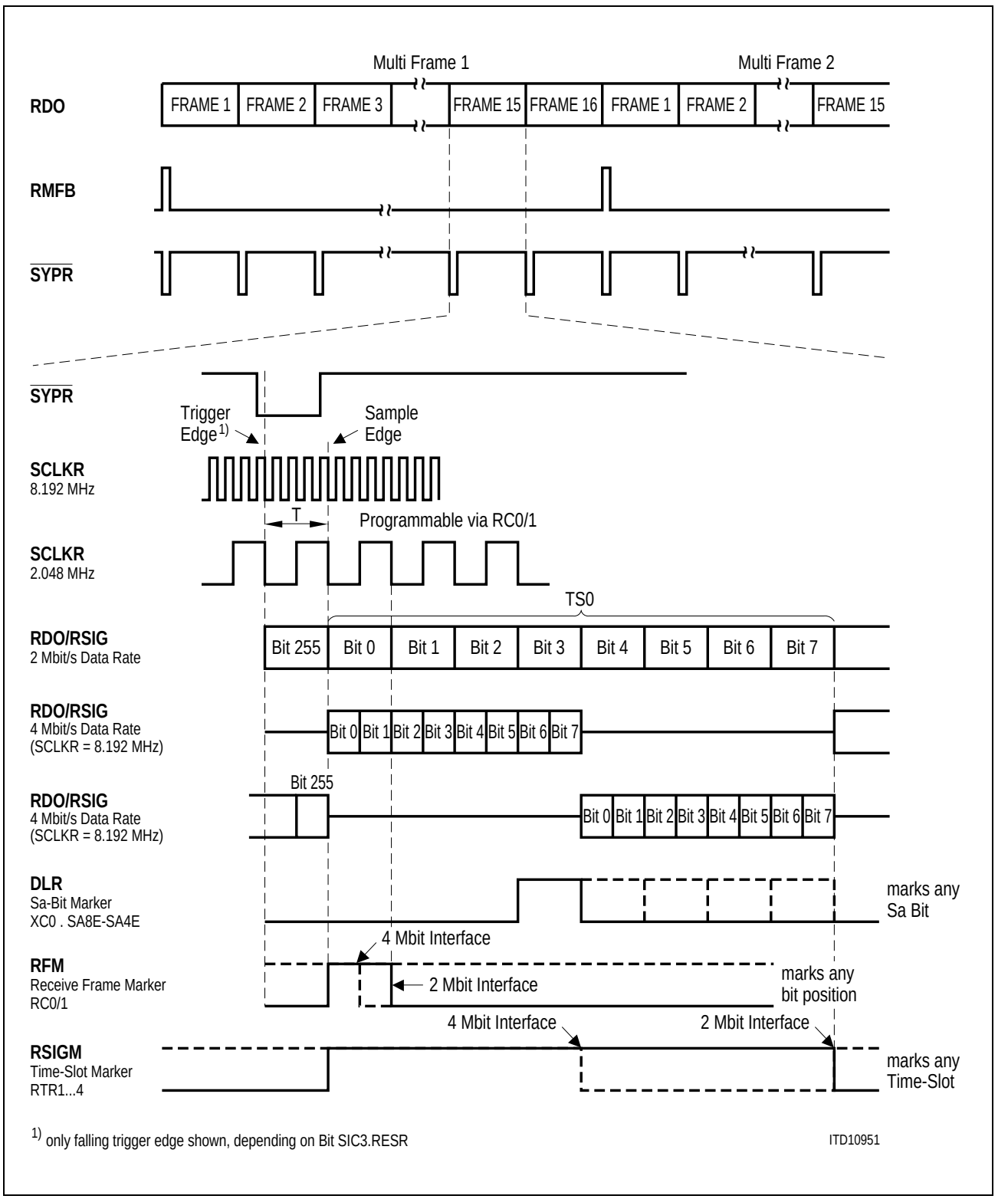


Figure 17
Receive System Interface Clocking

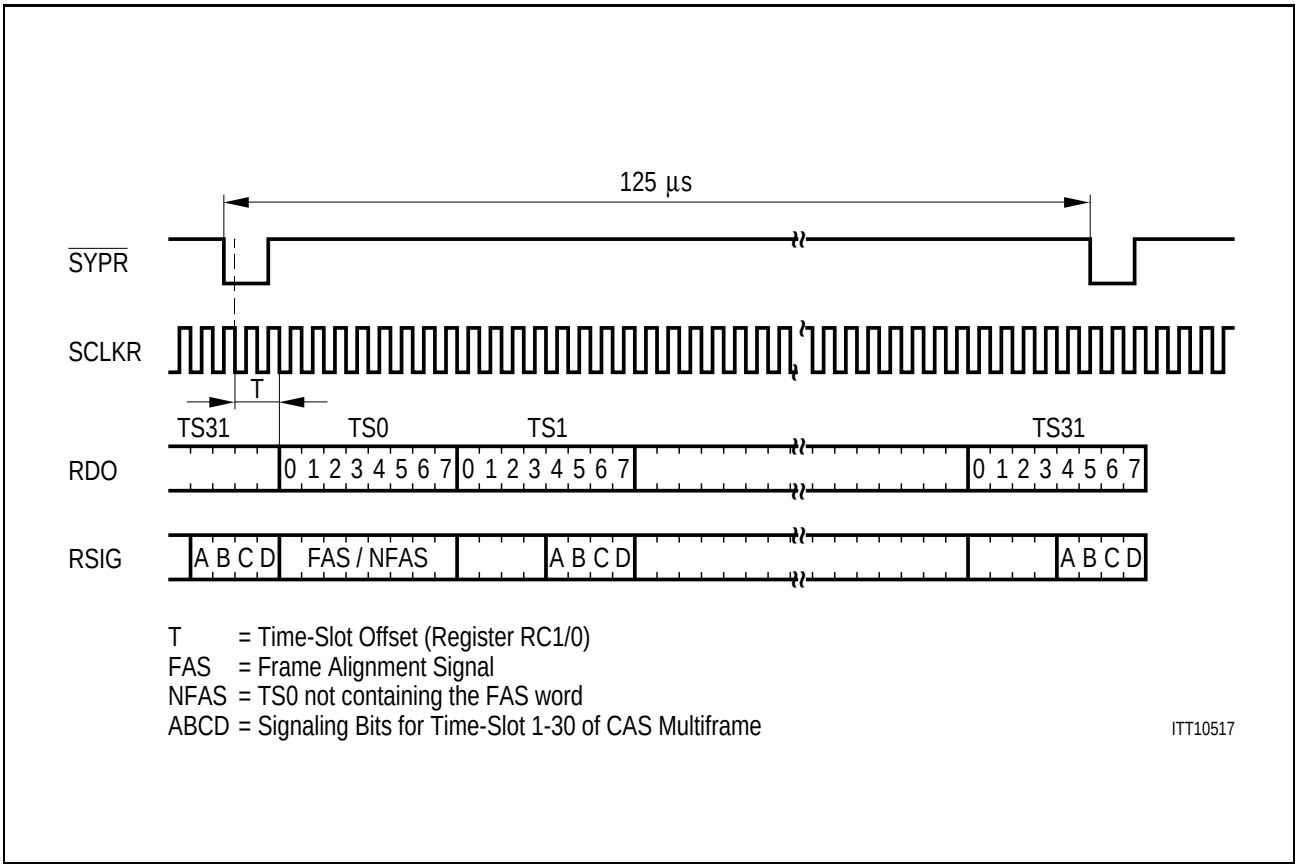


Figure 18
2.048 MHz Receive Signaling Highway

Time-Slot Assigner

The QuadFALC offers the flexibility to connect data during certain time-slots, as defined by registers RTR1-4 and TTR1-4, to the RFIFO and XFIFO, respectively. Any combinations of time-slots can be programmed for the receive and transmit directions. If CCR1.EITS = 1 the selected time-slots (RTR1-4) will be stored in the RFIFO of the signaling controller and the XFIFO contents will be inserted into the transmit path as controlled by registers TTR1-4.

Table 5
Time-Slot Assigner

Receive Time-Slot Register	Transmit Time-Slot Register	Time-Slots
RTR1.7	TTR1.7	0
RTR1.6	TTR1.6	1
RTR1.5	TTR1.5	2
RTR1.4	TTR1.4	3
RTR1.3	TTR1.3	4
RTR1.2	TTR1.2	5
RTR1.1	TTR1.1	6
RTR1.0	TTR1.0	7
RTR2.7	TTR2.7	8
RTR2.6	TTR2.6	9
RTR2.5	TTR2.5	10
RTR2.4	TTR2.4	11
RTR2.3	TTR2.3	12
RTR2.2	TTR2.2	13
RTR2.1	TTR2.1	14
RTR2.0	TTR2.0	15
RTR3.7	TTR3.7	16
RTR3.6	TTR3.6	17
RTR3.5	TTR3.5	18
RTR3.4	TTR3.4	19
RTR3.3	TTR3.3	20
RTR3.2	TTR3.2	21
RTR3.1	TTR3.1	22
RTR3.0	TTR3.0	23
RTR4.7	TTR4.7	24
RTR4.6	TTR4.6	25
RTR4.5	TTR4.5	26
RTR4.4	TTR4.4	27
RTR4.3	TTR4.3	28
RTR4.2	TTR4.2	29
RTR4.1	TTR4.1	30
RTR4.0	TTR4.0	31

3.6 Transmit Path

Compared to the receive paths the inverse functions are performed for the transmit direction.

The interface to the transmit system highway is realized by two data buses, one for the data XDI and one for the signaling data XSIG. The time-slot assignment is equivalent to the receive direction.

Latching of data is controlled by the System Clock (SCLKX) and the Synchronous Pulse ($\overline{\text{SYPX}}$ / XMFS) in conjunction with the programmed offset values for the Transmit Time-slot/Clock-slot Counters XC1/0. The frequency of the working clock of 2.048 / 4.096 / 8.192 / 16.384 MHz for the transmit system interface is programmable by SIC1.SSC1/0. Refer also **table 4**.

The received bit stream on ports XDI and XSIG could be multiplexed internally on a time-slot basis, if enabled by SIC3.TTRF = 1. The data received at port XSIG could be sampled if the transmit signaling marker XSIGM is active high. Data at port XDI will be sampled if XSIGM is low for the respective time-slot. Programming the XSIGM marker is done with registers TTR1-4.

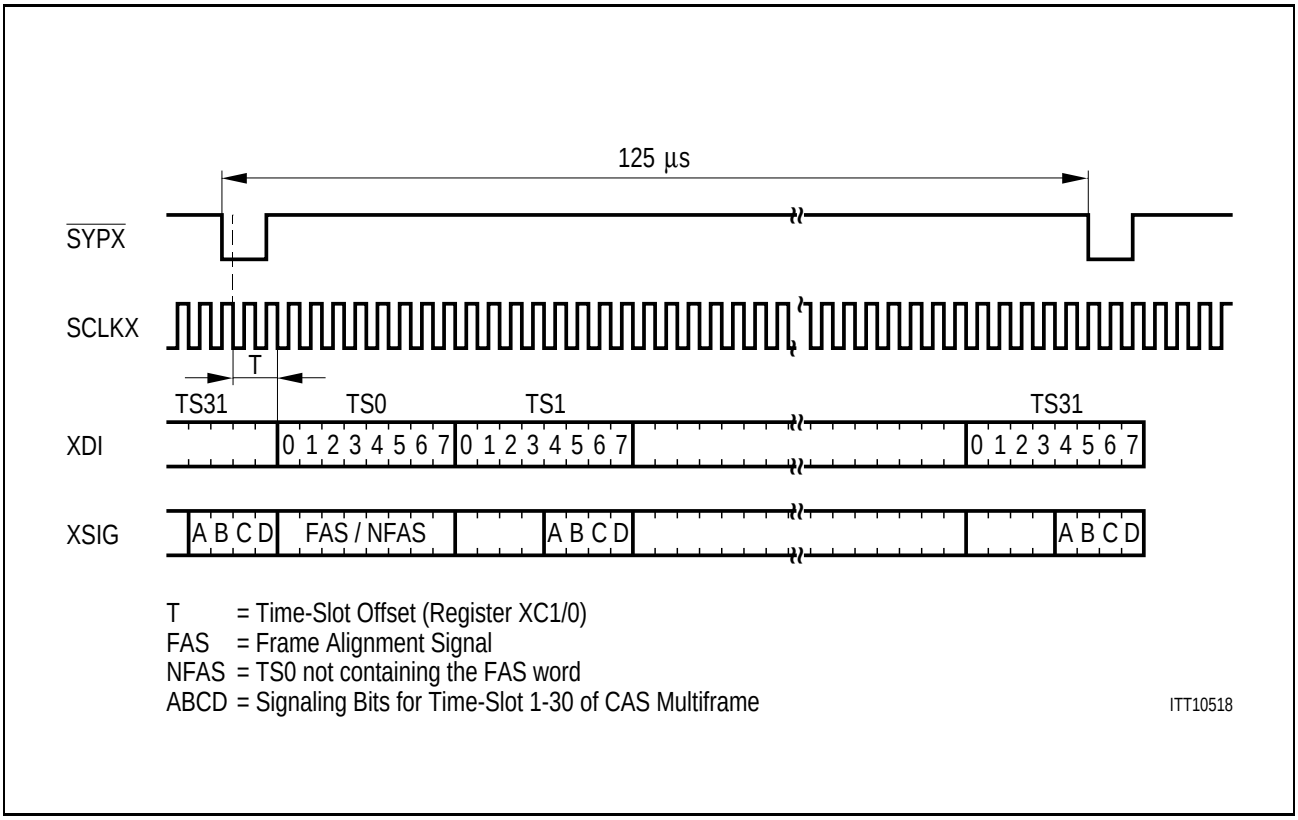


Figure 19
2.048 MHz Transmit Signaling Highway

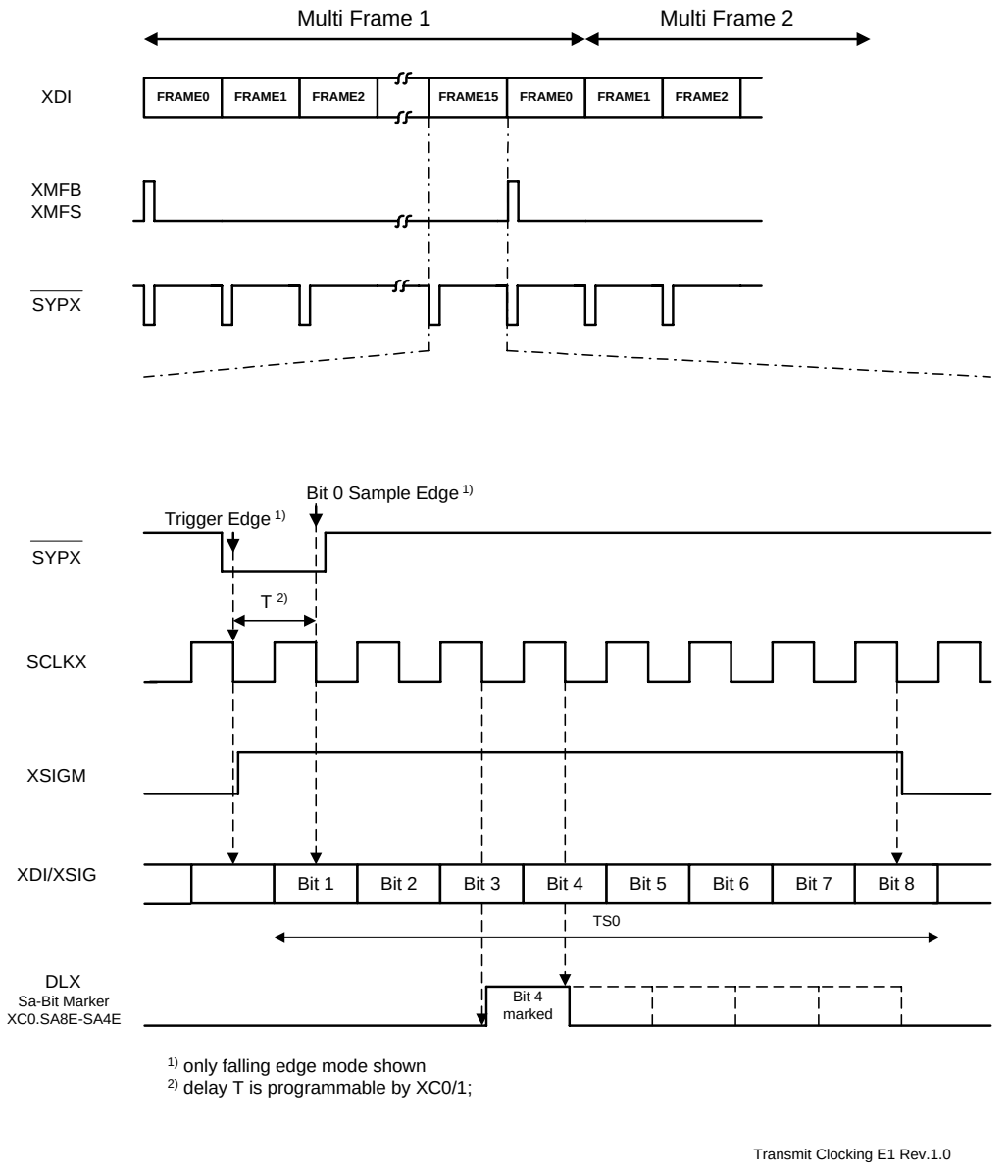


Figure 20
Transmit System Interface Clocking: 2.048 MHz

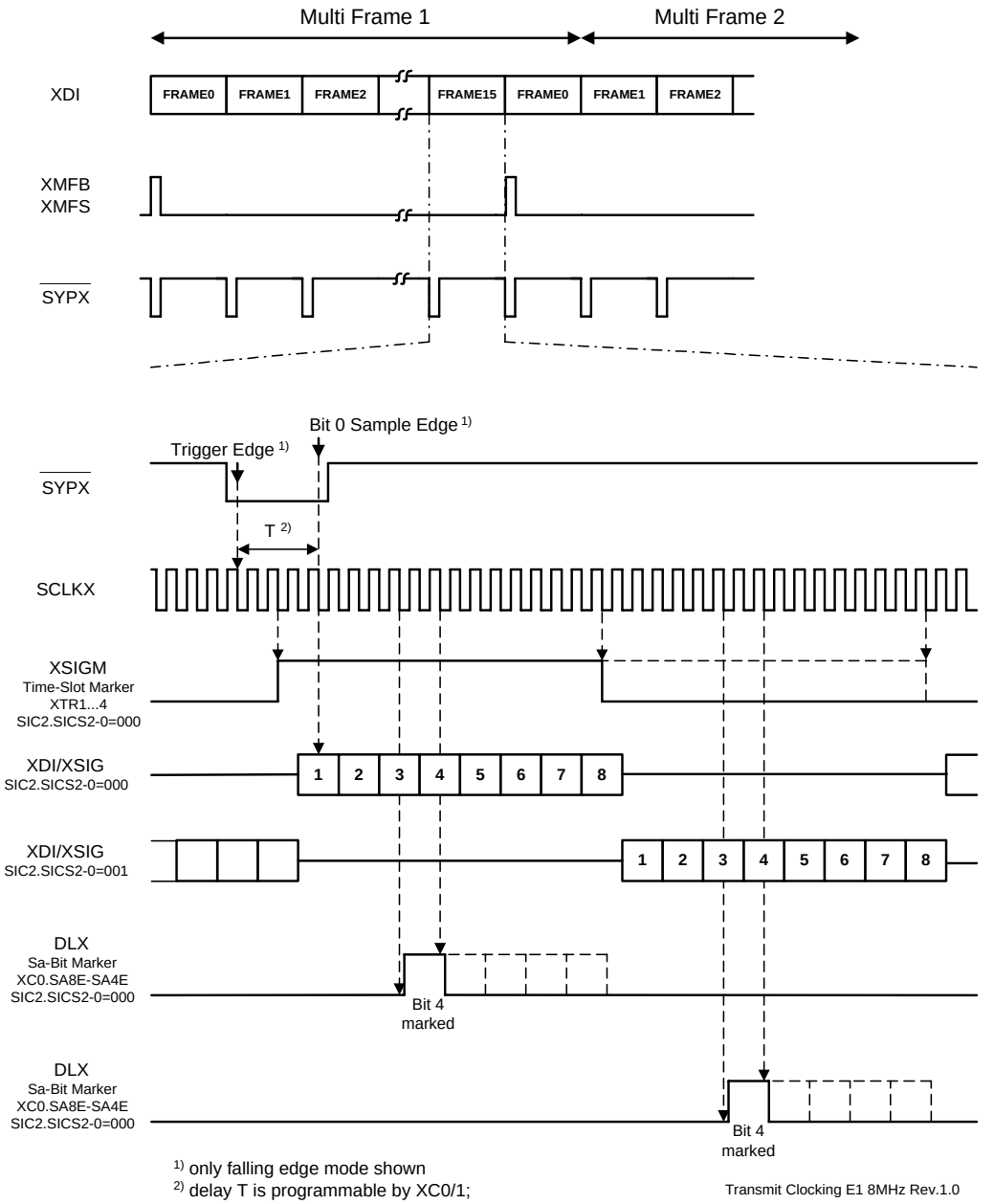


Figure 21
Transmit System Interface Clocking: 8.192 MHz and 4.096 MBit/s

Transmit Signaling Controller

Similar to the receive signaling controller the same signaling methods and the same time-slot assignment is provided. The QuadFALC will perform the following signaling and data link methods:

- **HDLC or LAPD access**
  The transmit signaling controller of the QuadFALC performs the FLAG generation, CRC generation, zero bit-stuffing and programmable IDLE code generation. Buffering of transmit data is done in the 64 byte deep XFIFO. The signaling information will be internally multiplexed with the data applied to port XDI or XSIG.
  In signaling controller transparent mode, fully transparent data transmission without HDLC framing is performed. Optionally the QuadFALC supports the continuous transmission of the XFIFO contents.
  The QuadFALC offers the flexibility to insert data during certain time-slots. Any combinations of time-slots may be programmed separately for the receive and transmit directions.
- **S_a bit Access**
  The QuadFALC supports the S_a bit signaling of time-slot 0 of every other frame as follows:
  - the access via registers XSW
  - the access via registers XSA8-4, capable of storing the information for a complete multiframe
  - the access via the 64 byte deep XFIFO of the signaling controller. This S_a bit access gives the opportunity to transparent a bit stream as well as HDLC frames where the signaling controller automatically processes the HDLC protocol. Any combination of S_a bits which should be inserted in the outgoing data stream may be selected by XC0.SA8-4.
- **Channel Associated Signaling CAS**
  Transmit data stored in registers XS1-16 will transmitted on a multiframe boundary in time-slot 16. The signaling controller inserts the bit stream either on the transmit line side or if external signaling is enabled on the transmit system side via pinfunction XSIG, which is selected by register PC1-4.
  In external signaling mode the signaling data is received at port XSIG. The signaling data is sampled with the working clock of the transmit system interface (SCLKX) in conjunction with the transmit synchron. pulse ($\overline{\text{SYPX}}$). Data on XSIG will be latched in the bit positions 5-8 per time-slot, bits 1-4 will be ignored. Time-slot 0 and 16 are sampled completly (bit 1-8). The received CAS multiframe will be inserted frame aligned into the data stream on XDI. Data sourced by the internal signaling controller will overwrite the external signaling data.

If the QuadFALC is optioned for no signaling, the data stream from the system interface will pass the QuadFALC undisturbed.

Transmit Elastic Buffer

The received bit stream from pin XDI is optionally stored in the transmit elastic buffer. The memory is organized as the receive elastic buffer. The functions are also equal to the receive side. Programming of the transmit buffer size is done by SIC1.XBS1/0 :

- XBS1/0 = 00 : Bypass of the transmit elastic buffer
- XBS1/0 = 01 : one frame buffer or 256 bits
  Max. wander amplitude (peak-to-peak): 94 UI (1 UI = 488 ns)
  average delay after performing a slip: 128 bits
- XBS1/0 = 10 : two frame buffer or 512 bits
  Maximum of wander amplitude: 190 UI
  average delay after performing a slip: 1 frame or 256 bits
- XBS1/0 = 11 : short buffer or 92 bits :
  Max. wander amplitude: 18 usec
  average delay after performing a slip: 46 bits

The functions of the transmit buffer are:

- Clock adaption between system clock (SCLKX) and internally generated transmit route clock (XCLK).
- Compensation of input wander and jitter.
- Frame alignment between system frame and transmit route frame
- Reporting and controlling of slips

Writing of received data from XDI is controlled by SCLKX/R and $\overline{\text{SYPX}}$ / XMFS in conjunction with the programmed offset values for the transmit time-slot/clock-slot counters. Reading of stored data is controlled by the clock generated by DCO-X circuitry or the externally generated TCLK and the transmit framer. With the dejittered clock data is read from the transmit elastic buffer and are forwarded to the transmitter. Reporting and controlling of slips is done according to the receive direction. Positive / negative slips are reported in interrupt status bits ISR4.XSP and ISR4.XSN. If the transmit buffer is bypassed data is directly transfered to the transmitter.

The following table gives an overview of the transmit buffer operating modes.

Buffer Size	TS Offset program.	Slip perform.
bypass	enabled	no
short buffer	enabled	yes
1 frame	enabled	yes
2 frames	enabled	yes

Transmitter

The serial bit stream is then processed by the transmitter which has the following functions:

- Frame/multiframe synthesis of one of the two selectable framing formats
- Insertion of service and data link information
- AIS generation (Alarm indication signal)
- Remote alarm generation
- CRC generation and insertion of CRC bits
  CRC bits inversion in case of a previously received CRC error
- IDLE code generation per DS0

The frame / multiframe boundries of the transmitter may be externally synchronized by using the $\overline{\text{SYPX}}$ / XMFS pin. Any change of the transmit time-slot assignment will subsequently produce a change of the framing bit positions on the line side. This feature is required if signaling- and service- bits are routed through the switching network and are inserted in transmit direction via the system interface.

In loop-timed configuration (LIM2.ELT) disconnecting the control of the transmit system highway from the transmitter is done by setting XSW.XTM. The transmitter is now in a free running mode without any possibility to actualize the multiframe position in case of changing the transmit time-slot assignment. The framing bits are generated independent of the transmit system interface. For proper operation the transmit elastic buffer size should be programmed to 2 frames.

The contents of selectable time-slots can be overwritten by the pattern defined via register IDLE. The selection of “idle channels” is done by programming the four-byte registers ICB1 … ICB4.

Transmit Line Interface

The analog transmitter transforms the unipolar bit stream to ternary (alternate bipolar) return to zero signals of the appropriate programmable shape. The unipolar data is provided by the digital transmitter.

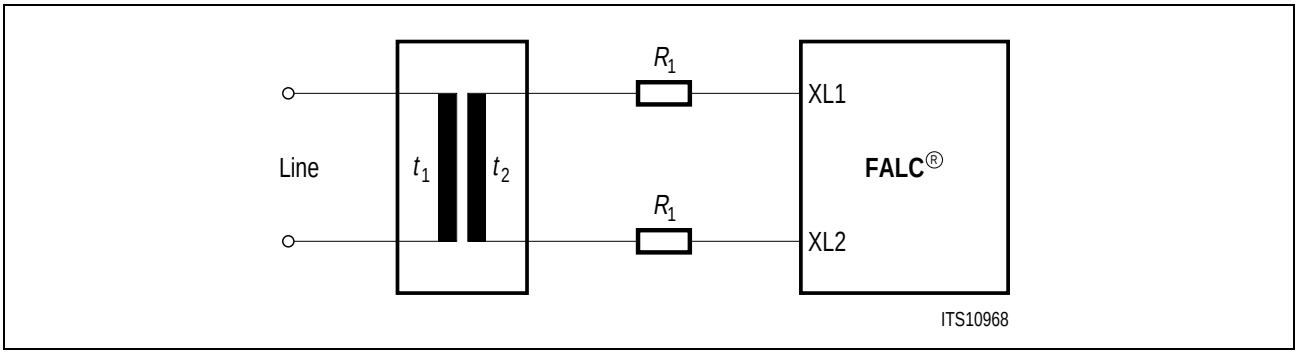


Figure 22
Transmitter Configuration

Recommended Transmitter Configuration Values

Parameter	Characteristic Impedance [Ω]	
	120	**75**
R_1 (± 1 %) [Ω]	7.5	7.5
t2 : t1	1 : 2.4	1 : 2.4

Similar to the receive line interface three different data types are supported:

- Ternary Signal
  Single rail data is converted into a ternary signal which is output on pins XL1 and XL2. The HDB3 and AMI line code is employed. Selected by FMR0.XC1/0 and LIM1.DRS = 0.
- Dual rail data PCM(+), PCM(–) at multifunction ports XDOP/ XDON with 50 % or 100 % duty cycle and with programmable polarity. Line coding is done in the same way as in the ternary interface. Selected by FMR0.XC1/0 and LIM1.DRS = 1.
- Unipolar data on port XOID will be transmitted either in NRZ (Non Return to Zero) with 100 % duty cycle or in CMI (Code Mark Inversion or known as 1T2B) Code with or without (FMR3.CMI) preprocessed HDB3 coding to a fibre optical interface. Clocking off data is done with the rising edge of the transmit clock XCLK (2048 kHz) and with a programmable polarity. Selection is done by FMR0.XC1 = 0 and LIM1.DRS = 1.

Programmable Pulse Shaper

The analog transmitter includes a programmable pulse shaper to satisfy the requirements of ITU-T I.431. The amplitude and shape of the transmit pulses are completely programmable via registers XPM0-2 from the microprocessor interface.

The transmitter requires an external step up transformer to drive the line.

Transmit Line Monitor

The transmit line monitor compares the transmit line current on XL1 and XL2 with an on-chip transmit line current limiter. The monitor detects faults on the primary side of the transformer indicated by a highly increased transmit line current (more than 120 mA for at least 3 pulses) and protects the device from damage by setting the transmit line driver XL1/2 automatically in a high impedance state. Two conditions will be detected by the monitor: transmit line ones density (more than 31 consecutive zeros) indicated by FRS1.XLO and transmit line high currrent indicated by FRS1.XLS. In both cases a transmit line monitor status change interrupt will be provided.

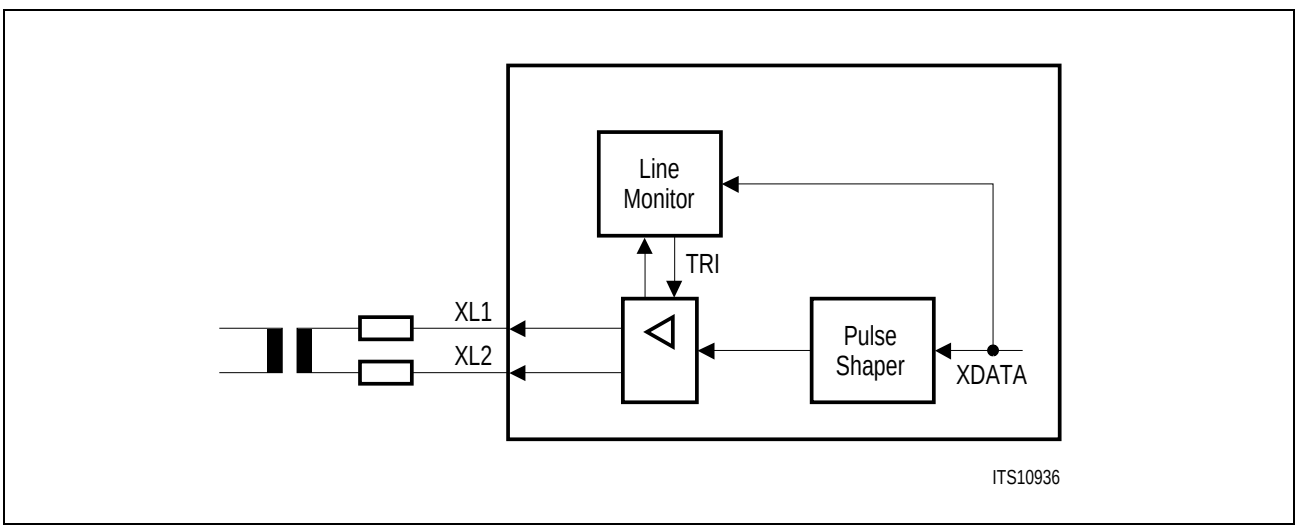


Figure 23
Transmit Line Monitor Configuration

3.7 Framer Operating Modes E1

General

Bit: FMR1.PMOD = 0

PCM line bit rate	:	2.048 MBit/s
Single frame length	:	256 bit, No. 1 … 256
Framing frequency	:	8 kHz
HDLC controller	:	nx64 kbit/s , n = 1 ... 32 or nx4 kbit/s , n=1 ... 5
Organization	:	32 time-slots, No. 0 … 31 with 8 bits each, No. 1 … 8

The operating mode of the QuadFALC is selected by programming the carrier data rate and characteristics, line code, multiframe structure, and signaling scheme.

The QuadFALC implements all of the standard framing structures for E1 or PCM 30 (CEPT, 2.048 MBit/s) carriers. The internal HDLC- or CAS Controller supports all signaling procedures including signaling frame synchronization / synthesis and signaling alarm detection in all framing formats. The time-slot assignment from the PCM line to the system highway and vv. is performed without any changes of numbering (TS0 ↔ TS0, … , TS31 ↔ TS31).

Summary of E1- Framing Modes

- Doubleframe format according to ITU-T G. 704
- Multiframe format according to ITU-T G. 704
  CRC4 processing according to ITU-T G. 706
- Multiframe format with CRC4 to non CRC4 interworking according to ITU-T G. 706
- Multiframe format with modified CRC4 to non CRC4 interworking
- Multiframe format with CRC4 performance monitoring

After RESET, the QuadFALC is switched into doubleframe format automatically. Switching between the framing formats is done via bit FMR2.RFS1/0 and FMR3.EXTIW for the receiver and FMR1.XFS for the transmitter.

3.7.1 Doubleframe Format

The framing structure is defined by the contents of time-slot 0 (refer to **table 6**).

Table 6
Allocation of Bits 1 to 8 of Time-Slot 0

Alternate Frames / Bit Number	1	2	3	4	5	6	7	8
Frame Containing the Frame Alignment Signal	S_i	0	0	1	1	0	1	1
	Note 1	Frame Alignment Signal						
Frame not Containing the Frame Alignment Signal or Service Word	S_i	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	Note 1	Note 2	Note 3	Note 4				

Note:

1. *S_i bits: reserved for international use. If not used, these bits should be fixed to '1'. Access to received information via bits RSW.RSI and RSP.RSIF. Transmission is enabled via bits XSW.XSIS and XSP.XSIF.*
2. *Fixed to '1'. Used for synchronization.*
3. *Remote alarm indication: In undisturbed operation '0'; in alarm condition '1'.*
4. *S_a bits: Reserved for national use. If not used, they should be fixed at '1'. Access to received information via bits RSW.RY0 … RY4. Transmission is enabled via bits XSW.XY0 … XY4. HDLC-signaling in bits Sa4- Sa8 is selectable. (*)*

Note: (*) As a special extension for double frame format, the S_a -bit registers RSA4-8 / XSA4-8 may be used optionally.

Transmit Transparent Modes

In transmit direction, contents of time-slot 0 frame alignment signal of the outgoing PCM frame are normally generated by the QuadFALC. However, transparency for the complete time-slot 0 can be achieved by selecting the transparent mode XSP.TT0. With the Transparent Service Word Mask register TSWM the Si-bits, A-bit and the SA4-8 bits can be selectively switched through transparently.

	Transmit Transparent Source for			
Enabled by	**Framing**	**A Bit**	**S_a Bits**	**S_i Bits**
–	(int. generated)	XSW.XRA[2)]	XSW.XY0 … 4[3)]	XSW.XSIS, XSP.XSIF
XSP.TT0	via pin XDI[1)]	via pin XDI	via pin XDI	via pin XDI
TSWM.TSIF	(int. generated)	XSW.XRA	XSW.XY0 … 4	via pin XDI
TSWM.TSIS	(int. generated)	XSW.XRA	XSW.XY0 … 4	via pin XDI
TSWM.TRA	(int. generated)	via pin XDI	XSW.XY0 … 4	XSW.XSIS, XSP.XSIF
TSWM.TSA4-8	(int. generated)	XSW.XRA	via pin XDI	XSW.XSIS, XSP.XSIF

1) pin XDI or XSIG or XFIFO-Buffer (signaling controller)

2) Additionally, automatic transmission of the A-bit is selectable

3) As a special extension for double frame format, the Sa-bit register may be used optionally.

Synchronization Procedure

Synchronization status is reported via bit FRS0.LFA. Framing errors are counted by the Framing Error Counter (FEC). Asynchronous state is reached after detecting 3 or 4 consecutive incorrect FAS words or 3 or 4 consecutive incorrect service words (bit 2 = 0 in time-slot 0 of every other frame not containing the frame alignment word), the selection is done via bit RC1.ASY4. Additionally, the service word condition can be disabled. When the framer lost its synchronization an interrupt status bit ISR2.LFA is generated.

In asynchronous state, counting of framing errors and detection of remote alarm will be stopped. AIS is automatically sent to the backplane interface (can be disabled via bit FMR2.DAIS).

Further on the updating of the registers RSW, RSP, RSA4-8, RSA6S and RS1-16 will be halted (remote alarm indication, Sa/Si-Bit access).

The resynchronization procedure starts automatically after reaching the asynchronous state. Additionally, it may be invoked user controlled via bit: FMR0.FRS (Force Resynchronization: the FAS word detection is interrupted until the framer is in the asynchronous state. After that, resynchronization starts automatically).

Synchronous state is established after detecting:

– a correct FAS word in frame n,
– the presence of the correct service word (bit 2 = 1) in frame n + 1,

– a correct FAS word in frame n + 2.

If the service word in frame n + 1 or the FAS word in frame n + 2 or both are not found searching for the next FAS word will be start in frame n + 2 just after the previous frame alignment signal.

Reaching the synchronous state causes a frame alignment recovery interrupt status ISR2.FAR if enabled. Undisturbed operation starts with the beginning of the next doubleframe.

A-Bit Access

If the QuadFALC detects a remote alarm indication in the received data stream the interrupt status bit ISR2.RA will be set. With setting of bit XSW.XRA a remote alarm (RAI) will be send to the far end.

By setting FMR2.AXRA the QuadFALC automatically transmit the remote alarm bit = 1 in the outgoing data stream if the receiver detects a loss of frame alignment FRS0.LFA = 1. If the receiver is in synchronous state FRS0.LFA = 0 the remote alarm bit will be reset.

Note: The A-bit may be processed via the system interface. Setting bit TSWM.TRA enables transparency for the A bit in transmit direction (refer to **table 7**).

S_a - Bit Access

As an extension for access to the S_a-bits via registers RSA4-8/XSA4-8 an option is implemented to allow the usage of internal S_a-bit registers RSA4-8/XSA4-8 in doubleframe format.

This function is enabled by setting FMR1.ENSA = 1 for the transmitter and FMR1.RFS1/0 = 01 for the receiver. The QuadFALC works then internally with a 16-frame structure but no CRC multiframe alignment/generation is performed.

3.7.2 CRC-Multiframe

The multiframe structure shown in **table 7** is enabled by setting bit: FMR1.RFS1/0 for the receiver and FMR1.XFS for the transmitter.

Multiframe	:	2 submultiframes = 2 × 8 frames
Frame alignment	:	refer to section Doubleframe Format
Multiframe alignment	:	bit 1 of frames 1, 3, 5, 7, 9, 11 with the pattern ‘001011’
CRC bits	:	bit 1 of frames 0, 2, 4, 6, 8, 10, 12, 14
CRC block size	:	2048 bit (length of a submultiframe)
CRC procedure	:	CRC4, according to ITU-T Rec. G.704, G.706

Table 7
CRC-Multiframe Structure

	Sub-Multiframe	Frame Number	Bits 1 to 8 of the Frame							
			1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Multiframe	I	0	C_1	0	0	1	1	0	1	1
		1	0	1	A	S_{a4}	S_{a5}	S_{a61}	S_{a7}	S_{a8}
		2	C_2	0	0	1	1	0	1	1
		3	0	1	A	S_{a4}	S_{a5}	S_{a62}	S_{a7}	S_{a8}
		4	C_3	0	0	1	1	0	1	1
		5	1	1	A	S_{a4}	S_{a5}	S_{a63}	S_{a7}	S_{a8}
		6	C_4	0	0	1	1	0	1	1
		7	0	1	A	S_{a4}	S_{a5}	S_{a64}	S_{a7}	S_{a8}
	II	8	C_1	0	0	1	1	0	1	1
		9	1	1	A	S_{a4}	S_{a5}	S_{a61}	S_{a7}	S_{a8}
		10	C_2	0	0	1	1	0	1	1
		11	1	1	A	S_{a4}	S_{a5}	S_{a62}	S_{a7}	S_{a8}
		12	C_3	0	0	1	1	0	1	1
		13	E*	1	A	S_{a4}	S_{a5}	S_{a63}	S_{a7}	S_{a8}
		14	C_4	0	0	1	1	0	1	1
		15	E*	1	A	S_{a4}	S_{a5}	S_{a64}	S_{a7}	S_{a8}

E: Spare bits for international use. Access to received information via bits RSP.RS13 and RSP.RS15. Transmission is enabled via bits XSP.XS13 and XSP.XS15. Additionally, automatic transmission for submultiframe error indication is selectable.

S_a: Spare bits for national use. Additionally, Sa bit access via registers RSA4 … 8 and XSA4 … 8 is provided. HDLC-signaling in bits Sa4- Sa8 is selectable.

C_1 … C_4: Cyclic redundancy check bits.

A: Remote alarm indication. Additionally, automatic transmission of the A-bit is selectable.

For transmit direction, contents of time-slot 0 are additionally determined by the selected transparent mode:

	Transmit Transparent Source for			
enabled by	**Framing + CRC**	**A Bit**	**Sa Bits**	**E Bits**
–	(int. generated)	XSW.XRA[2)]	XSW.XY0 … 4[3)]	XSP.XS13/XS15[4)]
XSP.TT0	via pin XDI[1)]	via pin XDI	via pin XDI	via pin XDI
TSWM.TSIF	(int. generated)	XSW.XRA[1)]	XSW.XY0 … 4[2)]	(int. generated)
TSWM.TSIS	(int. generated)	XSW.XRA[1)]	XSW.XY0 … 4[2)]	via pin XDI
TSWM.TRA	(int. generated)	via pin XDI	XSW.XY0 … 4[2)]	XSP.XS13/XS15[3)]
TSWM.TSA4–8	(int. generated)	XSW.XRA[1)]	via pin XDI	XSP.XS13/XS15[3)]

1) pin XDI or XSIG or XFIFO buffer (signaling controller)

2) Automatic transmission of the A-bit is selectable

3) The S_a-bit register XSA4-8 may be used optionally

4) Additionally, automatic transmission of submultiframe error indication is selectable

The CRC procedure is automatically invoked when the multiframe structure is enabled. CRC errors in the received data stream are counted by the 16 bit CRC Error Counter CEC (one error per submultiframe, maximum).

Additionally a CRC4 error interrupt status ISR0.CRC4 may be generated if enabled by IMR0.CRC4.

All CRC bits of one outgoing submultiframe are automatically inverted in case a CRC error is flagged for the previous received submultiframe. This function is enabled via bit RC0.CRCI. Setting the bit RC0.XCRCI will invert the CRC bits before transmission to the distant end. The function of RC0.XCRCI and RC0.CRCI are logically ored.

Synchronization Procedure

Multiframe alignment is assumed to have been lost if doubleframe alignment has been lost (flagged at status bits FRS0.LFA and FRS0.LMFA). The rising edge of these bits will cause an interrupt status bits ISR2.LFA + ISR2.LMFA.

The multiframe resynchronization procedure starts when Doubleframe alignment has been regained which is indicated by an interrupt status bit ISR2.FAR. For Doubleframe synchronization refer to section Doubleframe Format. It may also be invoked by the user by setting

– bit FMR0.FRS for complete Doubleframe **and** multiframe re-synchronization
– bit FMR1.MFCS for multiframe re-synchronization only.

The CRC checking mechanism will be enabled after the first correct multiframe pattern has been found. However, CRC errors will not be counted in asynchronous state.

In doubleframe asynchronous state, counting of framing errors, CRC4 bit errors and detection of remote alarm will be stopped. AIS is automatically sent to the backplane interface (can be disabled via bit FMR2.DAIS). Further on the updating of the registers RSW, RSP, RSA4-8, RSA6S and RS1-16 will be halted (remote alarm indication, Sa/Si-bit access).

The multiframe synchronous state is established after detecting two correct multiframe alignment signals at an interval of $n \times 2$ ms (n = 1, 2, 3 …). The Loss of multiframe alignment flag FRS0.LMFA will be reset. Additionally an interrupt status multiframe alignment recovery bit ISR2.MFAR is generated with the falling edge of bit FRS0.LMFA.

Automatic Force Resynchronization

In addition, a search for Doubleframe alignment is automatically initiated if two multiframe pattern with a distance of $n \times 2$ ms have not been found within a time interval of 8 ms after doubleframe alignment has been regained (bit FMR1.AFR). A new search for frame alignment will be started just after the previous frame alignment signal.

Floating Multiframe Alignment Window

After reaching doubleframe synchronization a 8 ms timer is started. If a multiframe alignment signal is found during the 8 ms time interval the internal timer will be reset to remaining 6 ms in order to find the next multiframe signal within this time. If the multiframe signal is not found for a second time an interrupt status ISR0. T8MS will be provided. This interrupt will usually occur every 8 ms until multiframe synchronization is achieved.

CRC4 Performance Monitoring

In the synchronous state checking of multiframe pattern is disabled. However, with bit FMR2.ALMF an automatic multiframe resynchronization mode can be activated. If 915 out of 1000 errored CRC submultiframes are found then a false frame alignment will be assumed and a search for double- and multiframe pattern is initiated. The new search for frame alignment will be started just after the previous basic frame alignment signal. The internal CRC4 resynchronization counter will be reset when the multiframe synchronization has been regained.

Modified CRC4 Multiframe Alignment Algorithm

The modified CRC4 multiframe alignment algorithm allows an automatic interworking between framers with and without a CRC4 capability. The interworking is realized as it is described in ITU-T G.706 Appendix B.

If doubleframe synchronization is consistently present but CRC4 multiframe alignment is not achieved within 400 ms it is assumed that the distant end is initialized to doubleframe format. The CRC4 - Non CRC4 interworking is enabled via FMR2.RFS1/0 = 11 and is activated only if the receiver has lost its synchronization. If doubleframe alignment (basic frame alignment) is established a 400 ms timer and searching for multiframe alignment will be started. A research for basic frame alignment will be initiated if the CRC4 multiframe synchronization could not be achieved within 8 ms and will be started just after the previous frame alignment signal. The research of the basic frame alignment is done in parallel and is independent of the synchronization procedure of the primary basic frame alignment signal. During the parallel search all receiver functions are based on the primary frame alignment signal, like framing errors, Sa-, Si-, A-bits …). All subsequent multiframe searches are associated with each basic framing sequence found during the parallel search.

If the CRC4 multiframe alignment sequence was not found within the time interval of 400 ms, the receiver will be switched into a Non CRC4 mode indicated by setting the bit FRS0.NMF (No Multiframing Found) and ISR2.T400MS. In this mode checking of CRC bits is disabled and the received E-bits are forced to low. The transmitter framing format will not be changed. Even if multiple basic FAS resynchronizations have been established during the parallel search, the receiver will be maintained to the initially determined primary frame alignment signal location.

However, if the CRC4 multiframe alignment could be achieved within the 400 ms time interval assuming a CRC4 to CRC4 interworking, then the basic frame alignment sequence associated to the CRC4 multiframe alignment signal will be chosen. If necessary, the primary frame alignment signal location will be adjusted according to the multiframe alignment signal. The CRC4 performance monitoring will be started if enabled by FMR2.ALMF and the received E-bits will be processed in accordance with ITU-T G.704.

Switching into the doubleframe format (non CRC4) mode after 400 msec can be disabled by setting of FMR3.EXTIW. In this mode the QuadFALC continues search for multiframing. In the interworking mode setting of bit FMR1.AFR is not allowed.

A-Bit Access

If the QuadFALC detects a remote alarm indication (bit 2 in TS0 not containing the FAS word) in the received data stream the interrupt status bit ISR2.RA will be set. With the deactivation of the remote alarm the interrupt status bit ISR2.RAR is generated.

By setting FMR2.AXRA the QuadFALC automatically transmits the remote alarm bit = 1 in the outgoing data stream if the receiver detects a loss of frame alignment (FRS0.LFA = 1). If the receiver is in synchronous state (FRS0.LFA = 0) the remote alarm bit will be reset in the outgoing data stream.

Additionally, if bit FMR3.EXTIW is set and the multiframesynchronous state could not be achieved within the 400 msec after finding the primary basic framing, the A-bit will be transmitted active high to the remote end until the multiframing is found.

*Note: The A-bit may be processed via the system interface. Setting bit TSWM.TRA enables transparency for the A bit in transmit direction (refer to **table 7**).*

S_a - Bit Access

Due to signaling procedures using the five S_a bits (S_{a4} … S_{a8}) of every other frame of the CRC multiframe structure, three possibilities of access via the microprocessor are implemented.

- The standard procedure allows reading/writing the S_a-bit registers RSW, XSW without further support. The S_a-bit information will be updated every other frame.
- The advanced procedure, enabled via bit FMR1.ENSA, allows reading/writing the S_a-bit registers RSA4 … 8, XSA4 … 8.

  A transmit or receive multiframe begin interrupt (ISR0.RMB or ISR1.XMB) is provided.

  Registers RSA4-8 contains the service word information of the previously received CRC-multiframe or 8 doubleframes (bitslots 4-8 of every service word). These registers will be updated with every multiframe begin interrupt ISR0.RMB.

  With the transmit multiframe begin an interrupt ISR1.XMB is generated and the contents of this registers XSA4-8 will be copied into shadow registers. The contents will subsequently sent out in the service words of the next outgoing CRC multiframe (or every doubleframes) if none of the time-slot 0 transparent modes is enabled. The transmit multiframe begin interrupt XMB request that these registers should be serviced. If requests for new information will be ignored, current contents will be repeated.
- The extended access via the receive and transmit FIFOs of the signaling controller. In this mode it is possible to transmit / receive a HDLC frame or a transparent bit stream in any combination of the S_a bits. Enabling is done by setting of bit CCR1.EITS and the corresponding bits XC0.SA8E-4E / TSWM.TSA8-4 and resetting of registers TTR1-4, RTR1-4 and FMR1.ENSA. The access to and from the FIFOs is supported by ISR0.RME,RPF and ISR1.XPR,ALS.

– SA6-Bit Detection according to ETS 300233

Four consecutive received SA6-bits are checked on the by ETS 300233 defined SA6-bit combinations. The QuadFALC will detect following fixed SA6-bit combinations: SA61,SA62,SA63,SA64 = 1000; 1010; 1100; 1110; 1111. All other possible 4 bit combinations are grouped to status “X”.

A valid SA6-bit combination must occur three times in a row. The corresponding status bit in register RSA6S will be set. Register RSA6S is from type “Clear on Read”. With any

change of state of the SA6-bit combinations an interrupt status ISR0.SA6SC will be generated.

During the basicframe asynchronous state updating of register RSA6S and interrupt status ISR0.SA6SC is disabled. In multiframe format the detection of the SA6-bit combinations can be done either synchronous or asynchronous to the submultiframe (FMR3.SA6SY). In synchronous detection mode updating of register RSA6S is done in the multiframe synch. state (FRS0.LMFA=0). In asynchr. detection mode updating is independent to the multiframe synchronous state.

– Sa6 Bit Error Indication Counters

The Sa6 bit error indication counter CRC2L/H (16 bits) counts the received Sa6 bit sequence 0001 or 0011 in every CRC submultiframe.In the primary rate access digital section this counter option gives information about CRC errors reported from the TE via Sa6 bit. Incrementing is only possible in the multiframe synchronous state.

The Sa6 bit error indication counter CRC3L/H (16 bits) counts the received Sa6 bit sequence 0010 or 0011 in every CRC submultiframe. In the primary rate access digital section this counter option gives information about CRC errors detected at T-reference point and reporting them via the Sa6 bit. Incrementing is only possible in the multiframe synchronous state.

E-Bit Access

Due to signaling requirements, the E bits of frame 13 and frame 15 of the CRC multiframe can be used to indicate received errored submultiframes:

Submultiframe I status E- Bit located in frame 13
Submultiframe II status E- Bit located in frame 15

no CRC error: : E = 1

CRC error: : E = 0

– Standard Procedure

After reading the Submultiframe Error Indication RSP.SI1 and RSP.SI2, the microprocessor has to update contents of register XSP (XS13, XS15). Access to these registers has to be synchronized to Transmit or Receive Multiframe Begin Interrupts (ISR0.RMB or ISR1.XMB).

– Automatic Mode

By setting bit XSP.AXS status information of received submultiframes is automatically inserted in E-bit position of the outgoing CRC Multiframe without any further interventions of the microprocessor.

In the double- and multiframe asynchronous state the E-bits are set to zero. However they can be set to one in the async. state if enabled by bit XSP.EBP. In the multiframe sync. state the E-bits are processed according to ITU-T G.704 independent of bit XSP.EBP

– Submultiframe Error Indication Counter

The EBC (E-Bit) Counter EBCL and EBCH (16 bits) counts zeros in E-bit position of frame 13 and 15 of every received CRC Multiframe. This counter option gives information about the outgoing transmit PCM line if the E bits are used by the remote end for submultiframe error indication. Incrementing is only possible in the multiframe synchronous state.

*Note: E-bits may be processed via the system interface. Setting bit TSWM.TSIS enables transparency for E bits in transmit direction (refer to **table 7**).*

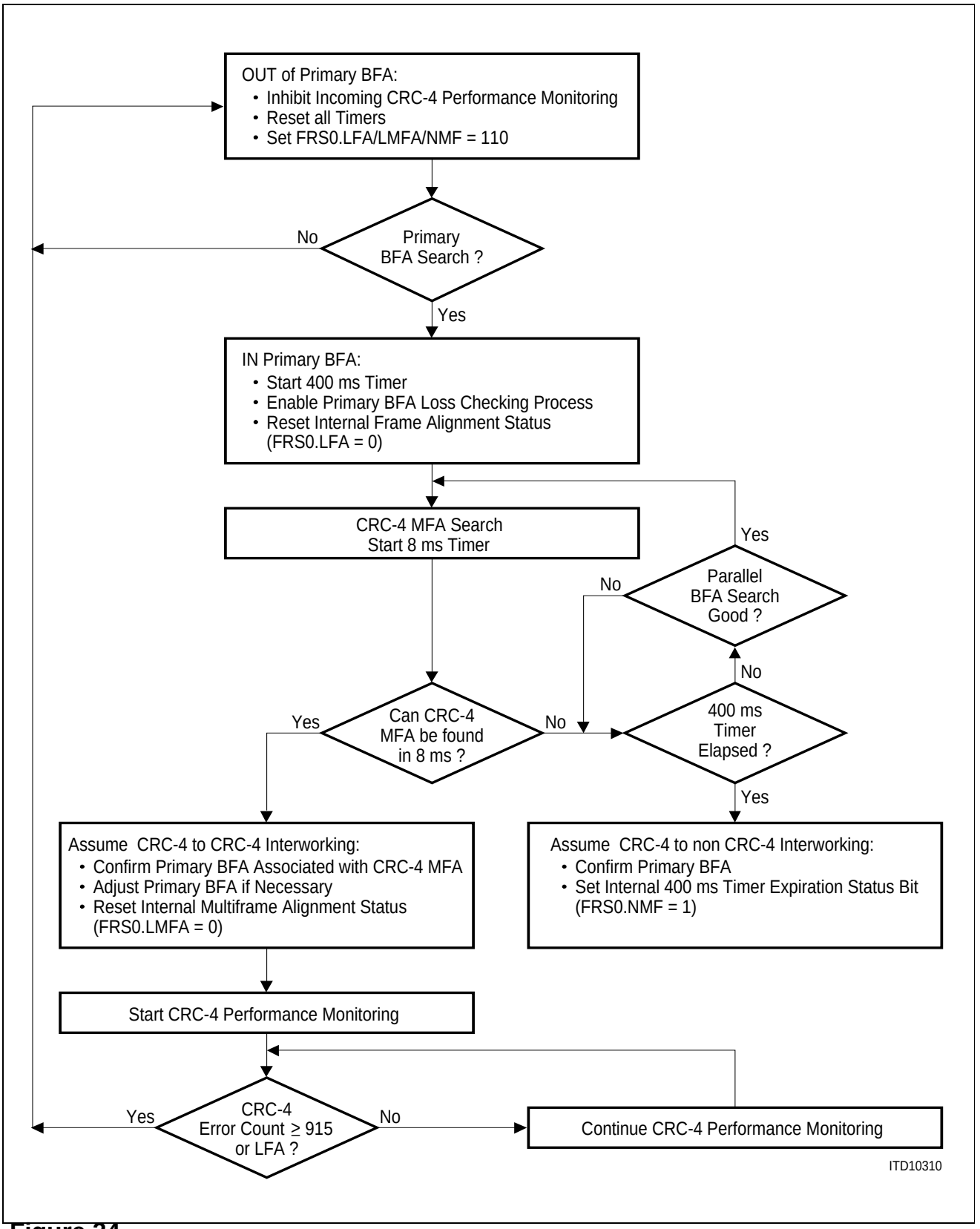


Figure 24
CRC4 Multiframe Alignment Recovery Algorithms (BFA = Basic Frame Alignment)

3.7.3 Additional Functions

Error performance monitoring and alarm handling

- alarm detection and generation

Alarm Indication Signal: Detection and recovery is flagged by bit FRS0.AIS and ISR2.AIS. Transmission is enabled via bit FMR1.XAIS.

Loss of Signal: Detection and recovery is flagged by bit FRS0.LOS and ISR2.LOS.

Remote Alarm Indication: Detection and release is flagged by bit FRS0.RRA, RSW.RRA and ISR2.RA/RAR. Transmission is enabled via bit XSW.XRA.

AIS in Time-Slot 16: Detection and release is flagged by bit FRS1.TS16AIS and ISR3.AIS16. Transmission is enabled by writing all ones in registers XS1-16.

LOS in Time-Slot 16: Detection and release is flagged by bit FRS1.TS16LOS. Transmission is enabled by writing all zeros in registers XS1-16.

Remote Alarm in Time-Slot 16: Detection and release is flagged by bit FRS1.TS16RA and ISR3.RA16. Transmission is enabled via bit CCR1.XTS16RA or XS1.2 .

Transmit Line Shorted: Detection and release is flagged by bit FRS1.XLS and ISR1.XLSC.

Transmit Ones Density: Detection and release is flagged by bit FRS1.XLO and ISR1.XLSC.

Table 8
Summary of Alarm Detection and Release

Alarm	Detection Condition	Clear Condition
Loss of Signal (LOS)	no transitions (logical zeros) in a programmable time interval of 16 - 4096 consecutive pulse periods. Programmable receive input signal threshold	programmble number of ones (1-256) in a programmable time interval of 16 - 4096 consecutive pulse periods. A one is a signal with a level above the programmed threshold.
Alarm Indication Signal (AIS)	FMR0.ALM = 0: less than 3 zeros in 250 µsec and loss of frame alignment declared FMR0.ALM = 1: less than 3 zeros in each of two consecutive 250 µsec periods	FMR0.ALM = 0: more than 2 zeros in 250 µsec FMR0.ALM = 1: more than 2 zeros in each of two 500 µsec periods
Remote Alarm (RRA)	bit 3 = 1 in time-slot 0 not containing the FAS word	set conditions no longer detected.
Remote Alarm in Time-Slot 16 (TS16RA)	Y-bit = 1 received in CAS multiframe alignment word	Y-bit = 0 received in CAS multiframe alignment word
Loss of Signal in Time-Slot 16 (TS16LOS)	all zeros for at least 16 consecutively received time-slots 16	receiving a one in time-slot 16
Alarm Indication Signal in Time-Slot 16 (TS16AIS)	time-slot 16 containing less than 4 zeros in each of two consecutive CAS multiframes periods	time-slot 16 containing more than 3 zeros in each of two consecutive CAS multiframes periods
Transmit Line Short (XLS)	more than 32 pulse periods with highly increased transmit line current on XL1/2	no transmit line current limiter active
Transmit Ones Density (XLO)	32 consecutive zeros in the transmit data stream on XL1/2	Cleared with each transmitted pulse

- **Auto modes**
  - Automatic remote alarm access

  If the receiver has lost its synchronization a remote alarm could be sent automatically, if enabled by bit FMR2.AXRA to the distant end. The remote alarm bit will be automatically set in the outgoing data stream if the receiver is in asynchronous state (FRS0.LFA bit is set). In synchronous state the remote alarm bit will be removed.
  - Automatic E bit access

  By setting bit XSP.AXS status information of received submultiframes is automatically inserted in E-bit position of the outgoing CRC Multiframe without any further interventions of the microprocessor.
  - Automatic AIS to system interface

  In asynchronous state the synchronizer enforces automatically an AIS to the receive system interface. However, received data can be transparently switched through if bit FMR2.DAIS is set.
  - Automatic clock source switching

  In Slave mode (LIM0.MAS = 0) the DCO-R will synchronize to the recovered route clock. In case of Loss of Signal LOS the DCO-R switches automatically to Master mode. If bit CMR1.DCS is set automatic switching from RCLK to SYNC may be disabled.
  - Automatic freeze signaling:

  Updating of the received signaling information is controlled by the freeze signaling status. The freeze signaling status is automatically activated if a Loss of Signal, or a Loss of CAS Multiframe Alignment or a receive slip occures. The internal signaling buffer RS1-16 is frozen. Optionally automatic freeze signaling may be disabled by setting bit SIC3.DAF.
- **Error counter**

  The QuadFALC offers six error counters each of them has a length of 16 bit. They record code violations, framing bit errors, CRC4 bit errors and CRC4 error events which are flagged in the different SA6 bit combinations or the number of received multiframes in the asynchronous state or the change of frame alignment (COFA). Counting of the multiframes in the asyn. state and the COFA parameter is done in a 6 / 2 bit counter and is shared with CEC3L/H. Each of the error counter is buffered. Updating the buffer is done in two modes:
  - one second accumulation
  - on demand via handshake with writing to the DEC register

  In the one second mode an internal/external one second timer will update these buffers and reset the counter to accumulate the error events in the next one second period. The error counter can not overflow. Error events occuring during reset will not lost.
- **Status : errored second**

  The QuadFALC supports the error performance monitoring by detecting the following alarms or error events in the received data:
  framing errors , CRC errors , code violations , loss of frame alignment , loss of signal,

alarm indication signal , E bit error , receive and transmit slips.
With a programmable interrupt mask register ESM all these alarms or error events could generate an Errored Second interrupt (ISR3.ES) if enabled.

- **Second timer**
  Additionally per channel a one second timer interrupt could be internally generated to indicate that the enabled alarm status bits or the error counters have to be checked. If enabled via bit GPC1.FSS2-0 the one second timer of the selected channel can be output on port SEC/FSC (GPC1.CSFP1/0). Optionally if all four channels of the QuadFALC should synchronized to an external second timer an appropriate clock has to be provided to pin SEC/FSC. Selecting the external second timer is done with GCR.SES. Refer also to register GPC1.

In-Band Loop Generation and Detection

The QuadFALC generates and detects a framed or unframed in-band loop up/actuate - and down/deactuate pattern with bit error rates as high as 1/100. Framed or unframed in-band loop code is selected by LCR1.FLLB . Replacing transmit data with the in-band loop codes is done by FMR3.XLD / XLU.
The QuadFALC also offers the ability generating and detecting of a flexible in-band loop up - and down pattern (LCR1.LLBP = 1). The loop up and loop down pattern is individual programmable from 2 to 8 bit in length (LCR1.LAC1/0 and LCR1.LDC1/0). Programming of loop codes is done in registers LCR2 and LCR3.
Status and interrupt-status bits will inform the user whether loop up - or loop down code was detected.

Time-Slot 0 Transparent Mode

The transparent modes are useful for loopbacks or for routing data unchanged through the QuadFALC.

In receive direction, transparency for ternary or dual / single rail unipolar data is always achieved if the receiver is in the synchronous state. In asynchronous state the data may be transparently switched through if bit FMR2.DAIS is set. However, correct time-slot assignment can not be guaranteed due to missing frame alignment between line and system side.
Setting of bit FMR2.RTM disconnects control of the internal elastic store from the receiver. The elastic buffer is now in a “free running” mode without any possibility to actualize the time slot assignment to a new frame position in case of re-synchronization of the receiver. Together with FMR2.DAIS this function can be used to realize undisturbed transparent reception.

Transparency in transmit direction can be achieved by activating the time-slot 0 transparent mode (bit XSP.TT0 or TSWM.7-0). If XSP.TT0 = 1 all internal information of

the QuadFALC (framing, CRC, Sa/Si bit signaling, remote alarm) will be ignored. With register TSWM the Si-bits, A-bit or the Sa4-8 bits could be selectively enabled to send data transparent from port XDI to the far end. For complete transparency the internal signaling controller, IDLE code generation and AIS alarm generation, single channel and payload loop back has to be disabled.

Pseudo-Random Bit Sequence Generation and Monitor

The QuadFALC has the added ability to generate and monitor 2^{15}-1 and 2^{20}-1 pseudo-random bit sequences (PRBS). The generated PRBS pattern will be transmitted optionally inverted or not to the remote end via pins XL1/2 resp. XDOP/N. Generating and monitoring of PRBS pattern is done according to ITU-T O. 151.
The PRBS monitor senses the PRBS pattern in the incoming data stream. Synchronization is done on the inverted and non inverted PRBS pattern. The current synchronization status is reported in status and interrupt status registers. Enabled by bit LCR1.EPRM each PRBS bit error will increment an error counter (CEC2). Synchronization will be reached within 400 msec with a probability of 99.9% and a BER of 1/10.

Single Channel Loop Back

Each of the 32 time-slots may be selected for loopback from the system PCM input (XDI) to the system PCM output (RDO). This loopback is programmed for one time-slot at a time selected by register LOOP. During loopback, an idle channel code programmed in register IDLE is transmitted to the remote end in the corresponding PCM route time-slot.

For the time-slot test, sending sequences of test patterns like a 1 kHz check signal should be avoided. Otherwise, an increased occurrence of slips in the tested time-slot will disturb testing. These slips do not influence the other time-slots and the function of the receive memory. The usage of a quasi-static test pattern is recommended.

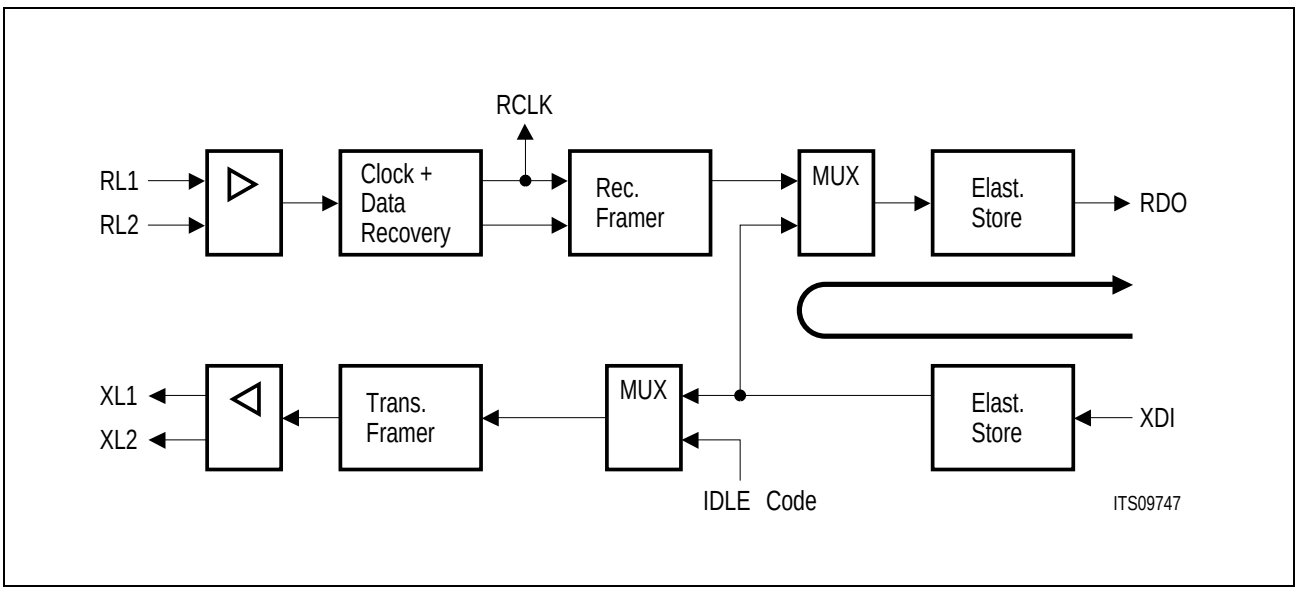


Figure 25
Single Channel Loopback

Payload Loop Back

To perform an effective circuit test a payload loop is implemented. The payload loop back (FMR2.PLB) will loop the data stream from the receiver section back to transmitter section. The looped data will pass the complete receiver including the wander and jitter compensation in the receive elastic store and were output on pin RDO. Instead of the data an AIS (FMR2.SAIS) could be sent to the system interface.

The framing bits, CRC4 and Spare bits are not looped, if XSP.TT0 =0. They are originated by the QuadFALC transmitter. If the PLB is enabled the transmitter and the data on pins XL1/2 or XDOP/XDON are clocked with SCLKR instead of SCLKX. If XSP.TT0 = 1 the received time-slot 0 is sent transparently back to the line interface. Data on the following pins are ignored: XDI, XSIG, TCLK, SCLKX, $\overline{\text{SYPX}}$ and XMFS. All the received data is processed normally.

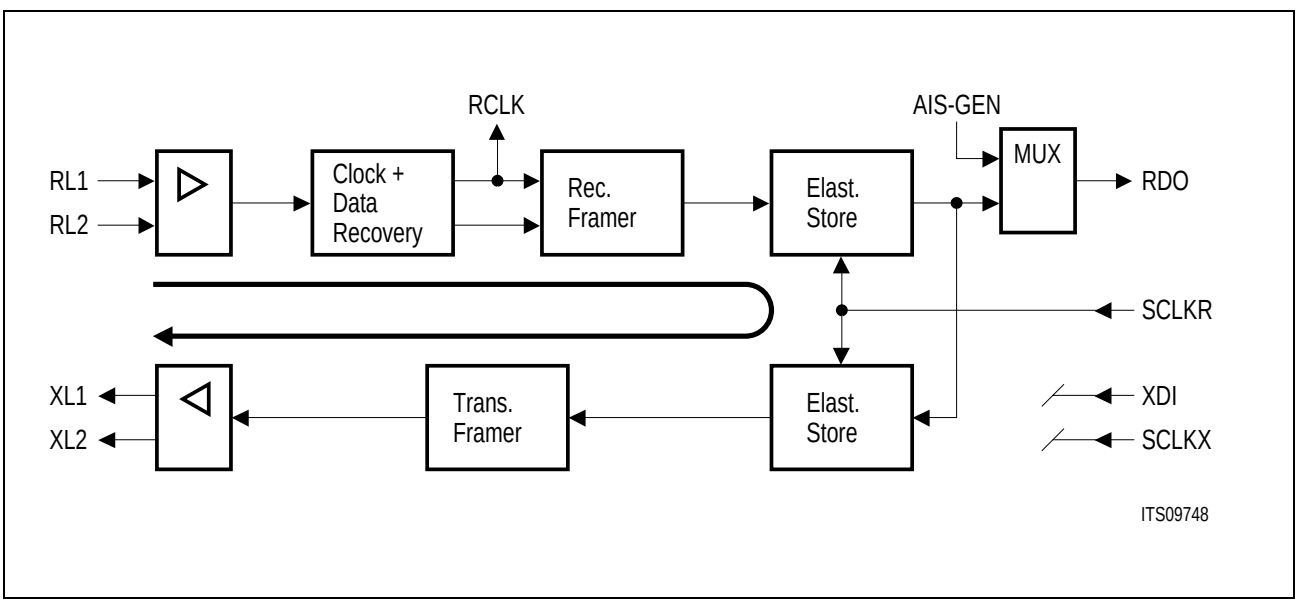


Figure 26
Payload Loop

Local Loop

The local loopback mode, selected by LIM0.LL = 1, disconnects the receive lines RL1/2 or RDIP/RDIN from the receiver. Instead of the signals coming from the line the data provided by system interface are routed through the analog receiver back to the system interface. However, the bit stream will be undisturbed transmitted on the line. However an AIS to the distant end could be enabled by setting FMR1.XAIS without influencing the data looped back to the system interface.

Note that enabling the local loop will usually invoke an out of frame error until the receiver can resync to the new framing. The serial code from the transmitter and receiver has to be programmed identically.

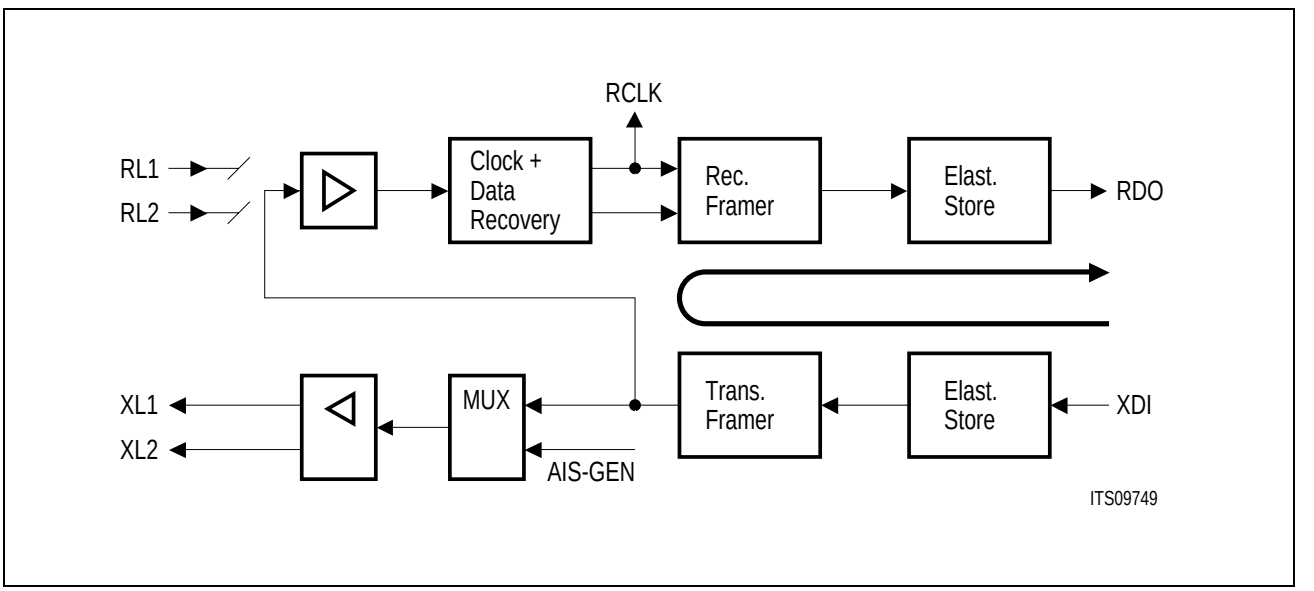


Figure 27
Local Loop

Remote Loop

In the remote loopback mode the clock and data recovered from the line inputs RL1/2 or RDIP/RDIN are routed back to the line outputs XL1/2 or XDOP/XDON via the analog or digital transmitter. As in normal mode they are also processed by the synchronizer and then sent to the system interface.The remote loopback mode is selected by setting the respective control bits LIM1.RL+JATT. Received data may be looped with or without the transmit jitter attenuator (FIFO).

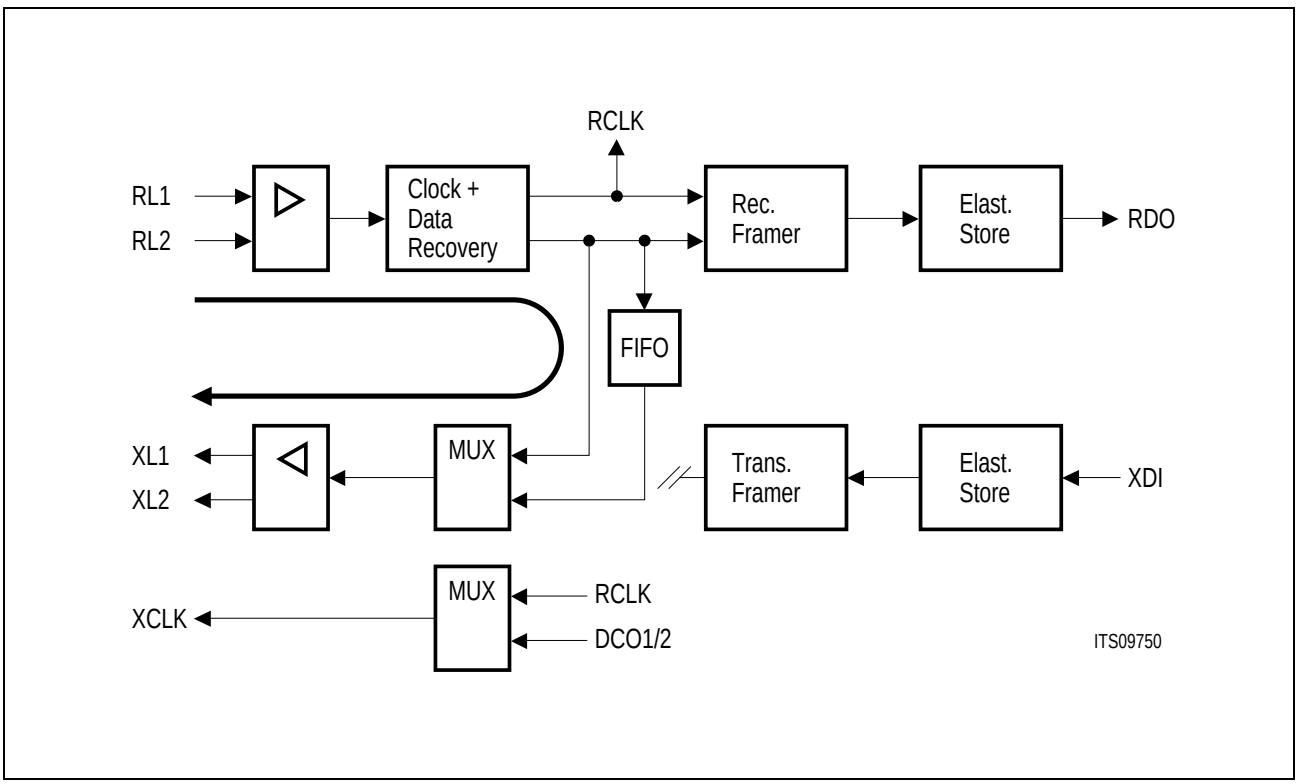


Figure 28
Remote Loop

Alarm Simulation

Alarm simulation does not affect the normal operation of the device, i.e. all time-slots remain available for transmission. However, possible ‘real’ alarm conditions are not reported to the processor or to the remote end when the device is in the alarm simulation mode.

The alarm simulation is initiated by setting the bit FMR0.SIM. The following alarms are simulated:

- Loss of Signal
- Alarm Indication Signal (AIS)
- Loss of pulse frame
- Remote alarm indication
- Receive and transmit slip indication
- Framing error counter
- Code violation counter (HDB3 Code)
- CRC4 error counter
- E-Bit error counter
- CEC2 counter
- CEC3 counter

Some of the above indications are only simulated if the QuadFALC is configured in a mode where the alarm is applicable (e.g. no CRC4 error simulation when doubleframe format is enabled).

– Setting of the bit FMR0.SIM initiates alarm simulation, interrupt status bits will be set. Error counting and indication will occurs while this bit is set. After it is reset all simulated error conditions disappear, but the generated interrupt statuses are still pending until the corresponding interrupt status register is read. Alarms like AIS and LOS are cleared automatically. Interrupt status register and error counters are automatically cleared on read.

4 Operational Description E1

4.1 Signaling Controller Operating Modes

The HDLC controller can be programmed to operate in various modes, which are different in the treatment of the HDLC frame in receive direction. Thus, the receive data flow and the address recognition features can be performed in a very flexible way, to satisfy almost any practical requirements.

There are 4 different operating modes which can be set via the MODE register.

4.1.1 HDLC Mode

All frames with valid addresses are forwarded directly via the RFIFO to the system memory.

Depending on the selected address mode, the QuadFALC can perform a 1 or 2 byte address recognition (MODE.MDS0).

If a 2-byte address field is selected, the high address byte is compared with the fixed value FEH or FCH (group address) as well as with two individually programmable values in RAH1 and RAH2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address will be interpreted as COMMAND/RESPONSE bit (C/R) and will be excluded from the address comparison.

Similarly, two compare values can be programmed in special registers (RAL1, RAL2) for the low address byte. A valid address will be recognized in case the high and low byte of the address field correspond to one of the compare values. Thus, the QuadFALC can be called (addressed) with 6 different address combinations. HDLC frames with address fields that do not match any of the address combinations, are ignored by the FALC.

In case of a 1-byte address, RAL1 and RAL2 will be used as compare registers. The HDLC control field, data in the I-field and an additional status byte are temporarily stored in the RFIFO. Additional information can also be read from a special register (RSIS).

As defined by the HDLC protocol, the QuadFALC perform the zero bit insertion/deletion (bit-stuffing) in the transmit/receive data stream automatically. That means, it is guaranteed that at least after 5 consecutive “1”-s a “0” will appear.

Non-Auto-Mode (MODE.MDS2-1=01)

Characteristics: address recognition, FLAG - and CRC generation/check, bit-stuffing

All frames with valid addresses are forwarded directly via the RFIFO to the system memory.

Transparent Mode 1 (MODE.MDS2-0=101)

Characteristics: address recognition, FLAG - and CRC generation/check, bit-stuffing

Only the high byte of a 2-byte address field will be compared with registers RAH1/2. The whole frame excluding the first address byte will be stored in RFIFO.

Transparent Mode 0 (MODE.MDS2-0=100)

Characteristics: FLAG - and CRC generation/check, bit-stuffing
No address recognition is performed and each frame will be stored in the RFIFO.

Receive Data Flow

The following figure gives an overview of the management of the received HDLC frames in the different operating modes.

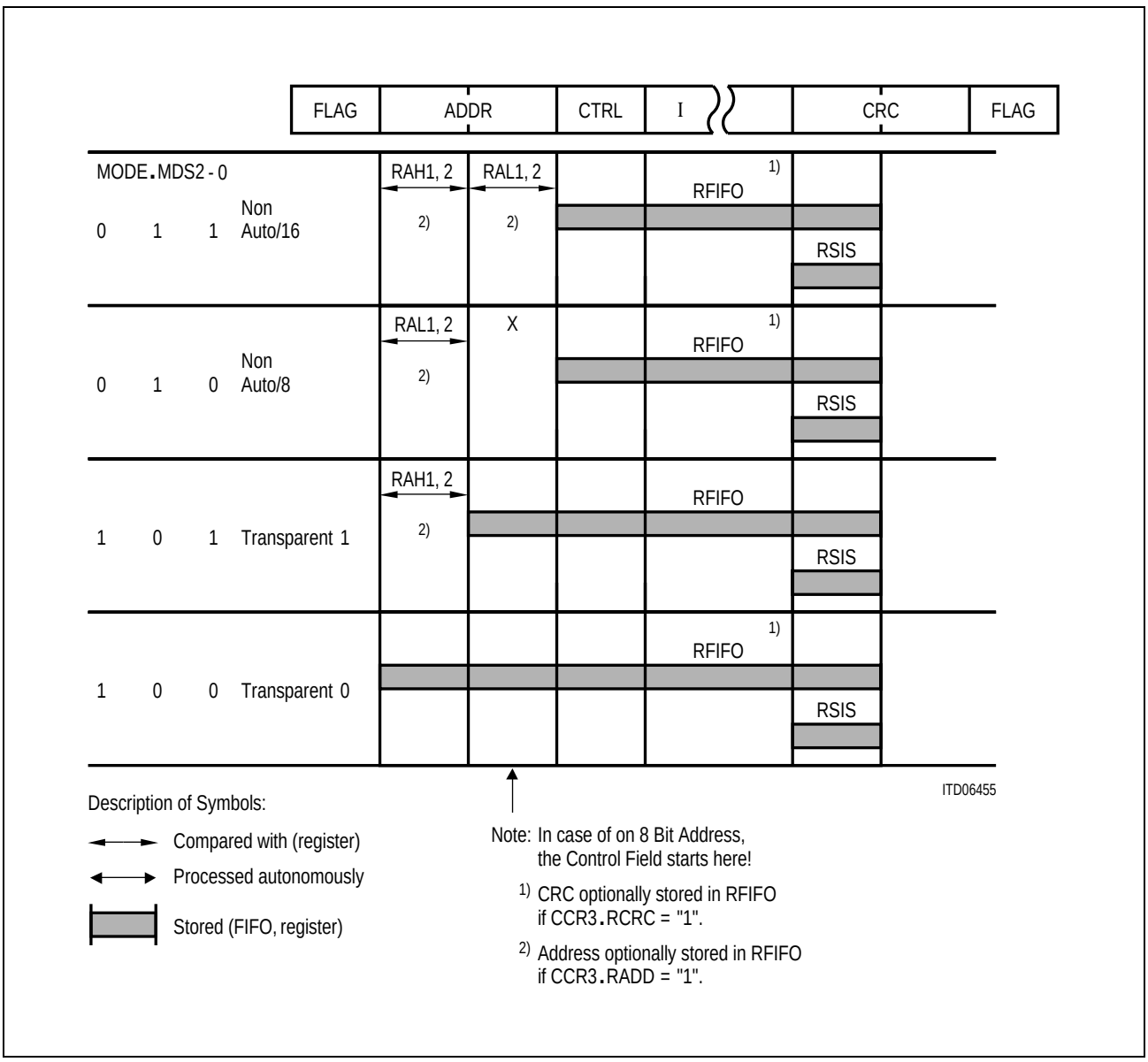


Figure 29
Receive Data Flow of QuadFALC

Transmit Data Flow

The frames can be transmitted as shown below.

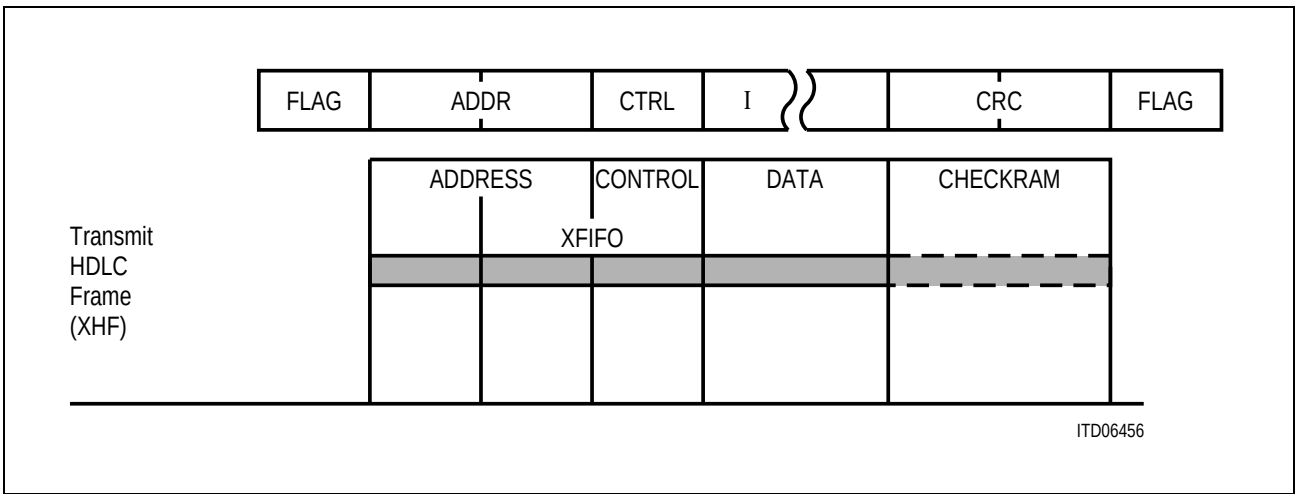


Figure 30
Transmit Data Flow of QuadFALC

Transmitting a HDLC frame via register CMDR.XTF, the address, the control fields and the data field have to be entered in the XFIFO.

If CCR3.XCRC is set, the CRC checksum will not be generated internally. The checksum has to be provided via the transmit FIFO (XFIFO) as the last two bytes. The transmitted frame will be closed automatically only with a (closing) flag.

The QuadFALC does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.

4.1.2 Extended Transparent Mode

Characteristics: fully transparent

In no HDLC mode, fully transparent data transmission/reception without HDLC framing is performed, i.e. without FLAG generation/recognition, CRC generation/check, or bit-stuffing. This feature can be profitably used e.g for:

- Specific protocol variations
- Transmission of a BOM frame
- Test purposes

Data transmission is always performed out of the XFIFO. In transparent mode, the receive data is shifted into the RFIFO.

4.1.3 Signaling Controller Functions

Shared Flags

The closing Flag of a previously transmitted frame simultaneously becomes the opening Flag of the following frame if there is one to be transmitted. The Shared Flag feature is enabled by setting bit SFLG in control register CCR1.

Transparent Transmission and Reception

When programmed in the extended transparent mode via the MODE register (MDS2-0 = 111), the QuadFALC performs fully transparent data transmission and reception without HDLC framing, i.e. without

- FLAG insertion and deletion
- CRC generation and checking
- Bit-stuffing

In order to enable fully transparent data transfer, bit MODE.HRAC has to be set.

Received data is always shifted into RFIFO.

Data transmission is always performed out of XFIFO by directly shifting the contents of XFIFO in the outgoing datastream. Transmission is initiated by setting CMDR.XTF (04_H). A synch-byte FF_H is automatically sent before the first byte of the XFIFO will be transmitted.

Cyclic Transmission (fully transparent)
If the extended transparent mode is selected, the QuadFALC supports the continuous transmission of the contents of the transmit FIFO.

After having written 1 to 32 bytes to XFIFO, the command XREP.XTF via the CMDR register (bit 7 … 0 = '00100100' = 24_H) forces the QuadFALC to transmit the data stored in XFIFO repeatedly to the remote end.

Note: The cyclic transmission continues until a reset command (CMDR: SRES) is issued or with resetting CMDR.XREP, after which continuous '1'-s are transmitted. During cyclic transmission the XREP-bit has to be set with every write operation to CMDR.

CRC ON/OFF Features

As an option in HDLC mode the internal handling of received and transmitted CRC checksum can be influenced via control bits CCR3.RCRC and CCR3.XCRC.

- Receive Direction
  The received CRC checksum is always assumed to be in the 2 (CRC-ITU) last bytes of a frame, immediately preceding a closing flag. If CCR3.RCRC is set, the received CRC checksum will be written to RFIFO where it precedes the frame status byte (contents of register RSIS). The received CRC checksum is additionally checked for

correctness. If HDLC mode is selected, the limits for ‘Valid Frame’ check are modified (refer to description of bit RSIS.VFR).

- Transmit Direction
  If CCR3.XCRC is set, the CRC checksum is not generated internally. The checksum has to be provided via the transmit FIFO (XFIFO) as the last two bytes. The transmitted frame will only be closed automatically with a (closing) flag.
  The QuadFALC does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.

4.1.3.1 HDLC Data Transmission

In transmit direction 2x32 byte FIFO buffers are provided. After checking the XFIFO status by polling the bit SIS.XFW or after an interrupt ISR1.XPR (Transmit Pool Ready), up to 32 bytes may be entered by the CPU to the XFIFO.

The transmission of a frame can be started by issuing a XTF or XHF command via the command register. If the transmit command does not include an end of message indication (CMDR.XME), the QuadFALC will repeatedly request for the next data block by means of a XPR interrupt as soon as no more than 32 bytes are stored in the XFIFO, i.e. a 32-byte pool is accessible to the CPU.

This process will be repeated until the CPU indicates the end of message per XME command, after which frame transmission is finished correctly by appending the CRC and closing flag sequence. Consecutive frames may be share a flag, or may be transmitted as back-to-back frames, if service of XFIFO is quick enough.

In case no more data is available in the XFIFO prior to the arrival of XME, the transmission of the frame is terminated with an abort sequence and the CPU is notified per interrupt ISR1.XDU. The frame may be aborted per software CMDR.SRES.

The data transmission sequence, from the CPU's point of view, is outlined in **figure 31**.

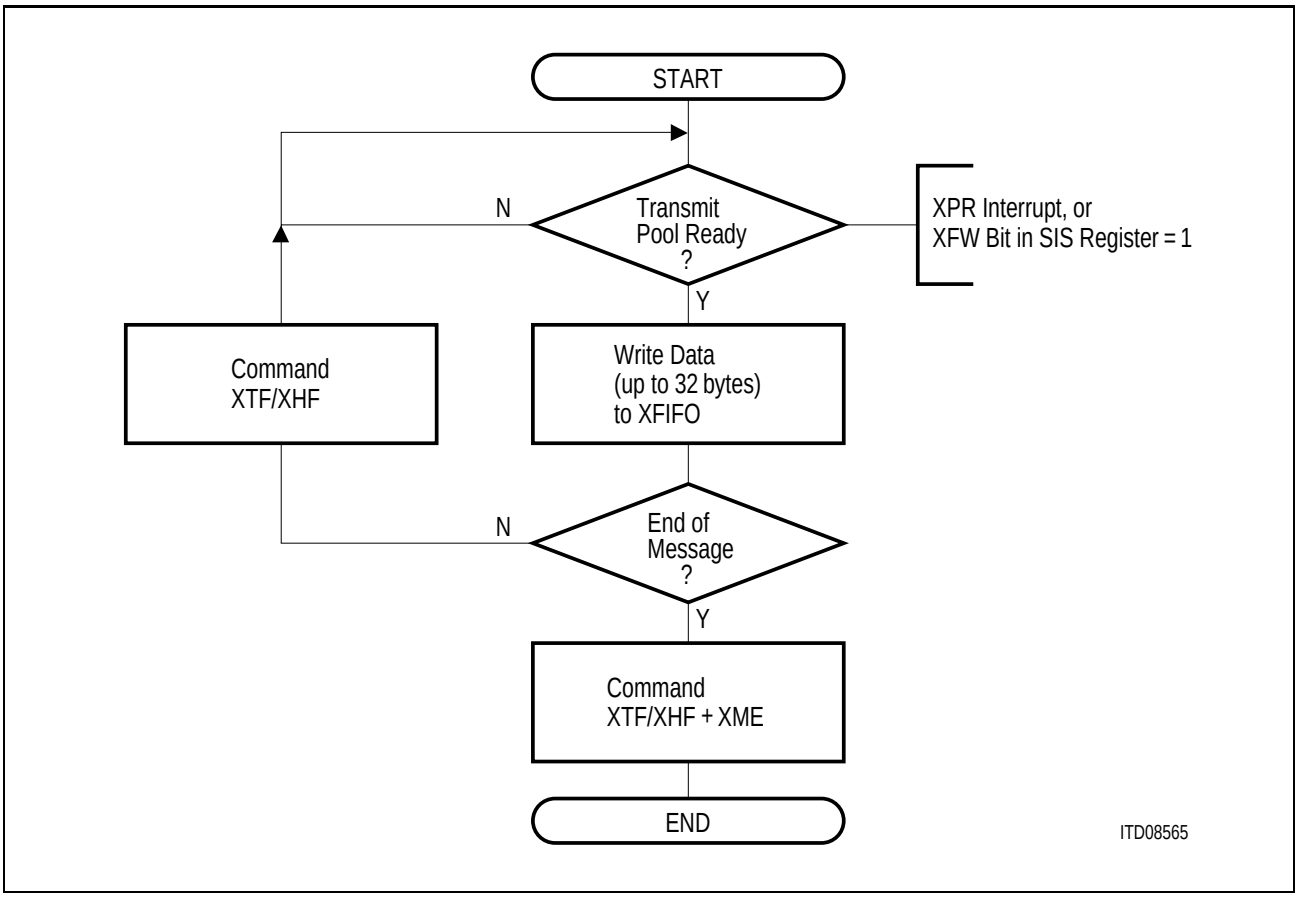


Figure 31
Interrupt Driven Data Transmission (flow diagram)

The activities at both serial and CPU interface during frame transmission (supposed frame length = 70 bytes) shown in **figure 32**.

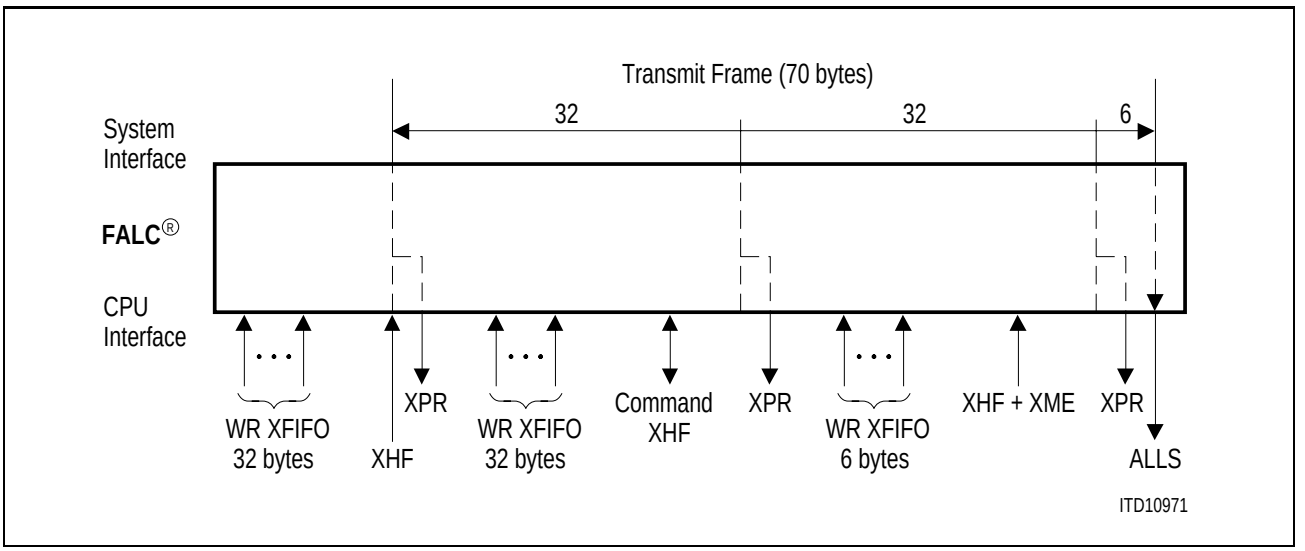


Figure 32
Interrupt Driven Transmission Example

4.1.3.2 HDLC Data Reception

Also 2×32 byte FIFO buffers are provided in receive direction. There are different interrupt indications concerned with the reception of data:

RPF (Receive Pool Full) interrupt, indicating that a 32-byte-block of data can be read from RFIFO and the received message is not yet complete.

RME (Receive Message End) interrupt, indicating that the reception of one message is completed.

The following figure gives an example of a reception sequence, assuming that a “long” frame (66 bytes) followed by two short frames (6 bytes each) are received.

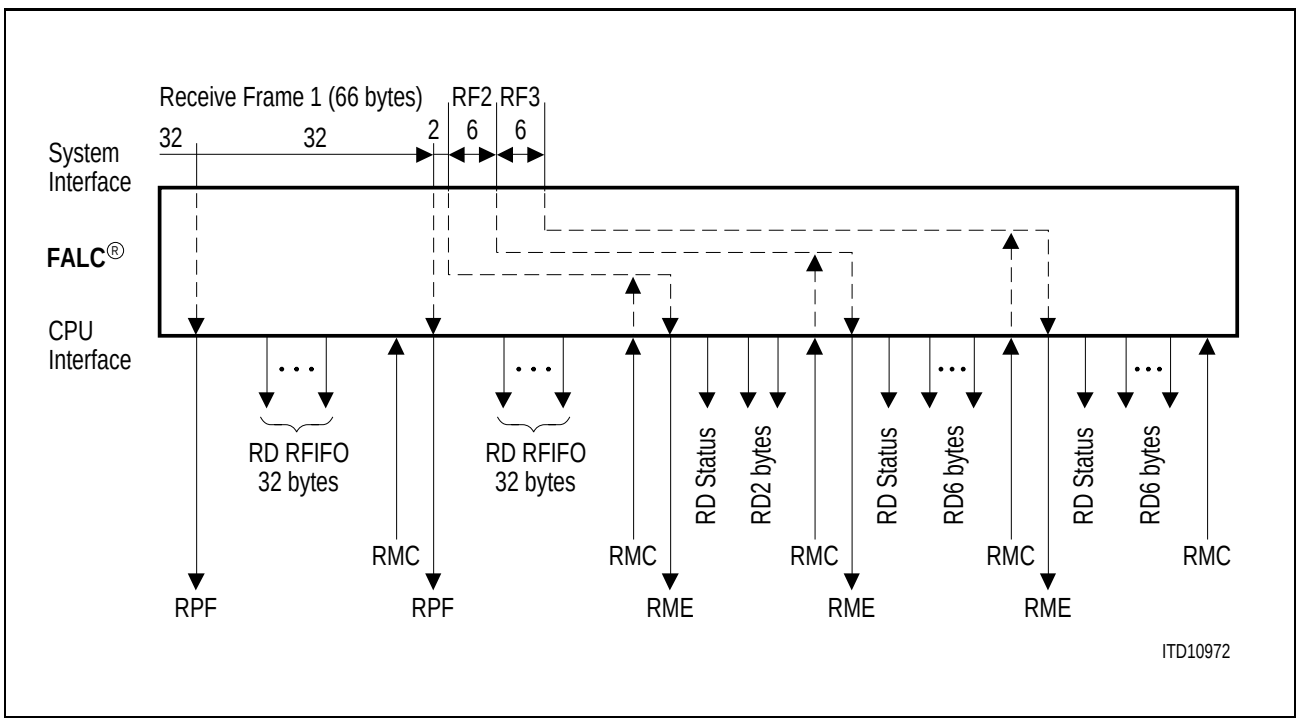


Figure 33
Interrupt Driven Reception Sequence Example

4.1.4 S_a bit Access

The QuadFALC supports the S_a bit signaling of time-slot 0 of every other frame as follows:

- The access via registers RSW / XSW
- the access via registers RSA8-4 / XSA4-8
  capable of storing the information for a complete multiframe
- the access via the 64 byte deep receive/transmit FIFO of the integrated signaling controller. This S_a bit access gives the opportunity to transmit/receive a transparent bit stream as well as HDLC frames where the signaling controller automatically processes the HDLC protocol. Enabling is done by setting of bit CCR1.EITS and resetting of registers TTR1-4, RTR1-4 and FMR1.ENSA.
  The data written to the XFIFO will subsequently transmit in the S_a bit positions defined by register XC0.SA8E-4E and the corresponding bits of TSWM.TSA8-4. Any combination of S_a bits can be selected. After the data have been completely sent out an “all ones” or Flags (CCR1.ITF) will be transmitted. The continuous transmission of a transparent bit stream, which is stored in the XFIFO, can be enabled.
  With the setting of bit MODE.HRAC the received S_a bits can be forwarded to the receive FIFO.
  The access to and from the FIFOs is supported by ISR0.RME/RPF and ISR1.XPR/ALS.

4.2 Operational Phase

The QuadFALC is programmable via a microprocessor interface which enables byte or word access to all control and status registers.

After RESET the QuadFALC must be first initialized. General guidelines for initialization are described in section **Initialization**.

The status registers are read-only and are continuously updated. Normally, the processor periodically reads the status registers to analyze the alarm status and signaling data.

Reset

The QuadFALC is forced to the reset state if a high signal is input at port RES for a minimum period of 10 µs. During RESET the QuadFALC needs an active clock on pin MCLK. All output stages are in a high impedance state, all internal flip-flops are reset and most of the control registers are initialized with default values.

After RESET, the QuadFALC is initialized for doubleframe format with register values listed in **Table 9**.

Table 9
Initial Values after RESET

Register	Reset Value	Meaning
FMR0	00_H	NRZ Coding, no alarm simulation.
FMR1 FMR2	00_H	PCM 30 – doubleframe format, 2 MBit/s system data rate, no AIS transmission to remote end or system interface, Payload Loop off.
SIC1 SIC2, SIC3	00_H 00_H 00_H	8.192 MHz system clocking rate, Rec. Buffer 2 Frames, Transmit Buffer bypass, Data sampled or transmitted on the falling edge of SCLKR/X, Automatic freeze signaling, data is active in the first channel phase
LOOP XSW XSP TSWM	00_H 40_H 00_H 00_H	Channel loop back and single frame mode are disabled. All bits of the transmitted service word are cleared (bit 2 excl.). Spare bit values are cleared. No transparent mode active.
XC0 XC1	00_H 00_H	The transmit clock offset is cleared. The transmit time-slot offset is cleared.
RC0 RC1	00_H 00_H	The receive clock slot offset is cleared. The receive time-slot offset is cleared.
IDLE ICB 1 … 4	00_H 00_H	Idle channel code is cleared. Normal operation (no ‘Idle Channel’ selected).
LIM0 LIM1 PCD PCR	00_H 00_H 00_H 00_H	Slave Mode, Local Loop off Analog interface selected, Remote Loop off Pulse Count for LOS Detection cleared Pulse Count for LOS Recovery cleared
XPM2-0	00_H, 03_H, $9C_H$	Transmit Pulse Mask
IMR0-4	FF_H,FF_H,FF_H, FF_H,FF_H,	All interrupts are disabled
RTR1-4 TTR1-4	00_H,00_H,00_H, 00_H,	No time-slots selected
GCR	00_H	Internal second timer, Power on of all 4 single FALC channels,
CMR1	00_H	DCO-R reference clock: channel 1, RCLK output: DPLL clock, DCO-X enabled, DCO-X internal reference clock

Table 9
Initial Values after RESET (cont'd)

Register	Reset Value	Meaning
CMR2	00_H	SCLKR selected, SCLKX selected, Rec. synchr. pulse sourced by $\overline{SYPR}$, Tr. synchr. pulse sourced by $\overline{SYPX}$,
GPC1	00_H	system multiplex mode disabled, SEC port input active high, FSC is sourced by channel 1, RCLK1 clock source: channel 1,
PC1-4	00_H , 00_H 00_H , 00_H	Input function of ports RP(A-D) : $\overline{SYPR}$, Input function of ports XP(A-D) : $\overline{SYPX}$
PC5	00_H	SCLKR, SCLKX, RCLK configured to inputs, XMFS active low
MODE	00_H	Signaling controller disabled
RAH1/2 RAL1/2	FD_H, FF_H FF_H, FF_H	Compare register for receive address cleared

Initialization

For a correct start up of the Primary Access Interface a set of parameters specific to the system and hardware environment must be programmed after RESET goes inactive. Both the basic and the operational parameters must be programmed **before** the activation procedure of the PCM line starts. Such procedures are specified in ITU-T and ETSI recommendations (e.g. Fault conditions and consequent actions). Setting optional parameters primarily makes sense when basic operation via the PCM line is guaranteed. **Table 10** gives an overview of the most important parameters in terms of signals and control bits which are to be programmed in one of the above steps. The sequence is recommended but not mandatory. Accordingly, parameters for the basic and operational set up, for example, may be programmed simultaneously. The bit FMR1.PMOD should always be kept low.

Table 10
Initialization Parameters

Basic Set Up	E1
Mode Select	FMR1.PMOD = 0
Specification of Line interface and clock generation	LIM0, LIM1, XPM2-0
Line interface coding	FMR0.XC1/0, FMR0.RC1/0
Loss of Signal detection/recovery conditions	PCD, PCR, LIM1, LIM2
System clocking and data rate	SIC1.SSC1/0, SIC1.SSD1,FMR1.SSD0 CMR2.IRSP/IRSC/ IXSP/IXSC
Transmit offset counters	XC0.XCO, XC1.XTO
Receive offset counters	RC0.RCO, RC1.RTO
AIS to system interface	FMR2.DAIS/SAIS

Operational Set Up	E1
Select framing	FMR2.RFS1/0, FMR1.XFS
Framing additions	RC1.ASY4, RC1.SWD
Synchronization mode	FMR1.AFR, FMR2.ALMF
Signaling mode	XSP, XSW, FMR1.ENSA, XSA8-4, TSWM, MODE, CCR1, CCR2, RAH1/2, RAL1/2

Features like channel loop back, idle channel activation, extensions for signaling support, alarm simulation, …may be activated later. Transmission of alarms (e.g. AIS, remote alarm) and control of synchronization in connection with consequent actions to remote end and internal system depend on the activation procedure selected.

Note: Read access to unused register addresses: value should be ignored.
Write access to unused register addresses: should be avoided, or set to '00' hex.
All control registers (except XFIFO, XS1-16, CMDR, DEC) are of type: Read/Write.

4.3 Specific E1 Initialization

The following is a suggestion for a basic initialization to meet most of the E1 requirements. Depending on different applications and requirement any other initialization can be used.

LIU Initialization

FMR0.XC0/ FMR0.RC0/ LIM1.DRS FMR3.CMI	The QuadFALC supports requirements for the analog line interface as well as the digital line interface. For the analog line interface the codes AMI and HDB3 are supported. For the digital line interface modes (dual or single rail) the QuadFALC supports AMI, HDB3, CMI (with and without HDB3 precoding) and NRZ.
PCD = 0x0A	LOS detection after 176 consecutive “zeros” (fulfills G.775 spec).
PCR = 0x15	LOS recovery after 22 “ones” in the PCD intervall. (fulfills G.775).
LIM1.RIL2-0 = 0x02	LOS threshold of 0.6 V (fulfills G.775).

Framer Initialization

The selection of the following modes during the basic initialization supports the ETSI requirements for E-Bit Access, Remote Alarm and Synchronization (please refer also to QuadFALC driver code of the Evaluation System EASY22554 and application notes) and helps to reduce the software load. They are very helpful especially to meet requirements as specified in ETS300 011.

XSP.AXS = 1	ETS300 011 C4.x for instance requires the sending of E-Bits in TS0 if CRC4 errors have been detected. By programming XSP.AXS = 1 the submultiframe status is inserted automatically in the next outgoing multiframe.
XSP.EBP = 1	If the QuadFALC has reached asynchronous state the E-Bit is set to 0 if XSP.EBP = 0 and set to 1 if XSP.EBP = 1. ETS300 011 requires that the E-Bit is set to 1 in asynchronous state.
FMR2.AXRA = 1	The transmission of RAI via the line interface is done automatically by the QuadFALC in case of Loss of Frame Alignment (FRS0.LFA = 1). If basic framing has been reinstalled RAI is automatically reset.
FMR2.FRS1/2 = 10 FMR1.AFR = 1	In this mode a search of double framing is automatically reinitiated if no CRC4 multiframing could be found within 8ms. Together with FMR2.AXRA = 1 this mode is essential to meet ETS300 011 and reduces the processor load heavily.

FMR2.ALMF = 1	The receiver initiates a new basic- and multiframing research if more than 914 CRC4 errors have been detected in one second.
FMR2.FRS1/0 = 11	In the interworking mode the QuadFALC stays in double framing format if no multiframe pattern could be found in a time intervall of 400 ms. This is also indicated by a 400 ms interrupt. Additionally the extended interworking mode (FMR3.EXTIW = 1) will activate after 400 ms the remote alarm (FMR2.AXRA = 1) and will still search the multiframing without switching completely to the double framing. A complete resynchronization in an 8 ms interval is not initiated.

Signaling Controller Initialization

Initialization of the HDLC controller:

MODE = 0x88	HDLC Receiver active, no address comparison.
CCR1 = 0x18	Enable Signaling via TS0-31, Interframe Time Fill with continous FLAGs.
IMR0.RME = 0 IMR0.RPF = 0 IMR1.XPR = 0	Unmask interrupts for HDLC processor requests.
RTR3.TS16 = 1 XTR3.TS16 = 1	Select TS16 for HDLC data reception and transmission.

Initialization of the CAS-CC controller:

XSP.CASEN = 1 CCR1.EITS = 0	Send CAS infos stored in the XS1-16 registers.
IMR0.CASC = 0	Enable interrupt with any data change in the RS1-16 registers.

After the device initialization a software reset should be executed by setting of bits CMDR.XRES/RRES.

4.4 Control Register Description

Table 11
Control Register Address Arrangement

Address				Register	Type	Comment
00	100	200	300	XFIFO	W	Transmit FIFO
01	101	201	301	XFIFO	W	Transmit FIFO
02	102	202	302	CMDR	W	Command Register
03	103	203	303	MODE	R/W	Mode Register
04	104	204	304	RAH1	R/W	Receive Address High 1
05	105	205	305	RAH2	R/W	Receive Address High 2
06	106	206	306	RAL1	R/W	Receive Address Low 1
07	107	207	307	RAL2	R/W	Receive Address Low 2
08				IPC	R/W	Interrupt Port Configuration
09	109	209	309	CCR1	R/W	Common Configuration Register 1
0A	10A	20A	30A	CCR2	R/W	Common Configuration Register 2
0C	10C	20C	30C	RTR1	R/W	Receive Timeslot Register 1
0D	10D	20D	30D	RTR2	R/W	Receive Timeslot Register 2
0E	10E	20E	30E	RTR3	R/W	Receive Timeslot Register 3
0F	10F	20F	30F	RTR4	R/W	Receive Timeslot Register 4
10	110	210	310	TTR1	R/W	Transmit Timeslot Register 1
11	111	211	311	TTR2	R/W	Transmit Timeslot Register 2
12	112	212	312	TTR3	R/W	Transmit Timeslot Register 3
13	113	213	313	TTR4	R/W	Transmit Timeslot Register 4
14	114	214	314	IMR0	R/W	Interrupt Mask Register 0
15	115	215	315	IMR1	R/W	Interrupt Mask Register 1
16	116	216	316	IMR2	R/W	Interrupt Mask Register 2
17	117	217	317	IMR3	R/W	Interrupt Mask Register 3
18	118	218	318	IMR4	R/W	Interrupt Mask Register 4
1C	11C	21C	31C	FMR0	R/W	Framer Mode Register 0
1D	11D	21D	31D	FMR1	R/W	Framer Mode Register 1
1E	11E	21E	31E	FMR2	R/W	Framer Mode Register 2
1F	11F	21F	31F	LOOP	R/W	Channel Loop Back
20	120	220	320	XSW	R/W	Transmit Service Word

Table 11
Control Register Address Arrangement (cont'd)

Address				Register	Type	Comment
21	121	221	321	XSP	R/W	Transmit Spare Bits
22	122	222	322	XC0	R/W	Transmit Control 0
23	123	223	323	XC1	R/W	Transmit Control 1
24	124	224	324	RC0	R/W	Receive Control 0
25	125	225	325	RC1	R/W	Receive Control 1
26	126	226	326	XPM0	R/W	Transmit Pulse Mask 0
27	127	227	327	XPM1	R/W	Transmit Pulse Mask 1
28	128	228	328	XPM2	R/W	Transmit Pulse Mask 2
29	129	229	329	TSWM	R/W	Transparent Service Word Mask
2B	12B	22B	32B	IDLE	R/W	Idle Channel Code
2C	12C	22C	32C	XSA4	R/W	Transmit SA4 Bit Register
2D	12D	22D	32D	XSA5	R/W	Transmit SA5 Bit Register
2E	12E	22E	32E	XSA6	R/W	Transmit SA6 Bit Register
2F	12F	22F	32F	XSA7	R/W	Transmit SA7 Bit Register
30	130	230	330	XSA8	R/W	Transmit SA8 Bit Register
31	131	231	331	FMR3	R/W	Framer Mode Register 3
32	132	232	332	ICB1	R/W	Idle Channel Register 1
33	133	233	333	ICB2	R/W	Idle Channel Register 2
34	134	234	334	ICB3	R/W	Idle Channel Register 3
35	135	235	335	ICB4	R/W	Idle Channel Register 4
36	136	236	336	LIM0	R/W	Line Interface Mode 0
37	137	237	337	LIM1	R/W	Line Interface Mode 1
38	318	238	338	PCD	R/W	Pulse Count Detection
39	139	239	339	PCR	R/W	Pulse Count Recovery
3A	13A	23A	33A	LIM2	R/W	Line Interface Mode 2
3B	13B	23B	33B	LCR1	R/W	Loop Code Register 1
3C	13C	23C	33C	LCR2	R/W	Loop Code Register 2
3D	13D	23D	33D	LCR3	R/W	Loop Code Register 3
3E	13E	23E	33E	SIC1	R/W	System Interface Control 1
3F	13F	23F	33F	SIC2	R/W	System Interface Control 2

Table 11
Control Register Address Arrangement (cont'd)

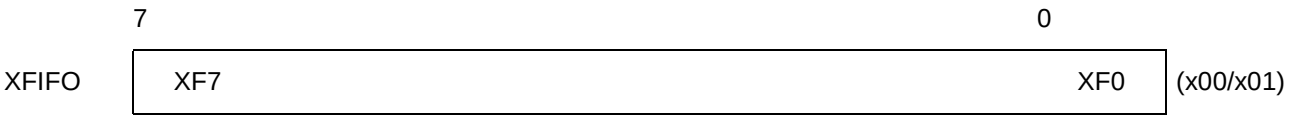
Address				Register	Type	Comment
40	140	240	340	SIC3	R/W	System Interface Control 3
44	144	244	344	CMR1	R/W	Clock Mode Register 1
45	145	245	345	CMR2	R/W	Clock Mode Register 2
46	146	246	346	GCR	R/W	Global Configuration Register
47	147	247	347	ESM	R/W	Errored Second Mask
60	160	260	360	DEC	W	Disable Error Counter
70	170	270	370	XS1	W	Transmit CAS Register 1
71	171	271	371	XS2	W	Transmit CAS Register 2
72	172	272	372	XS3	W	Transmit CAS Register 3
73	173	273	373	XS4	W	Transmit CAS Register 4
74	174	274	374	XS5	W	Transmit CAS Register 5
75	175	275	375	XS6	W	Transmit CAS Register 6
76	176	276	376	XS7	W	Transmit CAS Register 7
77	177	277	377	XS8	W	Transmit CAS Register 8
78	178	278	378	XS9	W	Transmit CAS Register 9
79	179	279	379	XS10	W	Transmit CAS Register 10
7A	17A	27A	37A	XS11	W	Transmit CAS Register 11
7B	17B	27B	37B	XS12	W	Transmit CAS Register 12
7C	17C	27C	37C	XS13	W	Transmit CAS Register 13
7D	17D	27D	37D	XS14	W	Transmit CAS Register 14
7E	17E	27E	37E	XS15	W	Transmit CAS Register 15
7F	17F	27F	37F	XS16	W	Transmit CAS Register 16
80	180	280	380	PC1	R/W	Port Configuration 1
81	181	281	381	PC2	R/W	Port Configuration 2
82	182	282	382	PC3	R/W	Port Configuration 3
83	183	283	383	PC4	R/W	Port Configuration 4
84	184	284	384	PC5	R/W	Port Configuration 5
85				GPC1	R/W	Global Port Configuration 1

After ‘RESET’ all control registers except the XFIFO and XS1-16 are initialized to defined values.

Unused bits have to be set to logical ‘0’.

The status registers are only readable and are updated by the QuadFALC.

Transmit FIFO (WRITE) XFIFO

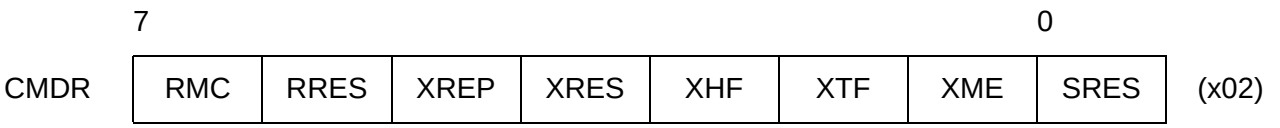


Up to 32 bytes/16 words of received data can be read from the RFIFO following a RPF or a RME interrupt.
Writing data to XFIFO can be done in 8-bit (byte) or 16-bit (word) access. The LSB is transmitted first.

Up to 32 bytes/16 words of transmit data can be written to the XFIFO following a XPR (or ALLS) interrupt.

Command Register (Write)

Value after RESET: 00_H



RMC… **Receive Message Complete**

Confirmation from CPU to QuadFALC that the current frame or data block has been fetched following a RPF or RME interrupt, thus the occupied space in the RFIFO can be released.

RRES… **Receiver Reset**

The receive line interface except the clock and data recovery unit (DPLL), the receive framer, the one second timer and the receive signaling controller are reset. However the contents of the control registers will not be deleted.

XREP… **Transmission Repeat**

If XREP is set to one together with XTF (write 24_H to CMDR), the QuadFALC repeatedly transmits the contents of the XFIFO (1 … 32 bytes) without HDLC framing fully transparently, i.e. without FLAG,CRC.

The cyclic transmission is stopped with a SRES command or by resetting XREP.

Note: During cyclic transmission the XREP-bit has to be set with every write operation to CMDR.

XRES… Transmitter Reset

The transmit framer and transmit line interface excluding the system clock generator and the pulse shaper will be reset. However the contents of the control registers will not be deleted.

XHF… Transmit HDLC Frame

After having written up to 32 bytes to the XFIFO, this command initiates the transmission of a HDLC frame.

XTF… Transmit Transparent Frame

Initiates the transmission of a transparent frame without HDLC framing.

XME… Transmit Message End

Indicates that the data block written last to the transmit FIFO completes the current frame. The QuadFALC can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data.

SRES… Signaling Transmitter Reset

The transmitter of the signaling controller will be reset. XFIFO is cleared of any data and an abort sequence (seven 1's) followed by interframe time fill is transmitted. In response to XRES a XPR interrupt is generated.

This command can be used by the CPU to abort a frame currently in transmission.

Note: The maximum time between writing to the CMDR register and the execution of the command takes 2.5 periods of the current system data rate. Therefore, if the CPU operates with a very high clock rate in comparison with the QuadFALC's clock, it is recommended that bit SIS.CEC should be checked before writing to the CMDR register to avoid any loss of commands.

Mode Register (Read/Write)

Value after RESET: 00_H

	7							0	
MODE	MDS2	MDS1	MDS0		HRAC	DIV			(x03)

MDS2-0… **Mode Select**

The operating mode of the HDLC controller is selected.

000… Reserved
001… Reserved
010… 1 byte address comparison mode (RAL1,2)
011… 2 byte address comparison mode (RAH1,2 and RAL1,2)
100… No address comparison
101… 1 byte address comparison mode (RAH1,2)
110… Reserved
111… No HDLC framing mode

HRAC… **HDLC Receiver Active**

Switches the HDLC receiver to operational or inoperational state.

0… Receiver inactive
1… Receiver active

DIV… **Data Inversion**

Setting this bit will invert the internal generated HDLC data stream.

0… normal operation, HDLC data stream not inverted
1… HDLC data stream inverted

Receive Address Byte High Register 1 (Read/Write)
Value after RESET: FD_H

	7	1	0	
RAH1		0		(x04)

In operating modes that provide high byte address recognition, the high byte of the received address is compared with the individually programmable values in RAH1 and RAH2.

RAH1… **Value of the First Individual High Address Byte**

Bit 1 (C/R-bit) is excluded from address comparison.

Receive Address Byte High Register 2 (Read/Write)
Value after RESET: FF_H

	7	0	
RAH2			(x05)

RAH2… Value of Second Individual High Address Byte

Receive Address Byte Low Register 1 (Read/Write)
Value after RESET: FF_H

	7	0	
RAL1			(x06)

RAL1… Value of First Individual Low Address Byte

Receive Address Byte Low Register 2 (Read/Write)
Value after RESET: FF_H

	7	0	
RAL2			(x07)

RAL2... Value of the second individually programmable low address byte.

Interrupt Port Configuration (READ/WRITE)

Value after RESET: 00_H

	7							0	
IPC						SSYF	IC1	IC0	(08)

Note: Unused bits have to be set to logical '0'.

SSYF… **Select SYNC Frequency**

Only appilcable in master mode (LIM0.MAS = 1) and bit CMR2.DCF is cleared.

0… Reference clock at port SYNC is 2.048 MHz
1… Reference clock at port SYNC is 8 KHz

IC0, IC1… **Interrupt Port Configuration**

These bits define the function of the interrupt output stage (pin INT):

IC1	IC0	Function
X	0	Open drain output
0	1	Push/pull output, active low
1	1	Push/pull output, active high

Common Configuration Register 1 (READ/WRITE)

Value after RESET: 00_H

	7							0	
CCR1			CASM	EITS	ITF	XMFA	RFT1	RFT0	(x09)

CASM… **CAS Synchronization Mode**

Determines the synchronization mode of the channel associated signaling multiframe alignment.

0… Synchronization is done in accordance to ITU-T G. 732

1… Synchronization is established when two consecutively correct multiframe alignment pattern are found.

EITS… **Enable Internal Time-Slot 0-31 Signaling**

0… Internal signaling in time-slots 0-31 defined via registers RTR1-4 or TTR1-4 is disabled.

1… Internal signaling in time-slots 0-31 defined via registers RTR1-4 or TTR1-4 is enabled.

ITF… **Interframe Time Fill**

Determines the idle (= no data to send) state of the transmit data coming from the signaling controller.

0… Continuous logical ‘1’ is output

1… Continuous FLAG sequences are output (‘01111110’ bit patterns)

XMFA … **Transmit Multiframe Aligned**

Determines the synchronization between the framer and the corresponding signaling controller.

0… Contents of the XFIFO is transmitted without multiframe alignment.

1… Contents of the XFIFO is transmitted multiframe aligned. After receiving a complete multiframe in the time-slot mode (RTR1-4) an ISR0.RME interrupt is generated, if no HDLC mode is enabled. In SA4-8 bit access XMFA is not valid.

Note: During the transmission of the XFIFO content, the $\overline{SYPX}$ or XMFS interval time should not be changed, otherwise the XFIFO data has to be retransmitted.

RFT1, RFT0…RFIFO Threshold Level

The size of the accessible part of RFIFO can be determined by programming these bits. The number of valid bytes after a RPF interrupt is given in the following table:

RFT1	RFT0	Size of Accessible Part of RFIFO
0	0	32 bytes (RESET value)
0	1	16 bytes
1	0	4 bytes
1	1	2 bytes

The value of RFT1, 0 can be changed dynamically.

– If reception is not running or

– after the current data block has been read, but before the command CMDR.RMC is issued (interrupt controlled data transfer).

Note: It is seen that changing the value of RFT1, 0 is possible even during the reception of one frame. The total length of the received frame can be always read directly in RBCL, RBCH after a RPF interrupt, except when the threshold is increased during reception of that frame. The real length can then be inferred by noting which bit positions in RBCL are reset by a RMC command (see table below):

RFT1	RFT0	Bit Positions in RBCL Reset by a CMDR.RMC Command
0	0	RBC4 …. 0
0	1	RBC3 … 0
1	0	RBC1,0
1	1	RBC0

Common Configuration Register 2 (READ/WRITE)

Value after RESET: 00_H

	7							0	
CCR2				RADD		RCRC	XCRC		(x0A)

Note: Unused bits have to be set to logical '0'.

RADD… Receive Address Pushed to RFIFO

If this bit is set to '1', the received HDLC address information (1 or 2 bytes, depending on the address mode selected via MODE.MDS0) is pushed to RFIFO. This function is applicable in non-auto mode.

RCRC… Receive CRC ON/OFF

Only applicable in non-auto mode.

If this bit is set to '1', the received CRC checksum will be written to RFIFO (CRC-ITU-T: 2 bytes). The checksum, consisting of the 2 last bytes in the received frame, is followed in the RFIFO by the status information byte (contents of register RSIS). The received CRC checksum will additionally be checked for correctness. If non-auto

mode is selected, the limits for “Valid Frame” check are modified (**refer to RSIS.VFR**).

XCRC… Transmit CRC ON/OFF

If this bit is set to ‘1’, the CRC checksum will not be generated internally. It has to be written as the last two bytes in the transmit FIFO (XFIFO). The transmitted frame will be closed automatically with a closing flag.

Note: The QuadFALC does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.

Receive Timeslot Register 1-4 (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H

	7							0	
RTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7	(x0C)
RTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	(x0D)
RTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	(x0E)
RTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	(x0F)

TS0…TS31… Timeslot Register

These bits define the received time-slots on the system highway port RDO to be extracted to RFIFO and marked. Additionally these registers will control the RSIGM marker which can be forced high during the respective time-slots independenltly of bit CCR1.EITS.
A one in the RTR1-4 bits will sample the corresponding time-slots and send their data to the RFIFO of the signaling controller if bit CCR1.EITS is set.

Assignments:
TS0 → time-slot 0
.
.
.

TS31→ time-slot 31

0 …The corresponding time-slot is not extracted and stored into the RFIFO.

1…The contents of the selected time-slot will be stored in the RFIFO. Although the idle time-slots can be selected. This function will only become active if bits CCR1.EITS is set.
The corresponding time-slot will be forced high on marker pin RSIGM.

Transmit Timeslot Register 1-4 (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H

	7							0	
TTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7	(x10)
TTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	(x11)
TTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	(x12)
TTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	(x13)

TS0…TS31… Transmit Timeslot Register

These bits define the transmit time-slots on the system highway to be inserted. Additionally these registers will control the XSIGM marker which can be forced high during the respective time-slots independently of bit CCR1.EITS.
A one in the TTR1-4 bits will insert the corresponding time-slot sourced by the XFIFO in the data received on pin XDI, if bit CCR1.EITS is set. If SIC3.TTRF is set and CCR1.EITS is cleared insertion of data received on port XSIG is controlled by this registers.

Assignments:
TS0 $\rightarrow$ time-slot 0

.

.

.
TS31 $\rightarrow$ time-slot 31

0 …The selected time-slot will not be inserted into the outgoing data stream.

1…The contents of the selected time-slot will be inserted in the outgoing data stream from XFIFO. This function will only become active if bits CCR1.EITS is set.
The corresponding time-slot will be forced high on marker pin XSIGM.

Interrupt Mask Register 0 ... 4 (READ/WRITE)

Value after RESET: FF_H, FF_H, FF_H, FF_H, FF_H

	7							0	
IMR0	RME	RFS	T8MS	RMB	CASC	CRC4	SA6SC	RPF	(x14)
IMR1	LLBSC	RDO	ALLS	XDU	XMB		XLSC	XPR	(x15)
IMR2	FAR	LFA	MFAR	T400MS	AIS	LOS	RAR	RA	(x16)
IMR3	ES	SEC	LMFA16	AIS16	RA16		RSN	RSP	(x17)
IMR4	XSP	XSN							(x18)

IMR0...IMR4... Interrupt Mask Register

Each interrupt source can generate an interrupt signal on port INT (characteristics of the output stage are defined via register IPC). A ‘1’ in a bit position of IMR0 ... 4sets the mask active for the interrupt status in ISR0 ... 4. Masked interrupt statuses neither generate a signal on INT, nor are they visible in registers GIS or CIS . Moreover, they will

– not be displayed in the Interrupt Status Register if bit GCR.VIS is set to ‘0’

– be displayed in the Interrupt Status Register if bit GCR.VIS is set to ‘1’.

*Note: After RESET, all interrupts are **dis**abled.*

Framer Mode Register 0 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR0	XC1	XC0	RC1	RC0	EXTD	ALM	FRS	SIM	(x1C)

XC1... XC0… Transmit Code

Serial code transmitter is independent to the receiver.

00... NRZ (optical interface)

01... CMI (1T2B + HDB3), (optical interface)

10... AMI (ternary or digital dual rail interface)

11... HDB3 Code (ternary or digital dual rail interface)

RC1... RC0… Receive Code

Serial code receiver is independent to the transmitter.

00... NRZ (optical interface)

01... CMI (1T2B+HDB3), (optical interface)

10... AMI (ternary or digital dual rail interface)

11... HDB3 Code (ternary or digital dual rail interface)

EXTD… Extended HDB3 Error Detection

Selects error detection mode.

0… Only double violations are detected.

1… Extended code violation detection: 0000 strings are detected additionally. Thereafter, incrementation of Code Violation Counter CVC is first done after receiving an additional four zeros.

ALM… Alarm Mode

Selects the AIS alarm detection mode.

0 ... The AIS alarm will be detected according to ETS300233.
Detection: An AIS alarm will be detected if the incoming data stream contains less than 3 zeros within a period of 512 bits and a Loss of Frame Alignment is indicated.
Recovery: The alarm will be cleared if 3 or more zeros within 512 bits will be detected or the FAS word is found.

1 ... The AIS alarm will be detected according to ITU-T G.775
Detection: An AIS alarm will be detected if the incoming data stream contains for two consecutive doubleframe periods

(1024 bits) less than 3 zeros for each doubleframe period (512 bits).
Recovery: The alarm will be cleared if within two consecutive doubleframe periods 3 or more zeros for each period of 512 bits will be detected.

FRS… Force Resynchronization

A transition from low to high will initiate a resynchronization procedure of the pulse frame and the CRC-multiframe (if enabled via bit FMR2.RFS1) starting directly after the old framing candidate.

SIM… Alarm Simulation

0… Normal operation.

1… Initiates internal error simulation of AIS, loss of signal, loss of synchronization, remote alarm, slip, framing errors, CRC errors, and code violations. The error counters FEC, CVC, CEC1 will be incremented.

Framer Mode Register 1 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR1	MFCS	AFR	ENSA	PMOD	XFS	ECM	SSD0	XAIS	(x1D)

MFCS… Multiframe Force Resynchronization

Only valid if CRC multiframe format is selected (FMR2.RFS1/0=10).

A transition from low to high will initiate the resynchronization procedure for CRC-multiframe alignment without influencing doubleframe synchronous state. In case, “Automatic Force Resynchronization” (FMR1.AFR) is enabled and multiframe alignment can not be regained, a new search of doubleframe (and CRC multiframe) is automatically initiated.

AFR… Automatic Force Resynchronization

Only valid if CRC multiframe format is selected (FMR2.RFS1/0=10).

If this bit is set, a search of doubleframe alignment is automatically initiated if two multiframe patterns with a distance of n $\times$ 2 ms have not been found within a time interval of 8 ms after doubleframe alignment has been regained or command FMR1.MFCS has been issued.

ENSA… Enable S_a-Bit Access via Register XSA4-8

Only applicable if FMR1.XFS is set to one.

0… Normal operation. The S_a-bit information will be taken from bits XSW.XY0…4 and written to bits RSW.RY0…4.

1… S_a-bit register access. The S_a-bit information will be taken from the registers XSA4-8. In addition, the received information will be written to registers RSA4-8. Transmitting contents of registers XSA4-8 will be disabled if one of time-slot 0 transparent modes is enabled (XSP.TT0 or TSWM.SA4-8).

PMOD… PCM Mode

For E1 application this bit must be set low. Switching from E1 to T1 or vv the device needs up to 10 µsec to settle up to the internal clocking.

FMR1.PMOD of all 4 channels has to be set equally.

0… PCM 30 or E1 mode.

1… PCM 24 or T1 mode.

XFS… Transmit Framing Select

Selection of the transmit framing format could be done independent of the receive framing format.

0… Doubleframe format enabled.

1… CRC4-multiframe format enabled.

ECM… Error Counter Mode

The function of the error counters will be determined by this bit.

0… Before reading an error counter the corresponding bit in the Disable Error Counter register (DEC) has to be set. In 8 bit access the low byte of the error counter should always be read before the high byte. The error counters will be reset with the rising edge of the corresponding bits in the DEC register.

1… Every second the error counter will be latched and then automatically be reset. The latched error counter state should be read within the next second. Reading the error counter during updating should be avoided.

SSD0… Select System Data Rate 0

FMR1.SSD0 and SIC1.SD1 define the data rate on the system highway. Programming is done with SSD1/SSD0 in the following table.

00…2.048 MBit/s

01…4.096 MBit/s

10…8.192 MBit/s

11…16.384 MBit/s

XAIS… Transmit AIS Towards Remote End

Sends AIS via ports XL1, XL2, XOID towards the remote end. The outgoing data stream which could be looped back via the Local Loop to the system interface will not be affected.

Framer Mode Register 2 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR2	RFS1	RFS0	RTM	DAIS	SAIS	PLB	AXRA	ALMF	(x1E)

RFS1... RFS0... Receive Framing Select

00 ... Doubleframe format

01 ... Doubleframe format

10 ... CRC4 Multiframe format

11 ... CRC4 Multiframe format with modified CRC4 Multiframe alignment algorithm (Interworking according to ITU-T G.706 Annex B). Setting of FMR3.EXTIW changes the reaction after the 400 msec timeout.

RTM… Receive Transparent Mode

Setting this bit disconnects control of the internal elastic store from the receiver. The elastic store is now in a “free running” mode without any possibility to actualize the time slot assignment to a new frame position in case of re-synchronization of the receiver. This function can be used in conjunction with the “disable AIS to system interface” feature (FMR2.DAIS) to realize undisturbed transparent reception.
This bit should be enabled in case of unframed data reception mode.

DAIS… Disable AIS to System Interface

0… AIS is automatically inserted into the data stream to RDO if QuadFALC is in asynchronous state.

1… Automatic AIS insertion is disabled. Furthermore, AIS insertion can be initiated by programming bit FMR2.SAIS.

SAIS… Send AIS Towards System Interface

Sends AIS via output RDO towards system interface. This function is not influenced by bit FMR2.DAIS.

PLB… Payload Loopback

0… Normal operation. Payload loop is disabled.

1... The payload loopback will loop the data stream from the receiver section back to transmitter section. Looped data is output on pin RDO. Data received at port XDI, XSIG, $\overline{\text{SYPX}}$ and XMFS will be ignored. With XSP.TT0=1 timeslot 0 will also be looped. If XSP.TT0=0 timeslot 0 will be generated internally. AIS is sent immediately on port RDO by setting the FMR2.SAIS bit. During payload loop is active a write access to register XC1 will set the read/write pointer of the transmit elastic buffer into its optimal position to ensure a maximum wander compensation.

AXRA… Automatic Transmit Remote Alarm

0 ... Normal operation

1 ... The Remote Alarm bit will be automatically set in the outgoing data stream if the receiver is in asynchronous state (FRS0.LFA bit is set). In synchronous state the remote alarm bit will be reset. Additionally in multiframe format FMR2.RFS1=1 and FMR3.EXTIW =1 and the 400 msec timeout has elapsed, the remote alarm bit will be active in the outgoing data stream. In multiframe synchronous state the outgoing remote alarm bit is cleared.

ALMF… Automatic Loss of Multiframe

0 ... Normal operation

1 ... The receiver will search a new basic- and multiframing if more than 914 CRC errors have been detected in a time interval of one second. The internal 914 CRC error counter will be reset if the multiframe synchronization is found. Incrementing the counter is only enabled in the multiframe synchronous state.

Channel Loop Back (Read/Write)

Value after RESET: 00_H

	7				0	
LOOP			ECLB	CLA4	CLA0	(x1F)

ECLB… **Enable Channel Loop Back**

0 ... Disables the channel loop back.

1 ... Enables the channel loop back selected by this register.

CLA4…CLA0… **Channel Address For Loop Back**

CLA = 0…31 selects the channel.

During looped back the contents of the assigned outgoing channel on ports XL1/XDOP/XOID and XL2/XDON is equal to the idle channel code programmed at register IDLE.

Transmit Service Word Pulseframe (Read/Write)

Value after RESET: 00_H

	7							0	
XSW	XSIS	XTM	XRA	XY0	XY1	XY2	XY3	XY4	(x20)

XSIS… **Spare Bit For International Use**

First bit of the service word. Only significant in doubleframe format. If not used, this bit should be fixed to ‘1’. If one of the time-slot 0 transparent modes is enabled (bit XSP.TT0, or TSWM.TSIS), bit XSW.XSIS will be ignored.

XTM… **Transmit Transparent Mode**

0…Ports $\overline{\text{SYPX}}$ / XMFS define the frame / multiframe begin on the transmit system highway. The transmitter is usually synchronized on this externally sourced frame boundary and generates the FAS bits according to this framing. Any change of the transmit time-slot assignment will subsequently produce a change of the FAS bit positions.

1… Disconnects the control of the transmit system interface from the transmitter. The transmitter is now in a free running mode without any possibility to actualize the multiframe position. The framing (FAS bits) generated by the transmitter will not be „disturbed“ (in case of

changing the transmit time-slot assignment) by the transmit system highway unless register XC1 is written. Useful in loop-timed applications. For proper operation the transmit elastic buffer (2 frames, SIC1.XBS1/0= 10) has to be enabled.

XRA… Transmit Remote Alarm

0… Normal operation.

1… Sends remote alarm towards remote end by setting bit 3 of the service word. If time-slot 0 transparent mode is enabled via bit XSP.TT0 or TSWM.TRA bit is set, bit XSW.XRA will be ignored.

XY0…XY4… Spare Bits For National Use (Y-Bits, S_n-Bits, S_a-Bits)

These bits are inserted in the service word of every other pulseframe if S_a-bit register access is disabled (FMR1.ENSA = 0). If not used, they should be fixed to '1'.

If one of the time-slot 0 transparent modes is enabled (bit XSP.TT0 or TSWM.TSA4-8), bits XSW.XY0…4 will be ignored.

Transmit Spare Bits (Read/Write)

Value after RESET: 00_H

	7							0	
XSP		CASEN	TT0	EBP	AXS	XSIF	XS13	XS15	(x21)

CASEN… Channel Associated Signaling Enable

0… Normal operation.

1… A one in this bit position will cause the transmitter to send the CAS information stored in the XS1-16 registers in the corresponding time slots.

TT0… Time-Slot 0 Transparent Mode

0… Normal operation.

1… All information for time-slot 0 at port XDI will be inserted in the outgoing pulseframe. All internal information of the QuadFALC (framing, CRC, S_a/S_i bit signaling, remote alarm) will be ignored. This function is mainly useful for system test applications (test loops). Priority sequence of transparent modes: XSP.TTO > TSWM.

EBP… **E- Bit Polarity**

0… In the basic - or multiframe asynchronous state the E-bit will be set to zero.

1… In the basic - or multiframe asynchronous state the E-bit will be set to one.

If automatic transmission of sub-multiframe status is enabled by setting bit XSP.AXS and the receiver has been lost multiframe synchronization, the E bit with the programmed polarity will be inserted automatically in S_i-bit position of every outgoing CRC multiframe (under the condition that time-slot 0 transparent mode and transparent Si bit in Service word are both disabled).

AXS… **Automatic Transmission of Submultiframe Status**

Only applicable to CRC multiframe.

0… Normal operation.

1… Information of submultiframe status bits RSP.SI1 and RSP.SI2 will be automatically inserted in S_i -bit positions of the outgoing CRC multiframe (RSP.SI1 $\rightarrow$ S_i -bit of frame 13; RSP.SI2 $\rightarrow$ S_i-bit of frame 15). Contents of XSP.XS13 and XSP.XS15 will be ignored. If one of the time-slot 0 transparent modes XSP.TT0 or TSWM.TSIS is enabled, bit XSP.AXS has no function.

XSIF… **Transmit Spare Bit For International Use (FAS Word)**

First bit in the FAS word. Only significant in doubleframe format. If not used, this bit should be fixed to ‘1’. If one of the time-slot 0 transparent modes is enabled (bits XSP.TT0, or TSWM.TSIF), bit XSP.XSIF will be ignored.

XS13… **Transmit Spare Bit (Frame 13, CRC-Multiframe)**

First bit in the service word of frame 13 for international use. Only significant in CRC-multiframe format. If not used, this bit should be fixed to ‘1’. The information of XSP.XS13 will be shifted into internal transmission buffer with beginning of the next following transmitted CRC multiframe.

If automatic transmission of submultiframe status is enabled via bit XSP.AXS, or, if one of the time-slot 0 transparent modes XSP.TT0 or TSWM.TSIS is enabled, bit XSP.XS13 will be ignored.

XS15… **Transmit Spare Bit (Frame 15, CRC-Multiframe)**

First bit in the service word of frame 15 for international use. Only significant in CRC-multiframe format. If not used, this bit should be fixed to '1'. The information of XSP.XS15 will be shifted into internal transmission buffer with beginning of the next following transmitted CRC multiframe.

If automatic transmission of submultiframe status is enabled via bit XSP.AXS, or, if one of the time-slot 0 transparent modes XSP.TT0 or TSWM.TSIF is enabled, bit XSP.XS15 will be ignored.

Transmit Control 0 (Read/Write)

Value after RESET: 00_H

	7							0	
XC0	SA8E	SA7E	SA6E	SA5E	SA4E	XCO10	XCO9	XCO8	(x22)

SA8E…SA4E **SA Bit Signaling Enable**

0… Standard operation.

1… Setting this bit it will be possible to send / receive a LAPD protocol in any combination of the SA8- SA4 bit positions in the outgoing / incoming data stream. The on chip signaling controller has to be configured in the HDLC/LAPD mode. In transmit direction together with these bits the TSWM.TSA8-4 bits must be set to enable transmission to the remote end transparently through the FALC.

XCO10…XCO8… **Transmit Offset**

Initial value loaded into the transmit bit counter at the trigger edge of SCLKX when the synchronous pulse at port $\overline{\text{SYPX}}$ / XMFS is active Refer to register XC1.

Transmit Control 1 (Read/Write)

Value after RESET: $9C_H$

	7							0	
XC1	XCO7							XCO0	(x23)

A write access to this address resets the transmit elastic buffer to its basic starting position. Therefore, updating the value should only be done when the QuadFALC is initialized or when the buffer should be centered. As a consequence a transmit slip may occur.

XCO7…XCO0… Transmit Offset

Calculation of delay time T (SCLKX cycles) depends on the value X of the „Transmit Offset“ register XC1/0:

$0 \leq T \leq 3 + SC/SD$: $X = 3 + SC/SD - T$
$4 + SC/SD \leq T \leq$ max. delay : $X = 2051 - T + SC/SD$

Delay time T = time between beginning of time-slot 0 (bit 0 , channel phase 0) at XDI / XSIG and the initial edge of SCLKX after $\overline{SYPX}$ / XMFS goes active. See **figure 20 + 21.**

with max. delay = (256 * SC/SD) -1
with SC = System clock defined by SIC1.SSC1/0
with SD = system data rate

Receive Control 0 (Read/Write)

Value after RESET: 00_H

	7							0	
RC0	SWD	ASY4	CRCI	XCRCI	RDIS	RCO10	RCO9	RCO8	(x24)

SWD … Service Word Condition Disable

0… Standard operation. Three or four consecutive incorrect service words (depending on bit RC1.ASY4) will cause loss of synchronization.

1… Errors in service words have no influence when in synchronous state. However, they are used for the resynchronization procedure.

ASY4 … **Select Loss of Sync Condition**

0… Standard operation. Three consecutive incorrect FAS words or three consecutive incorrect service words will cause loss of synchronization.

1… Four consecutive incorrect FAS words or four consecutive incorrect service words will cause loss of synchronization. The service word condition may be disabled via bit RC1.SWD.

CRCI … **Automatic CRC4 Bit Inversion**

If set, all CRC bits of one outgoing submultiframe are inverted in case a CRC error is flagged for the previous received submultiframe. This function is logically ORed with RC0.XCRCI.

XCRCI… **Transmit CRC4 Bit Inversion**

If set, the CRC bits in the outgoing data stream are inverted before transmission. This function is logically ORed with RC0.CRCI.

RDIS… **Receive Data Input Sense**

0… Inputs: RDIP, RDIN active low, input ROID is active high

1… Inputs: RDIP, RDIN active high, input ROID is active low

RCO10…RCO8… Receive Offset / Receive Frame Marker Offset

Depending on the RP(A-D) pin function different offsets could be programmed. The $\overline{\text{SYPR}}$ and the RFM pin function could not be selected in parallel.

Receive Offset (PC(1-4).RPC(2-0) = 000)
Initial value loaded into the receive bit counter at the trigger edge of SCLKR when the synchronous pulse at port $\overline{\text{SYPR}}$ is active (see **figure)**.

Calculation of delay time T (SCLKR cycles) depends on the value X of the „Receive Offset“ register RC1/0. For programing refer to register RC1.

Receive Frame Marker Offset (PC(1-4).RPC(2-0) = 001)

Offset programming of the receive frame marker which is output on port $\overline{\text{SYPR}}$. The receive frame marker could be activated during any bit position of the current frame.

Calculation of the value X of the „Receive Offset“ register RC1/0 depends on the bit position BP which should be marked and SCLKR. Refer to register RC1.

Receive Control 1 (Read/Write)

Value after RESET: $9C_H$

	7		0	
RC1	RCO7		RCO0	(x25)

RCO7…RCO0… Receive Offset / Receive Frame Marker Offset

Depending on the RP(A-D) pin function different offsets could be programmed. The $\overline{\text{SYPR}}$ and the RFM pin function could not be selected in parallel.

Receive Offset (PC(1-4).RPC(2-0) = 000)
Initial value loaded into the receive bit counter at the trigger edge of SCLKR when the synchronous pulse at port $\overline{\text{SYPR}}$ is active (see **figure 17)**.

Calculation of delay time T (SCLKR cycles) depends on the value X of the „Receive Offset“ register RC1/0:

$0 \leq T \leq 4$: X= 4- T
$5 \leq T \leq$ max. delay : X= 2052 - T

with max. delay = (256*SC/SD) -1
with SC = System clock defined by SIC1.SSC1/0
with SD = 2.048 MHz
Delay time T = time between beginning of time-slot 0 at RDO and the initial edge of SCLKR after $\overline{\text{SYPR}}$ goes active.

Receive Frame Marker Offset (PC(1-4).RPC(2-0) = 001)

Offset programming of the receive frame marker which is output on multifunction port RFM. The receive frame marker could be activated during any bit position of the entire frame and depends on the selected system clock rate.
Calculation of the value X of the „Receive Offset“ register RC1/0 depends on the bit position BP which should be marked :

$0 \leq BP \leq 2045$: X = BP + 2
$2046 \leq BP \leq 2047$: X= BP - 2046)

e.g: 2.048 MBit/s: BP = 0-255; .... 16.384 MBit/s: BP = 0-2047

Transmit Pulse-Mask 0...2 (Read/Write)

Value after RESET: $7B_H$, 03_H, 00_H

	7							0	
XPM0	XP12	XP11	XP10	XP04	XP03	XP02	XP01	XP00	(x26)
XPM1	XP30	XP24	XP23	XP22	XP21	XP20	XP14	XP13	(x27)
XPM2	XLLP	XLT	DAXLT		XP34	XP33	XP32	XP31	(x28)

The transmit pulse shape which is defined in ITU-T G.703 will be output on pins XL1 and XL2. The level of the pulse shape can be programmed via registers XPM2-0 to create a custom waveform. In order to get an optimized pulse shape for the external transformers each pulse shape will be internally devided into four sub pulse shapes. In each sub pulse shape a programmed 5 bit value will define the level of the analog voltage on pins XL1/2. Together four 5 bit values have to be programmed to form one complete transmit pulse shape. The four 5 bit values will be sent in the following sequence:

XP04-00: First pulse shape level
XP14-10: Second pulse shape level
XP24-20: Third pulse shape level
XP34-30: Fourth pulse shape level

Changing the LSB of each subpulse in registers XPM2-0 will change the amplitude of the differential voltage on XL1/2 by approximately 80 mV.
Example: 120 Ω interface and wired as shown in **figure 22**.

XPM04-00: $1B_H$ or 27 decimal
XPM14-10: $1B_H$ or 27 decimal
XPM24-20: 00_H
XPM34-30: 00_H

Programming values for XPM0-2: $7B_H$, 03_H, 00_H

XLT… **Transmit Line Tri-state**

0… Normal operation

1… Transmit line XL1/XL2 or XDOP/XDON are switched into high impedance state. If this bit is set the transmit line monitor status information will be frozen.

DAXLT... **Disable Automatic Tristating of XL1/2**

0... Normal operation. If a short is detected on pins XL1/2 the transmit line monitor will set the XL1/2 outputs into a high impedance state.

1... If a short is detected on XL1/2 pins automatic setting these pins into a high impedance (by the XL-monitor) state will be disabled.

XLLP… Reserved

0… Normal operation

1… Reserved (not to be used)

Transparent Service Word Mask (Read/Write)

Value after RESET: 00_H

	7							0	
TSWM	TSIS	TSIF	TRA	TSA4	TSA5	TSA6	TSA7	TSA8	(x29)

TSWM7…TSWM0…Transparent Service Word Mask

TSIS… Transparent Si Bit in Service Word

0… The SI Bit will be generated internally.

1… The SI Bit in the service word will be taken from port XDI and transparently passed through the QuadFALC without any changes. The internal information of the QuadFALC (register XSW) will be ignored.

TSIF… Transparent Si Bit in FAS Word

0… The SI Bit will be generated internally.

1… The SI Bit in the FAS word will be taken from port XDI and routed transparently through the QuadFALC without any changes. The internal information of the QuadFALC (register XSW) will be ignored.

TRA… Transparent Remote Alarm

0… The Remote Alarm Bit will be generated internally.

1… The A Bit will be taken from port XDI and routed transparently through the QuadFALC without any changes. The internal information of the QuadFALC (register XSW) will be ignored.

TSA4…TSA8... Transparent SA4...8 Bit

0… The SA4-8 bit will be generated internally.

1… The SA4-8 bit will be taken from port XDI or from the internal signaling controller if enabled and transparently passed

through the QuadFALC without any changes. The internal information of the QuadFALC (registers XSW and XSA4-8) will be ignored.

Idle Channel Code Register (Read/Write)

Value after RESET: 00_H

	7							0	
IDLE	IDL7							IDL0	(x2B)

IDL7…IDL0… Idle Channel Code

If channel loop back is enabled by programming LOOP.ECLB=1, the contents of the assigned outgoing channel on ports XL1/XL2 resp. XDOP/XDON is set equal to the idle channel code selected by this register.

Additionally, the specified pattern overwrites the contents of all channels selected via the idle channel registers ICB1…ICB4. IDL7 will be transmitted first.

Transmit SA4-8 Register (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H, 00_H

	7							0	
XSA4	XS47	XS46	XS45	XS44	XS43	XS42	XS41	XS40	(x2C)
XSA5	XS57	XS56	XS55	XS54	XS53	XS52	XS51	XS50	(x2D)
XSA6	XS67	XS66	XS65	XS64	XS63	XS62	XS61	XS60	(x2E)
XSA7	XS77	XS76	XS75	XS74	XS73	XS72	XS71	XS70	(x2F)
XSA8	XS87	XS86	XS85	XS84	XS83	XS82	XS81	XS80	(x30)

XSA8…XSA4… Transmit S_a-Bit Data

The Sa-bit register access is enabled by setting bit FMR1.ENSA = 1. With the transmit multiframe begin an interrupt ISR1.XMB is generated and the contents of these registers XSA4-8 will be copied into a shadow register. The contents will subsequently sent out in the service words of the next outgoing CRC multiframe (or doubleframes) if none of the time-slot 0 transparent modes is enabled. XS40 will be sent out in bit position 4 in frame 1, XS47 in frame 15. The transmit

multiframe begin interrupt XMB request that these registers should be serviced. If requests for new information are ignored, current contents will be repeated.

Framer Mode Register 3 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR3			XLD	XLU	CMI	SA6SY		EXTIW	(x31)

XLD… **Transmit LLB Down Code**

0… Normal operation.

1… A one in this bit position will cause the transmitter to replace normal transmit data with the LLB Down (Deactuate) Code continuously until this bit is reset. The LLB Down Code will be optionally overwritten by the timeslot 0 depending on bit LCR1.LLBF.

XLU… **Transmit LLB UP Code**

0… Normal operation.

1… A one in this bit position will cause the transmitter to replace normal transmit data with the LLB UP Code continuously until this bit is reset. The LLB UP Code will be overwritten by the timeslot 0 depending on bit LCR1.LLBF. For proper operation bit FMR3.XLD must be cleared.

CMI… **Select CMI Precoding**

Only valid if CMI code (FMR0.XC1/0=01) is selected. This bit defines the CMI precoding and influences only the transmit data and not the receive data.

0… CMI with HDB3 precoding

1… CMI without HDB3 precoding

SA6SY… **Receive SA6 Access Synchron Mode**

Only valid if multiframe format (FMR2.RFS1/0=1x) is selected.

0… The detection of the predefined SA6 bit pattern (refer to chapter SA6 Bit Detection according to ETS 300233) is done independently of the multiframe synchronous state.

1… The detection of the SA6 bit pattern is done synchronously to the multiframe.

EXTIW… Extended CRC4 to Non CRC4 Interworking

Only valid in multiframe format. This bit selects the reaction of the synchronizer after the 400 msec timeout has been elapsed and starts transmitting a remote alarm if FMR2.AXRA is set.

0… The CRC4 to Non CRC4 interworking is done as described in ITU-T G. 706 Annex B.

1… The interworking is done according to ITU-T G. 706 with the exception that the synchronizer will still search the multiframing even if the 400 msec timer is expired. Switching into doubleframe format is disabled. If FMR2.AXRA is set the remote alarm bit will be active in the outgoing data stream until the multiframe is found.

Idle Channel Register (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H

	7							0	
ICB1	IC0	IC1	IC2	IC3	IC4	IC5	IC6	IC7	(x32)
ICB2	IC8	IC9	IC10	IC11	IC12	IC13	IC14	IC15	(x33)
ICB3	IC16	IC17	IC18	IC19	IC20	IC21	IC22	IC23	(x34)
ICB4	IC24	IC25	IC26	IC27	IC28	IC29	IC30	IC31	(x35)

IC0…IC31… Idle Channel Selection Bits

These bits define the channels (time-slots) of the outgoing PCM frame to be altered.
Assignments:
IC0 → time-slot 0
IC1 → time-slot 1

IC31 → time-slot 31

0… Normal operation.

1… Idle channel mode. The contents of the selected time-slot is overwritten by the idle channel code defined via register IDLE.

Note: Although time-slot 0 can be selected via bit IC0, its contents is only altered if the transparent mode is selected (XSP.TT0).

Line Interface Mode 0 (Read/Write)

Value after RESET: 00_H

	7							0	
LIM0	XFB	XDOS			EQON		LL	MAS	(x36)

XFB… Transmit Full Bauded Mode

Only applicable for dual rail mode (bit LIM1.DRS = 1).

0…Output signals XDOP/XDON are half bauded (normal operation).

1…Output signals XDOP/XDON are full bauded.

Note: If CMI coding is selected (FMR0.XC1/0=01) this bit has to be cleared.

XDOS… Transmit Data Out Sense

0… Output signals XDOP/XDON are active low. Output XOID is active high (normal operation).

1… Output signals XDOP/XDON are active high. Output XOID is active low.

Note: If CMI coding is selected (FMR0.XC1/0=01) this bit has to be cleared.
The transmit frame marker XFM is independent of this bit.

EQON… Receive Equalizer On

0… -10 dB Receiver: short haul mode

1… -34 dB Receiver, long haul mode

LL… Local Loop

0… Normal operation

1… Local loop active. The local loopback mode disconnects the receive lines RL1/RL2 resp. RDIP/RDIN from the receiver. Instead of the signals coming from the line the data provided by system interface are routed through the analog receiver back to the system interface. The unipolar bit stream will be undisturbed transmitted on the line. Receiver and transmitter coding must be identical. Operates in analog and digital line

interface mode. In analog line interface mode data is transfered through the complete analog receiver.

MAS… Master Mode

0… Slave mode

1 … Master mode on. Setting this bit the DCO-R circuitry is frequency synchronized to the clock (2.048 MHz) supplied by SYNC. If this pin is connected to VSS or VDD the DCO-R circuitry is centered and no receive jitter attenuation is performed. The generated clocks are stable.

Line Interface Mode 1 (Read/Write)

Value after RESET: 00_H

	7							0	
LIM1		RIL2	RIL1	RIL0		JATT	RL	DRS	(x37)

RIL2…RIL0… Receive Input Threshold

Only valid if analog line interface is selected (LIM1.DRS=0.

No signal will be declared if the voltage between pins RL1 and RL2 drops below the limits programmed via bits RIL2-0 and the received data stream has no transition for a period defined in the PCD register.

The threshold where no signal will be declared is programmable via the RIL2-0 bits depending of bit LIM0.EQON.

LIM0.EQON = 0 (short haul mode):

000 = 0.9 V
001 = 0.7 V
010 = 0.6 V
011 = 0.4 V
100 = 0.3 V
101 = 0.2 V
110 = 0.07 V
111 = 0.05 V

LIM0.EQON = 1 (long haul mode):

000 = 1.7 V
001 = 0.8 V
010 = 0.8 V
011 = 0.5 V
100 = 0.5 V
101 = 0.2 V

110 = 0.1 V
111 = not assigned

JATT…RL... Transmit Jitter Attenuator / Remote Loop

00 ... Normal operation. The transmit jitter attenuator is disabled. Transmit data will bypass the buffer.

01 ... Remote Loop active without transmit jitter attenuator enabled. Transmit data will bypass the buffer.

10 ... not defined

11 ... Remote Loop and jitter attenuator active. Received data from pins RL1/2 or RDIP/N or ROID will be sent jitter free on ports XL1/2 or XDOP/N or XOID. The dejittered clock is generated by the DCO-X circuitry.

DRS… Dual Rail Select

0 ... The ternary interface is selected. Multifunction ports RL1/2 and XL1/2 become analog in/outputs.

1 ... The digital dual rail interface is selected. Received data is latched on multifunction ports RDIP/RDIN while transmit data is output on pins XDOP/XDON.

Pulse Count Detection Register (Read/Write)

Value after RESET: 00_H

	7						0	
PCD	PCD7						PCD0	(x38)

PCD7…PCD0… Pulse Count Detection

A LOS alarm will be detected if the incoming data stream has no transitions for a programmable number T consecutive pulse positions. The number T is programmable via the PCD register and can be calculated as follows:
T= 16(N+1) ; with 0 =< N =< 255.

The maximum time is: 256 x 16 x 488 ns = 2 ms. Every detected pulse will reset the internal pulse counter. The counter will be clocked with the receive clock RCLK.

Pulse Count Recovery (Read/Write)

Value after RESET: 00_H

	7						0	
PCR	PCR7						PCR0	(x39)

PCR7…PCR0… Pulse Count Recovery

A LOS alarm will be cleared if a pulse density is detected in the received bit stream. The number of pulses M which must occur in the predefined PCD time interval is programmable via the PCR register and can be calculated as follows:

M = N+1 ; with 0 =< N =< 255.

The time interval starts with the first detected pulse transition. With every received pulse a counter will be incremented and the actual counter is compared with the contents of PCR register. If the pulse number >= the PCR value the LOS alarm will be reset otherwise the alarm will still be active. In this case the next detected pulse transition will start a new time interval.

Line Interface Mode 2 (Read/Write)

Value after RESET: 00_H

	7							0	
LIM2		LBO1			SCF	ELT			(x3A)

LBO1 … **Line Build-Out**

In long haul applications LIM0.EQON = 1 a transmit filter can be optionally placed on the transmit path to attenuate the data on pins XL1/2. To meet the line build-out defined by FTZ221 registers XPM2-0 should be programmed as follows:

0… 0 dB

1… FTZ221 template --> XPM2-0 = tbd.

SCF… **Select Corner Frequency of DCO-R**

Setting this bit will reduce the corner frequency of the DCO-R circuit by the factor of ten to 0.2 Hz.

Note: Reducing the corner frequency of the DCO-R circuitry will increase the synchronization time before the frequencies are synchronized.

ELT… **Enable Loop-Timed**

0… normal operation

1… Transmit clock is generated from the clock supplied by MCLK which is synchronized to the extracted receive route clock. In this configuration the transmit elastic buffer has to be enabled. Refer to register XSW.XTM. For correct operation of loop timed the remote loop (bit LIM1.RL = 0) must be inactive and bit CMR1.DXSS must be cleared.

Loop Code Register 1 (Read/Write)

Value after RESET: 00_H

	7							0	
LCR1	EPRM	XPRBS	LDC1	LDC0	LAC1	LAC0	FLLB	LLBP	(x3B)

EPRM… **Enable Pseudo Random Bit Sequence Monitor**

0… Pseudo random bit sequence (PRBS) monitor is disabled.

1… PRBS is enabled. Setting this bit enables incrementing the CEC2 error counter with each detected PRBS bit error. With any change of state of the PRBS internal synchronization status an interrupt ISR1.LLBSC is generated. The current status of the PRBS synchronizer is indicated by bit RSP.LLBAD.

XPRBS… Transmit Pseudo Random Bit Sequence

A one in this bit position enables transmitting of a pseudo random bit sequence to the remote end. Depending on pit LLBP the PRBS is generated according to 2^{15} -1 or 2^{20}-1 (ITU-T O. 151).

LDC1…0... Length Deactuate (Down) Code

These bits defines the length of the LLB deactuate code which is programmable in register LCR2.

00… length: 5 bit

01… length: 6 bit, 2 bit, 3 bit

10… length: 7 bit

11… length: 8 bit, 2 bit, 4bit

LAC1…0... Length Actuate (Up) Code

These bits defines the length of the LLB actuate code which is programmable in register LCR3.

00… length: 5 bit

01… length: 6 bit, 2 bit, 3 bit

10… length: 7 bit

11… length: 8 bit, 2 bit, 4 bit

FLLB… Framed Line Loopback / Invert PRBS

Depending on bit LCR1.XPRBS this bit enables different functions:

LCR1.XPRBS=0:

0… The line loopback code is transmitted including framing bits.

1… The line loopback code is transmitted unframed.

Invert PRBS

LCR1.XPRBS=1:

0… The generated PRBS is transmitted not inverted.

1… The PRBS is transmitted inverted.

LLBP… Line Loopback Pattern

LCR1.XPRBS=0

0… Fixed line loopback code : 001 or 00001.

1… Enable user programmable line loopback code via register LCR2/3.

LCR1.XPRBS=1 or LCR1.EPRM = 1

0… 2^{15} -1

1… 2^{20} -1

Loop Code Register 2 (Read/Write)

Value after RESET: 00_H

	7						0	
LCR2	LDC7						LDC0	(x3C)

LDC7…LDC0… Line Loopback Deactuate Code

If enabled by bit FMR3.XLD the LLB deactuate code will automatically repeat until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LDC0 is transmittted last. For correct operations bit LCR1.XPRBS has to cleared.

Loop Code Register 3 (Read/Write)

Value after RESET: 00_H

	7						0	
LCR3	LAC7						LAC0	(x3D)

LAC7…LAC0… Line Loopback Actuate Code

If enabled by bit FMR3.XLU the LLB actuate code will automatically repeat until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LAC0 is transmittted last. For correct operations bit LCR1.XPRBS has to cleared.

System Interface Control 1 (Read/Write)

Value after RESET: 00_H

	7							0	
SIC1	SSC1	SSD1	RBS1	RBS0	SSC0	BIM	XBS1	XBS0	(x3E)

SSC1...0… **Select System Clock**

SIC1.SSC1/0 define the clocking rate on the system highway.

00…2.048 MHz

01…4.096 MHz

10…8.192 MHz

11…16.384 MHz

SSD1 … **Select System Data Rate 1**

SIC1.SSD1 and FMR1.SSD0 define the data rate on the system highway. Programming SSD1/SSD0 and corresponding data rate is shown below.

00…2.048 MBit/s

01…4.096 MBit/s

10…8.192 MBit/s

11…16.384 MBit/s

RBS1...0… **Receive Buffer Size**

00… buffer size : 2 frames

01… buffer size : 1 frame

10… buffer size : 96 bits

11… By-pass of receive elastic store

BIM … **Bit Interleaved Mode**

0…byte interleaved mode

1…bit interleaved mode

XBS1...0… **Transmit Buffer Size**

00… By-pass of transmit elastic store

01… buffer size : 1 frame

10… buffer size : 2 frames

11… buffer size : 96 bits

System Interface Control 2 (Read/Write)

Value after RESET: 00_H

	7							0	
SIC2	FFS	SSF	CRB		SICS2	SICS1	SICS0		(x3F)

FFS … **Force Freeze Signaling**

Setting this bit disables updating of the receive signaling buffer and current signaling information is frozen. After resetting this bit and receiving a complete superframe updating of the signaling buffer is started again. The freeze signaling status could be also automatically generated by detecting the Loss of Signal alarm or a Loss of CAS Frame Alignment or a receive slip (only if external register access via RSIG is enabled). This automatic freeze signaling function is logically ored with this bit.
The current internal freeze signaling status is output on pin RP(A-D) / pin function FREEZ which is selected by PC(1-4).RPC(2-0) = 110. Additionally this status is also available in register SIS.SFS.

SSF … **Serial Signaling Format**

Only applicable if pin function R/XSIG is selected.

0… Bits 1-4 in all time-slots except time-slots 0 +16 are cleared.

1… Bits 1-4 in all time-slots except time-slots 0 +16 are set high.

CRB … **Center Receive Elastic Buffer**

Only applicable if the time-slot assigner is disabled (PC1-4.RPC2-0 = 001) , no external or internal synchronous pulse receive is generated.
A transition from low to high will force a receive slip and the read-pointer of the receive elastic buffer is centered. The delay through the buffer is set to one half of the current buffer size. It should be hold high for at least two 2.048 MHz periods before it is cleared.

SICS2 …0 **System Interface Channel Select**

Only applicable if the system clock rate is greater than 2.048 MHz .

Received data is transmitted on pin RDO / RSIG or received on XDI / XSIG with the selected system data rate. If the data rate is greater than 2.048 MBit/s the data is output or sampled in half , a quarter or a 1/8 of the 125 µsec. They will not be repeated. The time where the data is active during a 488 nsec time-slot is called in the following a channel phase. RDO / RSIG are cleared while XDI / XSIG are

ignored for the remaining time of the 488 nsec or for the remaining channel phases. The channel phases are selectable with these bits.

000 …data active in channel phase 1, valid if system data rate is 16 / 8 / 4 MBit/s

001 …data active in channel phase 2, valid if system data rate is 16 / 8 / 4 MBit/s

010 …data active in channel phase 3, valid if data rate is 16 / 8 MBit/s

011 …data active in channel phase 4, valid if data rate is 16 / 8 MBit/s

100 …data active in channel phase 5 , valid if data rate is 16 MBit/s

101 …data active in channel phase 6 , valid if data rate is 16 MBit/s

110 …data active in channel phase 7, valid if data rate is 16 MBit/s

111 …data active in channel phase 8 , valid if data rate is 16 MBit/s

System Interface Control 3 (Read/Write)

Value after RESET: 00_H

	7							0	
SIC3	CASMF				RESX	RESR	TTRF	DAF	(x40)

CASMF… CAS Multiframe Begin Marker

0…The time-slot 0 multiframe begin is asserted on pin RP(A-D) / pin function RMFB.

1…The time-slot 16 CAS multiframe begin is asserted on pin RP(A-D) / pin function RMFB.

RESX… Rising Edge Synchronous Pulse Transmit

Depending on this bit all transmit system interface data and marker are clocked off or sampled with the selected active edge.

0… $\overline{\text{SYPX}}$ is latched with the first falling (active) edge of the SCLKX clock.

1… $\overline{\text{SYPX}}$ is latched with the first rising (active) edge of the SCLKX clock.

The $\overline{\text{SYPX}}$ pin function is selected by PC(1-4).XC(2-0) = 0000.

RESR… Rising Edge Synchronous Pulse Receive

Depending on this bit all receive system interface data and marker are clocked off with the selected active edge.

0… $\overline{\text{SYPR}}$ is latched with the first falling edge of the SCLKR clock.

1… $\overline{\text{SYPR}}$ is latched with the first rising edge of the SCLKR clock.

The $\overline{\text{SYPR}}$ pin function is selected by PC(1-4).RPC(2-0) = 000.

TTRF… TTR Register Function

Setting this bit the function of the TTR1-4 registers are changed. A one in each TTR register will force the XSIGM marker high for the respective time-slot and controls sampling of the time-slots provided on pin XSIG. XSIG is selected by PC(1-4).XPC(2-0).

DAF… Disable Automatic Freeze

0… Signaling is automaticly frozen if one of the following alarms occured: Loss of Signal (FRS0.LOS), Loss of CAS Frame Alignment (FRS1.TS16LFA) , or receive slips (ISR3.RSP/N).

1… Automatic freezing of signaling data is disabled. Updating of the signaling buffer is also done if one of the above described alarm conditions is active. However, updating of the signaling buffer is stopped if SIC2.FFS is set. Significant only if the serial signaling access is enabled.

Clock Mode Register 1 (Read/Write)

Value after RESET: 00_H

	7							0	
CMR1	DRSS1	DRSS0	RS1	RS0	DCS	STF	DXJA	DXSS	(x44)

DRSS1 ... 0 … DCO-R Synchronization Clock Source

These bits select the reference clock source for the DCO-R circuitry.

00… receive reference clock generated by the DPLL of channel 1

01… receive reference clock generated by the DPLL of channel 2

10… receive reference clock generated by the DPLL of channel 3

11… receive reference clock generated by the DPLL of channel 4

Note: After Reset all DCO-R circuitries will synchronize on the clock sourced by the DPLL of channel 1 . Each channel have to be configured individually.
If LIM0.MAS is set the DCO-R circuitry will synchronize on the clock applied to port SYNC.

RS1 ... 0 … **Select RCLK Source**

These bits select the source of RCLK.

00… extracted receive clock, generated by the DPLL

01… extracted receive clock with the option in case of an active LOS alarm this pin is set high.

10… dejittered 2.048 MHz clock generated by the internal DCO-R circuitry.

11… dejittered 8.192 MHz clock generated by the internal DCO-R circuitry.

DCS … **Disable Clock Switching**

In Slave mode (LIM0.MAS = 0) the DCO-R is synchronized on the recovered route clock. In case of loss of signal LOS the DCO-R switches automatically to the clock sourced by port SYNC. Setting this bit automatic switching from RCLK to SYNC is disabled.

STF … **Select TCLK Frequency**

Only applicable if the pin function TCLK port XP(A-D) is selected by PC(1-4).XPC(2-0) = 011. Data on XL1/2 (XDOP/N / XOID) are clocked off with TCLK.

0… 2.048 MHz

1… 8.192 MHz

DXJA… **Disable Internal Transmit Jitter Attenuation**

Setting this bit disables the transmit jitter attenuation. Reading the data out of the transmit elastic buffer and transmitting on XL1/2 (XDOP/N / XOID) is done with the clock provided on pin TCLK. In transmit elastic buffer bypass mode the transmit clock is taken from SCLKX, independent of this bit.

DXSS … **DCO-X Synchronization Clock Source**

0… The DCO-X circuitry of each channel will synchronize to the internal reference clock which is sourced by SCLKX/R or RCLK. Since there are many reference clock opportunities the following internal priorization in descenting order from left to right is realized: LIM1.RL > CMR2.DXSS > LIM2.ELT > current working clock of transmit system interface.
If one of these bits is set the corresponding reference clock is taken.

1… DCO-X synchronizes to an external reference clock provided by pin XP(A-D) pin function TCLK, if no remote loop is active. TCLK is selected by PC(1-4).XPC(2-0) = 011.

Clock Mode Register 2 (Read/Write)

Value after RESET: 00_H

	7							0	
CMR2				DCF	IRSP	IRSC	IXSP	IXSC	(x45)

DCF … DCO-R Center- Frequency Disabled

0… The DCO-R circuitry may be frequency centered
- in master mode if no reference clock on pin SYNC is provided or
- in slave mode if a loss of signal occurs in combination with no clock on pin SYNC or
- a gapped clock is provided at pin RCLKI and this clock is inactive or stopped.

1… The center function of the DCO-R circuitry is disabled. The generated clock (DCO-R) is frequency frozen in that moment when no clock is available at pin SYNC or pin RCLKI. The DCO-R circuitry will starts synchronization as soon as a clock at pins SYNC or RCLKI appears.

IRSP … Internal Receive System Frame Sync Pulse

0… The frame sync pulse for the receive system interface is sourced by $\overline{\text{SYPR}}$.

1… The frame sync pulse for the receive system interface is internally sourced by the DCO-R circuitry of each channel. This internally generated frame sync could be output active low on pin RP(A-D). RPC(2-0) = 001. Programming the receive time-slot offset is also done in the same way as it is done for the external $\overline{\text{SYPR}}$. For correct operation bit IRSC must be set. $\overline{\text{SYPR}}$ is ignored.

IRSC … Internal Receive System Clock

Only applicable if bit GPC1.SMM is cleared. If GPC1.SMM is set SCLKR1 of channel 1 provides the working clock for all four channels.

0… The working clock for the receive system interface is sourced by SCLKR of each channel or in receive elastic buffer bypass mode from the corresponding extracted receive clock RCLK.

1… The working clock for the receive system interface is sourced internally by DCO-R or in bypass mode by the extracted receive clock of each channel. SCLKR is ignored.

IXSP … Internal Transmit System Frame Sync Pulse

0… The frame sync pulse for the transmit system interface is sourced by $\overline{\text{SYPX}}$.

1… The frame sync pulse for the transmit system interface is internally sourced by the DCO-R circuitry of each channel. Additionally, the external XMFS signal defines the transmit multiframe begin. XMFS is enabled or disabled via the multifunction ports. For correct operation bits CMR2.IXSC / IRSC must be set. $\overline{\text{SYPX}}$ is ignored.

IXSC … Internal Transmit System Clock

Only applicable if bit GPC1.SMM is cleared. If GPC1.SMM is set SCLKX1 of channel 1 provides the working clock for all four channels.

0… The working clock for the transmit system interface is sourced by SCLKX of each channel.

1… The working clock for the transmit system interface is sourced internally by the working clock of the receive system interface. SCLKX is ignored.

Global Configuration Register (Read/Write)

Value after RESET: 00_H

	7							0	
GCR	VIS	SCI	SES	ECMC				PD	(x46)

VIS… Masked Interrupts Visible

0… Masked interrupt status bits are not visible in registers ISR0-4.

1… Masked interrupt status bits are visible in ISR0-4, but they are not visible in registers GIS and CIS.

SCI… Status Change Interrupt

0… Interrupts will be generated either on coming or going of the internal interrupt source.

1… The following interrupts will be activated if enabled with detecting and recovering of the internal interrupt source: ISR2.LOS , ISR2.AIS, ISR3.LMFA16

SES… Select External Second Timer

0… internal second timer selected

1… external second timer selected

ECMC… Error Counter Mode COFA

0… The SA6 bit error indications are accumulated in the error counter CEC3L/H.

1… A Change of Frame or Multiframe Alignment COFA is detected since the last re-synchronization. The events are accumulated in the error counter CEC3L.1-0.
Multiframe periods received in the asynchronous state are accumulated in the error counter CEC3L.7-2.
An overflow of each counter is disabled.

PD… Power Down

Switches the appropriate single FALC(1-4) between power up and power down mode.

0… Power Up

1… Power Down
All outputs are driven inactive, except the multifunction ports, which are driven high.

Errored Second Mask (Read/Write)

Value after RESET: FF_H

	7							0	
ESM	LFA	FER	CER	AIS	LOS	CVE	SLIP	EBE	(x47)

ESM Errored Second Mask

This register functions as an additional mask register for the interrupt status bit Errored Second (ISR3.ES). A ‘1’ in a bit position of ESM sets the mask active for the interrupt status.

Disable Error Counter (Write)

Value after RESET: 00_H

	7							0	
DEC	DRBD		DCEC3	DCEC2	DCEC1	DEBC	DCVC	DFEC	(x60)

DRBD **Disable Receive Buffer Delay**

This bit has to be set before reading the register RBD. It will be automatically reset if RBD has been read.

DCEC3… **Disable CRC Error Counter 3**

DCEC2… **Disable CRC Error Counter 2**

DCEC1… **Disable CRC Error Counter**

DEBC … **Disable Errored Block Counter**

DCVC… **Disable Code Violation Counter**

DFEC… **Disable Framing Error Counter**

These bits are only valid if FMR1.ECM is cleared. They have to be set before reading the error counters. They will be automatically reset if the corresponding error counter high byte has been read. With the rising edge of these bits the error counters are latched and then cleared.

Transmit CAS Register (Write)

Value after RESET: not defined

	7							0	
XS1	0	0	0	0	X	Y	X	X	(x70)
XS2	A1	B1	C1	D1	A16	B16	C16	D16	(x71)
XS3	A2	B2	C2	D2	A17	B17	C17	D17	(x72)
XS4	A3	B3	C3	D3	A18	B18	C18	D18	(x73)
XS5	A4	B4	C4	D4	A19	B19	C19	D19	(x74)
XS6	A5	B5	C5	D5	A20	B20	C20	D20	(x75)
XS7	A6	B6	C6	D6	A21	B21	C21	D21	(x76)
XS8	A7	B7	C7	D7	A22	B22	C22	D22	(x77)
XS9	A8	B8	C8	D8	A23	B23	C23	D23	(x78)
XS10	A9	B9	C9	D9	A24	B24	C24	D24	(x79)
XS11	A10	B10	C10	D10	A25	B25	C25	D25	(x7A)
XS12	A11	B11	C11	D11	A26	B26	C26	D26	(x7B)
XS13	A12	B12	C12	D12	A27	B27	C27	D27	(x7C)
XS14	A13	B13	C13	D13	A28	B28	C28	D28	(x7D)
XS15	A14	B14	C14	D14	A29	B29	C29	D29	(x7E)
XS16	A15	B15	C15	D15	A30	B30	C30	D30	(x7F)

Transmit CAS Register 1-16

The transmit CAS register access is enabled by setting bit XSP.CASEN = 1. Each register except XS1 contains the CAS bits for two timeslots. With the transmit multiframe begin ISR1.XMB the contents of these registers will be copied into a shadow register. The contents will subsequently sent out in the timeslots 16 of the outgoing data stream. If ISR1.XMB is not used and the write access to these registers is done exact in that moment when this interrupt is generated, data may be lost.

XS1.7 will be sent out first and XS16.0 will be sent last. The transmit multiframe begin interrupt (XMB) requests that these registers should be serviced. If requests for new information are ignored, current contents will be repeated. XS1 has to be programmed with the multiframe pattern. This pattern should always stay low otherwise the remote end will lose its synchronization. With setting the Y-bit a remote alarm will be transmitted to the far end. The X bits (Spare bits) should be set to one if they are not used.
If access to these registers is done without control of the interrupt ISR1.XMB the registers should be write twice to avoid a internally data transfer error.

Note: A software reset (CMDR.XRES) will reset these registers.

Port Configuration 1-4 (Read/Write)

Value after RESET: 00_H

	7							0	
PC1		RPC2	RPC1	RPC0		XPC2	XPC1	XPC0	(x80)
PC2		RPC2	RPC1	RPC0		XPC2	XPC1	XPC0	(x81)
PC3		RPC2	RPC1	RPC0		XPC2	XPC1	XPC0	(x82)
PC4		RPC2	RPC1	RPC0		XPC2	XPC1	XPC0	(x83)

RPC2 ...0… Receive multifunction port configuration

The multifunction ports RP(A-D) are bidirectional. After Reset these ports are configured as inputs. With the selection of the pin function the In/Output configuration is also achieved. The input function $\overline{\text{SYPR}}$ may only be selected once, it should not be selected twice or more. Register PC1 configures port RPA,while PC2 --> port RPB,
PC3 --> port RPC and PC4 --> port RPD.

000…$\overline{\text{SYPR}}$: Synchronous Pulse Receive (Input)
Together with register RC1/0 $\overline{\text{SYPR}}$ defines the frame begin on the receive system interface. Because of the offset programming the $\overline{\text{SYPR}}$ and the RFM pin function could not be selected in parallel.

001…RFM : Receive Frame Sync (Output)
CMR2.IRSP = 0: This receive frame marker could be active high for a 2.048 MHz period during any bit position of the current frame. Programming is done with registers RC1/0. The internal time-slot assigner is disabled.
CMR2.IRSP = 1: Internal generated frame synchronization pulse generated by the DCO-R circuitry. Together with registers RC1/0 the frame begin on the receive system interface is defined. This frame synchronization pulse is active low 2.048 MHz period.

010…RMFB : Receive Multiframe Begin (Output)
Marks the beginning of every received multiframe or optionally the begin of every CAS multiframe begin (active high).

011…RSIGM : Receive Signaling Marker (Output)
Marks the time-slots which are defined by register RTR1-4 of every frame at port RDO.

100…RSIG : Receive Signaling Data (Output)
The received CAS multiframe is transmitted on this pin. Time-slots on RSIG correlates directly to the time-slot assignment on RDO. In system interface multiplex mode all four received signaling data streams are merged into a single rail data stream byte or bit interleaved on RSIG1.

101…DLR : Data Link Bit Receive (Output)
Marks the SA8-4 bits within the data stream on RDO.

110…FREEZ : Freeze Signaling (Output)
The freeze signaling status is active high by detecting a Loss of Signal alarm, or a Loss of CAS Frame Alignment or a receive slip (pos. or neg.). It will hold high for at least one complete multiframe after the alarm disappears. Setting SIC2.FFS enforces a high on pin FREEZ.

111…$\overline{\text{RFSP}}$: Receive Frame Synchronous Pulse (Output)
Marks the frame begin in the receivers synchrounous state. This marker is active low for 488 ns with a frequency of 8 kHz.

XPC2 ...0… Transmit multifunction Port Configuration

The multifunction ports XP(A-D) are bidirectional. After Reset these ports are configured as inputs. With the selection of the pin function the In/Output configuration is also achieved. Each of the four different input functions ($\overline{\text{SYPX}}$, XMFS, XSIG, TCLK) may only be selected once. No input function should be selected twice or more. $\overline{\text{SYPX}}$ and XMFS should not be selected in parallel. Register PC1 configures port XPA,while PC2 --> port XPB, PC3 --> port XPC and PC4 --> port XPD.

000…$\overline{\text{SYPX}}$: Synchronous Pulse Transmit (Input)
Together with register XC1/0 $\overline{\text{SYPX}}$ defines the frame begin on the transmit system interface ports XDI and XSIG.

001…XMFS : Transmit Multiframe Synchronization (Input)
Together with register XC1/0 XMFS defines the frame and multiframe begin on the transmit system interface ports XDI and XSIG. Depending on PC5.CXMFS the signal on XMFS is active high or low.

010…XSIG : Transmit Signaling Data (Input)
Input for transmit signaling data received from the signaling highway. In system interface multiplex mode latching of the data stream containing the 4 signaling multiframes is done byte or bit interleaved on port XDI1. Optionally sampling of XSIG data is controlled by the active high XSIGM marker.

011…TCLK : Transmit Clock (Input)
A 2.048 / 8.192 MHz clock has to be sourced by the system if the internal generated transmit clock (DCO-X) should not be used. Optionally this input functions as a synchronization clock for the DCO-X circuitry with a frequencyof 2.048 MHz.

100…XMFB : Transmit Multiframe Begin (Output)
Marks the beginning of every transmit multiframe.

101…XSIGM : Transmit Signaling Marker (Output)
Marks the time-slots which are defined by register TTR1-4 of every frame at port XDI.

110…DLX : Data Link Bit Transmit (Output)
Marks the SA8-4 bits within the data stream on XDI.

111…XCLK : Transmit Line Clock (Output)
Frequency: 2.048 MHz

Port Configuration 5 (Read/Write)

Value after RESET: 00_H

	7							0	
PC5					CXMFS	CSXP	CSRP	CRP	(x84)

CXMFS … Configure XMFS Port

0… Port XMFS is active low.

1… Port XMFS is active high.

CSXP … Configure SCLKX Port

0… SCLKX : Input

1… SCLKX : Output

CSRP … Configure SCLKR Port

0… SCLKR : Input

1… SCLKR : Output

CRP … Configure RCLK Port

0… RCLK : Input

1… RCLK : Output

Global Port Configuration 1 (Read/Write)

Value after RESET: 00_H

	7							0	
GPC1	SMM	CSFP1	CSFP0		FSS1	FSS0	R1S1	R1S0	(85)

SMM … **System Interface Multiplex Mode**

Setting this bit enables a single rail data stream of 16.384 or 8.192 MBit/s containg all four E1 frames. The receive system interface for all four channels is running with the clock provided on SCLKR1 and the frame sync pulse provided on $\overline{\text{SYPR1}}$. The transmit system interface is running with SCLKX1 and $\overline{\text{SYPX1}}$. Data will be transmitted / accepted in a byte or bit interleaved format. In the system interface multiplex mode the following pin configuration has to be fulfilled and must be identically for all for 4 channels:

- $\overline{\text{SYPR1}}$ has to be provided on pin RPA1
- $\overline{\text{SYPX1}}$ has to be provided on pin XPA1 or
- XMFS has to be provided on pin XPB1
- XSIG has to be provided on pin XPC1
- RSIG will be output on pin RPB1

Each of the four channels have to be configured equally:

- clocking rate : 16.384 or 8.192 MHz , SIC1.SSC1/0
- data rate : 16.384 or 8.192 MBit/s, SIC1.SSD, FMR1.SSD0
- time-slot offset programming : RC1/0 , XC1/0
- receive buffer size : SIC1.RBS1/0 = 00 (2 frames)

e.g. : system clock rate = 8.192 MHz : SIC1.SSC1/0 = 10 and system data rate = 8.192 MBit/s : SIC1.SSD1 = 1 , FMR1.SSD0 = 0
The multiplexed data stream is internal logically ored. Therefore the selection of the active channel phase have to be configured different for each single channel FALC(1-4). Programming is done with SIC2.SICS2-0.
for FALC1: SIC2.SICS2-0 = 000, selects the first channel phase
for FALC2: SIC2.SICS2-0 = 001, selects the second channel phase
for FALC3: SIC2.SICS2-0 = 010, selects the third channel phase
for FALC4: SIC2.SICS2-0 = 011, selects the fourth channel phase

byte interleaved data format: SIC1.BIM = 0

XDI/RDO: F1-TS0, F2-TS0, F3-TS0, F4-TS0, F1-TS1, ... F4-TS31

X/RSIG: F1-STS0, F2-STS0, F3-STS0, F4-STS0, F1-... F4-STS31

or : bit interleaved data format: SIC1.BIM = 1

XDI/RDO: F1-TS0-B1, F2-TS0-B1, F3-TS0-B1, F4-TS0-B1, F1-TS0-B2, ... F4-TS31-B8

X/RSIG: F1-STS0-B1, F2-STS0-B1, F3-STS0-B1, F4-STS0-B1, F1-STS0-B2, ... F4-STS31-B8

with : F = Framer, TS = Time-Slot, STS = Signaling Time-Slot, B = Bit

In system interface multiplex mode signals on RDO2-4 and RSIG2-4 are undefined, while signals on SCLKR2-4, $\overline{\text{SYPR}}$2-4, SCLKX2-4, $\overline{\text{SYPX}}$2-4, XDI2-4 and XSIG2-4 are ignored.

CSFP1 ... 0 … **Configure SEC / FSC Port**

The FSC pulse is generated if the DCO-R circuitry of the selected channel is active (CMR2.IRSC = 1 or CMR1.RS1/0 = 10 or 11).

00 … SEC : Input , active high

01 … SEC : Output, active high

10 … FSC: Output , active high

11 … FSC: Output, active low

FSS1 ... 0 … **SEC / FSC Source**

One of the four internal generated dejittered 8 kHz clocks or second timers (SEC) are output on port SEC / FSC.

GPC1.CSFP1 = 1:

00 … FSC : 8 kHz sourced by channel 1

01 … FSC : 8 kHz sourced by channel 2

10 … FSC : 8 kHz sourced by channel 3

11 … FSC : 8 kHz sourced by channel 4

GPC1.CSFP1 = 0:

00 … SEC : second timer sourced by channel 1

01 … SEC: second timer sourced by channel 2

10 … SEC: second timer sourced by channel 3

11 … SEC: second timer sourced by channel 4

R1S1 ... 0 … **RCLK1 Source**

One of the four internal generated receive route clocks are output on port RCLK1. Outputs RCLK2-4 are valid independent of these bits.

Refer to bit CMR1.RS1/0.

00 … extracted receive clock of channel 1

01 … extracted receive clock of channel 2

10… extracted receive clock of channel 3

11… extracted receive clock of channel 4

4.5 Status Register Description

Table 12
Status RegisterAddress Arrangement

Address				Register	Type	Comment
00	100	200	300	RFIFO	R	Receive FIFO
49	149	249	349	RBD	R	Receive Buffer Delay
4A				VSTR	R	Version Status
4B	14B	24B	34B	RES	R	Receive Equalizer Status
4C	14C	24C	34C	FRS0	R	Framer Receive Status 0
4D	14D	24D	34D	FRS1	R	Framer Receive Status 1
4E	14E	24E	34E	RSW	R	Receive Service Word
4F	14F	24F	34F	RSP	R	Receive Spare Bits
50	150	250	350	FECL	R	Framing Error Counter Low
51	151	251	351	FECH	R	Framing Error Counter High
52	152	252	352	CVCL	R	Code Violation Counter Low
53	153	253	353	CVCH	R	Code Violation Counter High
54	154	254	354	CEC1L	R	CRC Error Counter 1 Low
55	155	255	355	CEC1H	R	CRC Error Counter 1 High
56	156	256	356	EBCL	R	E-Bit Error Counter Low
57	157	257	357	EBCH	R	E-Bit Error Counter High
58	158	258	358	CEC2L	R	CRC Error Counter 2 Low
59	159	259	359	CEC2H	R	CRC Error Counter 2 High
5A	15A	25A	35A	CEC3L	R	CRC Error Counter 3 Low
5B	15B	25B	35B	CEC3H	R	CRC Error Counter 3 High
5C	15C	25C	35C	RSA4	R	Receive SA4 Bit Register
5D	15D	25D	35D	RSA5	R	Receive SA5 Bit Register
5E	15E	25E	35E	RSA6	R	Receive SA6 Bit Register
5F	15F	25F	35F	RSA7	R	Receive SA7 Bit Register
60	160	260	360	RSA8	R	Receive SA8 Bit Register
61	161	261	361	RSA6S	R	Receive SA6 Bit Status Register
62	162	262	362	RSP1	R/W	Receive Signaling Pointer 1
63	163	263	363	RSP2	R/W	Receive Signaling Pointer 2

Table 12
Status RegisterAddress Arrangement

64	164	264	364	SIS	R	Signaling Status Register
65	165	265	365	RSIS	R	Receive Signaling Status Register
66	166	266	366	RBCL	R	Receive Byte Control Low
67	167	267	367	RBCH	R	Receive Byte Control High
68	168	268	368	ISR0	R	Interrupt Status Register 0
69	169	269	369	ISR1	R	Interrupt Status Register 1
6A	16A	26A	36A	ISR2	R	Interrupt Status Register 2
6B	16B	26B	36B	ISR3	R	Interrupt Status Register 3
6C	16C	26C	36C	ISR4	R	Interrupt Status Register 4
6D	16D	26D	36D			
6E	16E	26E	36E	GIS	R	Global Interrupt Status
6F				CIS	R	Channel Interrupt Status
70	170	270	370	RS1	R	Receive CAS Register 1
71	171	271	371	RS2	R	Receive CAS Register 2
72	172	272	372	RS3	R	Receive CAS Register 3
73	173	273	373	RS4	R	Receive CAS Register 4
74	174	274	374	RS5	R	Receive CAS Register 5
75	175	275	375	RS6	R	Receive CAS Register 6
76	176	276	376	RS7	R	Receive CAS Register 7
77	177	277	377	RS8	R	Receive CAS Register 8
78	178	278	378	RS9	R	Receive CAS Register 9
79	179	279	379	RS10	R	Receive CAS Register 10
7A	17A	27A	37A	RS11	R	Receive CAS Register 11
7B	17B	27B	37B	RS12	R	Receive CAS Register 12
7C	17C	27C	37C	RS13	R	Receive CAS Register 13
7D	17D	27D	37D	RS14	R	Receive CAS Register 14
7E	17E	27E	37E	RS15	R	Receive CAS Register 15
7F	17F	27F	37F	RS16	R	Receive CAS Register 16

Receive FIFO (Read) RFIFO

	7							0	
RFIFO	RF7							RF0	(x00/x01)

Reading data from RFIFO can be done in an 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. The LSB is received first from the serial interface.

The size of the accessible part of RFIFO is determined by programming the bits CCR1.RFT 1 … 0 (RFIFO threshold level). It can be reduced from 32 bytes (RESET value) down to 2 bytes (four values: 32, 16, 4, 2 bytes).

Data Transfer

Up to 32 bytes/16 words of received data can be read from the RFIFO following an RPF or an RME interrupt.
RPF Interrupt: A fixed number of bytes/words to be read (32, 16, 4, 2 bytes). The message is not yet complete.

RME Interrupt: The message is completely received. The number of valid bytes is determined by reading the RBCL, RBCH registers.

RFIFO is released by issuing the “Receive Message Complete” command (RMC).

Receive Buffer Delay (Read)

	7							0	
RBD			RBD5	RBD4	RBD3	RBD2	RBD1	RBD0	(x49)

RBD5…RBD0... Receive Elastic Buffer Delay

These bits informs the user about the current delay (in time-slots) through the receive elastic buffer. The delay is updated every 512 or 256 bits (SIC1.RBS1/0). Before reding this register the user has to set bit DEC.DRBD in order to halt the current value of this register. After reading RBD updating of this register is enabled. Not valid if the receive buffer is bypassed.

000000 = delay < 1 time-slot

:
:

111111 = delay >63 time-slots

Version Status Register (Read)

	7							0	
VSTR	VN7							VN0	(4A)

VN7 – VN0… **Version Number of Chip**

00_H…Version 1.1

Receive Equalizer Status (Read)

	7							0	
RES	EV1	EV0		RES4	RES3	RES2	RES1	RES0	(x4B)

EV1…EV0... **Equalizer Status Valid**

These bits informs the user about the current state of the receive equalization network. Only valid if LIM1.EQON is set.

00… equalizer status not valid, still adapting

01… equalizer status valid

10… equalizer status not valid

11… equalizer status valid but high noise floor

RES4…RES0... **Receive Equalizer Status**

The current line attenuation status in steps of nearly 1.7 dB are displayed in these bits. Only valid if bits EV1/0 = 01. Accuracy: +/- 2 digit, based on temperature influence and noise amplitude variations.

00000… attenuation: 0 dB

...

11001… max. attenuation: -34 dB

Framer Receive Status Register 0 (Read)

	7							0	
FRS0	LOS	AIS	LFA	RRA		NMF	LMFA		(x4C)

LOS… **Loss of Signal**

Detection:
This bit is set when the incoming signal has “no transitions” (analog

interface) or logical zeros (dig. interface) in a time interval of T consecutive pulses, where T is programmable via PCD register.
Total account of consecutive pulses: 16 < T < 4096.

Analog interface: The receive signal level where “no transition” will be declared is defined by the programmed value of LIM1.RIL2-0.

Recovery:
Analog interface: The bit will be reset in short haul mode when the incoming signal has transitions with signal levels greater than the programmed receive input level (LIM1.RIL2-0) for at least M pulse periods defined by register PCR in the PCD time interval. In long haul mode addtionally bit RES.6 must be set for at least 250µsec.
Digital interface: The bit will be reset when the incoming data stream contains at least M ones defined by register PCR in the PCD time interval.

With the rising edge of this bit an interrupt status bit (ISR2.LOS) will be set..
The bit will also be set during alarm simulation and reset if FMR0.SIM is cleared and no alarm condition exists.

AIS… **Alarm Indication Signal**

The function of this bit is determined by FMR0.ALM.

FMR0.ALM = 0: This bit is set when two or less zeros in the received bit stream are detected in a time interval of 250 µs and the QuadFALC is in the asynchronous state (FRS0.LFA = 1). The bit will be reset when no alarm condition is detected (ETSI).

FMR0.ALM = 1: This bit is set when the incoming signal has two or less Zeros in each of two consecutive double frame period (512 bits). This bit will be cleared when each of two consecutive doubleframe periods contain three or more zeros or when the frame alignment signal FAS has been found. (ITU-T: G.775)

The bit will also be set during alarm simulation and reset if FMR0.SIM is cleared and no alarm condition exists.

With the rising edge of this bit an interrupt status bit (ISR2.AIS) will be set.

LFA… **Loss of Frame Alignment**

This bit is set after detecting 3 or 4 consecutive incorrect FAS words or 3 or 4 consecutive incorrect service words (can be disabled). With the rising edge of this bit an interrupt status bit (ISR2.LFA) will be set. The specification of the loss of sync conditions is done via bits RC1.SWD and RC1.ASY4. After loss of synchronization, the frame aligner will resynchronize automatically.

The following conditions have to be detected to regain synchronous state:
– The presence of the correct FAS word in frame n.
– The presence of the correct service word (bit 2 = 1) in frame n + 1.
– For a second time the presence of a correct FAS word in frame n + 2.

The bit is cleared when synchronization has been regained (directly after the second correct FAS word of the procedure described above has been received).

If the CRC-multiframe structure is enabled by setting bit FMR2.RFS1, multiframe alignment is assumed to be lost if pulse-frame synchronization has been lost. The resynchronization procedure for multiframe alignment starts after the bit FRS0.LFA has been cleared.

Multiframe alignment has been regained if two consecutive CRC-multiframes have been received without a framing error (refer to FRS0.LMFA).

The bit will be set during alarm simulation and reset if FMR0.SIM is cleared and no alarm condition exists.

If bit FRS0.LFA is cleared a loss of frame alignment recovery interrupt status ISR2.FAR will be generated.

RRA… Receive Remote Alarm

Set if bit 3 of the received service word is set. An alarm interrupt status ISR2.RA can be generated if the alarm condition is detected.

FRS0.RRA will be cleared when no alarm is detected. At the same time a remote alarm recovery interrupt status ISR2.RAR will be generated.

The bit RSW.RRA has the same function.

Both status and interrupt status bits will be set during alarm simulation.

NMF… **No Multiframe Alignment Found**

This bit is only valid if the CRC4 interworking is selected (FMR2.RFS1/0 = 11). Set if the multiframe pattern could not be detected in a time interval of 400 msec after the framer has reached the doubleframe synchronous state. The receiver is then automatically switched to doubleframe format.

This bit is reset if the basic framing has been lost.

LMFA… **Loss of Multiframe Alignment**

Not used in doubleframe format (FMR2.RFS1 = 0). In this case, set to logical ‘1’.

In CRC-multiframe mode (FMR2.RFS1 = 1), this bit is set

– if force resynchronization is initiated by setting bit FMR0.FRS, or

– if multiframe force resynchronization is initiated by setting bit FMR1.MFCS, or

– if pulseframe alignment has been lost (FRS0.LFA).

It is reset if two CRC-multiframes have been received at an interval of $n \times 2$ ms (n = 1, 2, 3…) without a framing error.

If bit FRS0.LMFA is cleared a loss of multiframe alignment recovery interrupt status ISR2.MFAR will be generated.

Framer Receive Status Register 1 (Read)

	7							0	
FRS1		TS16RA	TS16LOS	TS16AIS	TS16LFA		XLS	XLO	(x4D)

TS16RA… **Receive Timeslot 16 Remote Alarm**

This bit contains the actual information of the received remote alarm bit RS1.2 in time-slot 16. Setting and resetting of this bit will cause an interrupt status change ISR3.RA16.

TS16LOS… **Receive Timeslot 16 Loss of Signal**

This bit is set if the incoming TS16 data stream contains always zeros for at least 16 contiguously received time-slots. A one in a time-slot 16 will reset this bit.

TS16AIS… Receive Timeslot 16 Alarm Indication Signal

The detection of the alarm indication signal in timeslot 16 is according to ITU-T G.775.

This bit is set if the incoming TS16 contains less than 4 zeros in each of two consecutive TS16 multiframe periods. This bit will be cleared if two consecutive received CAS multiframe periods contains more than 3 zeros or the multiframe pattern was found in each of them. This bit will be cleared if TS0 synchronization is lost.

TS16LFA… Receive Timeslot 16 Loss of Multiframe Alignment

0 ... The CAS controller is in synchronous state after frame alignment is accomplished.

1 ... This bit is set if the framing pattern ‘0000’ in 2 consecutive CAS multiframes were not found or in all TS16 of the preceding multiframe all bits were reset. An interrupt ISR3.LMFA16 will be generated.

XLS… Transmit Line Short

Significant only if the ternary line interface is selected by LIM1.DRS=0.

0… Normal operation. No short is detected.

1… The XL1 and XL2 are shortend for at least 3 pulses. As a reaction of the short the pins XL1 and XL2 are automatically forced into a high impedance state if bit XPM2.DAXLT is reset. After 128 consecutive pulse periods the outputs XL1/2 are activated again and the internal transmit current limiter is checked. If a short between XL1/2 is still further active the outputs XL1/2 are in high impedance state again. When the short disappears pins XL1/2 are activated automatically and this bit will be reset. With any change of this bit an interrupt ISR1.XLSC will be generated. In case of XPM2.XLT is set this bit will be frozen.

XLO… Transmit Line Open

0… Normal operation

1… This bit will be set if at least 32 consecutive zeros were sent via pins XL1/XL2 resp. XDOP/XDON. This bit is reset with the first transmitted pulse. With the rising edge of this bit an interrupt ISR1.XLSC will be set. In case of XPM2.XLT is set this bit will be frozen.

Receive Service Word Pulseframe (Read)

	7							0	
RSW	RSI		RRA	RYO	RY1	RY2	RY3	RY4	(x4E)

RSI… **Receive Spare Bit for International Use**

First bit of the received service word. It is fixed to one if CRC-multiframe mode is enabled.

RRA… **Receive Remote Alarm**

Equivalent to bit FRS0.RRA.

RY0…RY4… **Receive Spare Bits for National Use (Y-Bits, Sn-Bits, Sa-Bits)**

Receive Spare Bits/Additional Status (Read)

	7							0	
RSP	SI1	SI2		LLBDD	LLBAD	RSIF	RS13	RS15	(x4F)

SI1…SI2… **Submultiframe Error Indication 1, 2**

Not valid if doubleframe format is enabled. In this case, both bits are set to logical ‘1’.

When using CRC-multiframe format these bits are set to

0… If multiframe alignment has been lost, or
if the last multiframe has been received with CRC error(s). SI1 flags a CRC error in last sub-multiframe 1, SI2 flags a CRC error in last sub-multiframe 2.

1 ... If at multiframe synchronous state last assigned sub-multiframe has been received without a CRC error.

Both flags will be actualized with beginning of every received CRC multiframe.

If automatic transmission of sub-multiframe status is enabled by setting bit XSP.AXS, above status information will be inserted automatically in S_i -bit position of every outgoing CRC multiframe (under the condition that time-slot 0 transparent modes are both disabled):
SI1 $\rightarrow$ S_i -bit of frame 13, SI2 $\rightarrow$ S_i -bit of frame 15.

LLBDD… Line Loop Back Deactuation Signal Detected

This bit is set to one in case the LLB deactuate signal is detected and then received over a period of more than 25 msec with a bit error rate less than 1/100. The bit remains set as long as the bit error rate does not exceed 1/100.

If framing is aligned, the timeslot 0 is not taken into account for the error rate calculation.

Any change of this bit will cause a LLBSC interrupt.

LLBAD… Line Loop Back Actuation Signal Detected

Depending on bit LCR1.EPRM the source of this status bit changed.

LCR1.EPRM=0: This bit is set to one in case the LLB actuate signal is detected and then received over a period of more than 25 msec with a bit error rate less than 1/100. The bit remains set as long as the bit error rate does not exceed 1/100.

If framing is aligned, the timeslot 0 is not taken into account for the error rate calculation.

Any change of this bit will cause a LLBSC interrupt.

PRBS Status

LCR1.EPRM=1: The current status of the PRBS synchronizer is indicated in this bit. It is set high if the synchronous state is reached even in the presence of a BER 1/10. A data stream containing all zeros with / without framing bits is also a valid pseudo random bit sequence.

RSIF… Receive Spare Bit for International Use (FAS Word)

First bit in FAS-word. Used only in doubleframe format, otherwise fixed to ‘1’.

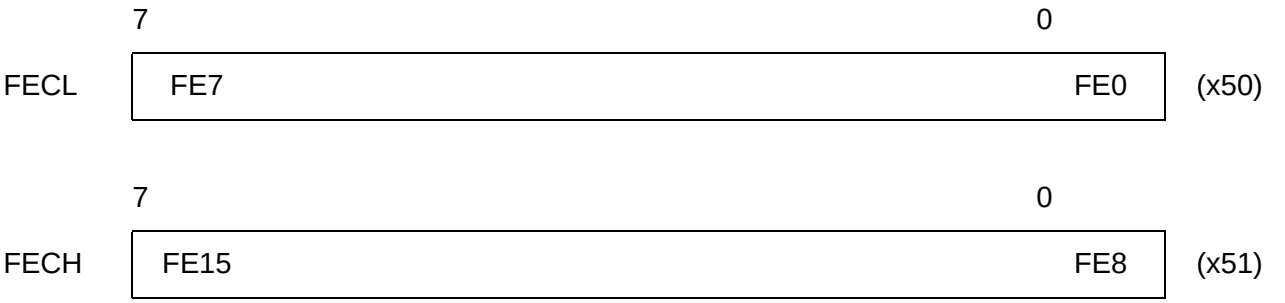
RS13… Receive Spare Bit (Frame 13, CRC Multiframe)

First bit in service word of frame 13. Significant only in CRC-multiframe format, otherwise fixed to ‘0’. This bit is updated with beginning of every received CRC multiframe.

RS15… Receive Spare Bit (Frame 15, CRC Multiframe)

First bit in service word of frame 15. Significant only in CRC-multiframe format, otherwise fixed to ‘0’. This bit is updated with beginning of every received CRC multiframe.

Framing Error Counter (Read)



FE15…FE0… **Framing Errors**

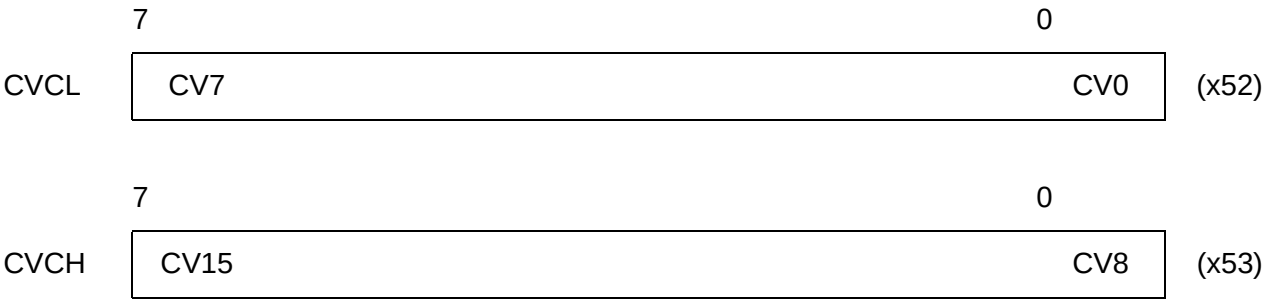
This 16-bit counter will be incremented when a FAS word has been received with an error.

Framing errors will not be counted during asynchronous state. During alarm simulation, the counter is incremented every 250 µs up to its saturation. The error counter will not roll over.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DFEC has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DFEC will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

Code Violation Counter (Read)



CV15…CV0… Code Violations

No function if NRZ code has been enabled.

If the HDB3 or the CMI code is selected, the 16-bit counter will be incremented when violations of the HDB3 code are detected. The error detection mode is determined by programming the bit FMR0.EXTD.

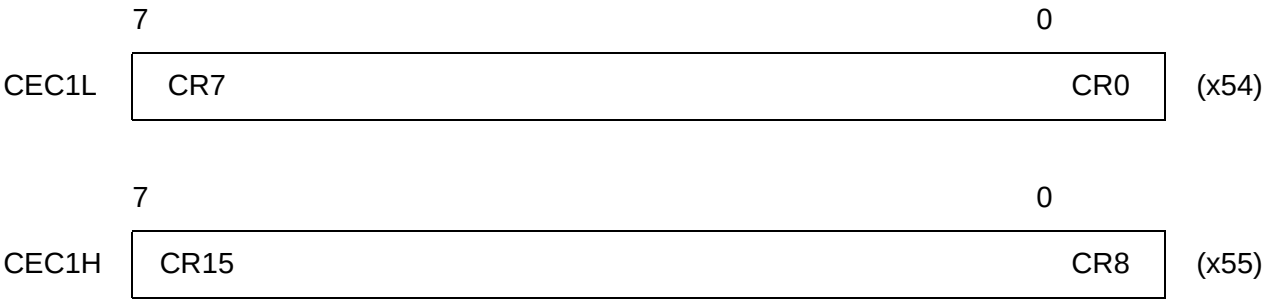
If simple AMI coding is enabled (FMR0.RC0/1 = 10) all bipolar violations are counted. The error counter will not roll over.

During alarm simulation, the counter is incremented every four bits received up to its saturation.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCVC has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DCVC will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

CRC Error Counter 1 (Read)



CR15…CR0… CRC Errors

No function if doubleframe format is selected.

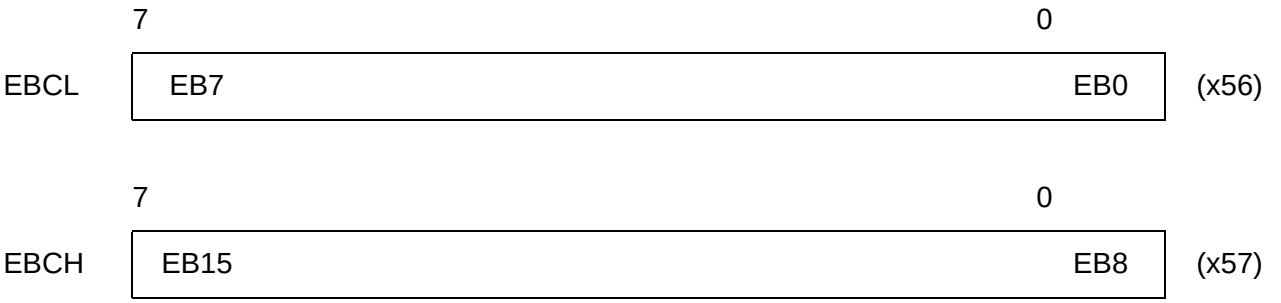
In CRC-multiframe mode, the 16-bit counter will be incremented when a CRC-submultiframe has been received with a CRC error. CRC errors will not be counted during asynchronous state. The error counter will not roll over.

During alarm simulation, the counter is incremented once per submultiframe up to its saturation.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC1 has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DCEC1 will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

E Bit Error Counter (Read)



EB15…EB0… E-Bit Errors

If doubleframe format is selected, FEBEH/L has no function. If CRC-multiframe mode is enabled, FEBEH/L works as submultiframe error indication counter (16 bits) which counts zeros in Si-bit position of frame 13 and 15 of every received CRC multiframe. The error counter will not roll over.

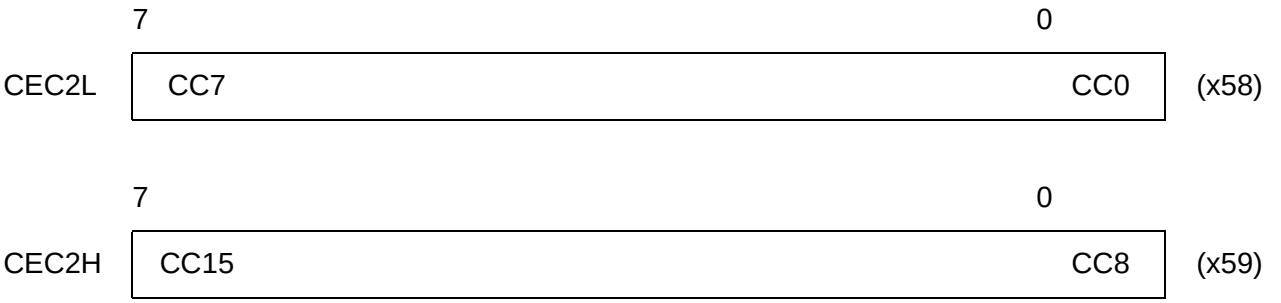
During alarm simulation, the counter is incremented once per submultiframe up to its saturation.

Clearing and updating the counter is done according to bit FMR1.ECM.

If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DEBC has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DEBC will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

CRC Error Counter 2 (Read)



CC15…CC0… CRC Error Counter (Reported from TE via Sa6 -Bit)

Depending of bit LCR1.EPRM the error counter increment is selected:

LCR1.EPRM=0:
If doubleframe format is selected, CEC2H/L has no function. If CRC-multiframe mode is enabled, CEC2H/L works as SA6 Bit error indication counter (16 bits) which counts the SA6 Bit sequence 0001 and 0011in every received CRC submultiframe.
Incrementing the counter is only possible in the multiframe synchronous state FRS0.LMFA = 0.

SA6 Bit sequence: SA61, SA62, SA63, SA64 = 0001 or 0011 where SA61 is received in frame 1 or 9 in every multiframe.

Pseudo Random Bit Sequence Error Counter

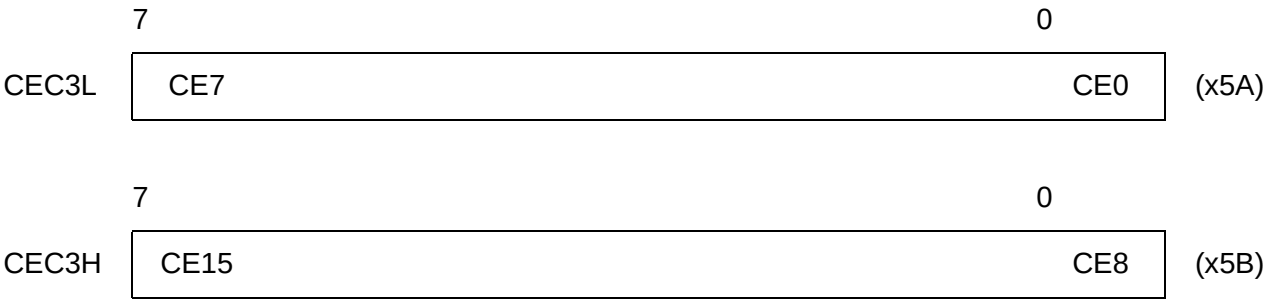
LCR1.EPRM=1:
This 16-bit counter will be incremented with every received PRBS bit error in the PRBS synchronous state FRS1.LLBAD = 1. The error counter will not roll over.

During alarm simulation, the counter is incremented once per submultiframe up to its saturation.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC2 has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DCEC2 will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

CRC Error Counter 3 (Read)



CE15…CE0… CRC Error Counter (detected at T Ref. Point via Sa6 -Bit)

GCR.ECMC = 0 : If doubleframe format is selected, CEC3H/L has no function. If CRC-multiframe mode is enabled, CEC3H/L works as SA6 Bit error indication counter (16 bits) which counts the SA6 Bit sequence 0010 and 0011in every received CRC submultiframe.
Incrementing the counter is only possible in the multiframe synchronous state FRS0.LMFA = 0.

SA6 Bit sequence: SA61, SA62, SA63, SA64 = 0010 or 0011 where SA61 is received in frame 1 or 9 in every multiframe. The error counter will not roll over.
During alarm simulation, the counter is incremented once per submultiframe up to its saturation.

CE7…CE2… Multiframe Counter

GCR.ECMC = 1 : This 6 bit counter increments with each multiframe period in the asynchronous state FRS0.LFA/LMFA =1.

During alarm simulation, the counter is incremented once per multiframe up to its saturation.

CE1…CE0… Change of Frame Alignment Counter

GCR.ECMC = 1 : This 2 bit counter increments with each detected change of frame / multiframe alignment. The error counter will not roll over.

During alarm simulation, the counter is incremented once per multiframe up to its saturation.
Clearing and updating the counter is done according to bit FMR1.ECM.

If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC3 has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DCEC3 will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

Receive Sa4-Bit Register (Read)

	7	0	
RSA4	RS47	RS40	(x5C)
RSA5	RS57	RS50	(x5D)
RSA6	RS67	RS60	(x5E)
RSA7	RS77	RS70	(x5F)
RSA8	RS87	RS80	(x60)

RS47…RS40… Receive Sa4-Bit Data (Y-Bits)

RS57…RS50… Receive Sa5-Bit Data

RS67…RS60… Receive Sa6-Bit Data

RS77…RS70… Receive Sa7-Bit Data

RS87…RS80… Receive Sa8-Bit Data

This register contains the information of the eight SAx bits (x = 4 - 8) of the previously received CRC multiframe. These registers will be updated with every multiframe begin interrupt ISR0.RMB.

RS40 is received in bit-slot 4 of every service word in frame 1, RS47 in frame 15

RS50 is received in bit-slot 5, time-slot 0, frame 1, RS57 in frame 15

RS60 is received in bit-slot 6, time-slot 0, frame 1, RS67 in frame 15

RS70 is received in bit-slot 7, time-slot 0, frame 1, RS77 in frame 15

RS80 is received in bit-slot 8, time-slot 0, frame 1, RS87 in frame 15

Valid if CRC multiframe format is enabled by setting bits FMR2.RFS1 = 1 or FMR2.RFS1/0 = 01 (Doubleframe format).

Receive Sa6-Bit Status (Read)

	7							0	
RSA6S			S_X	S_F	S_E	S_C	S_A	S_8	(x61)

Four consecutive received SA6-bits are checked on the by ETS 300233 defined SA6-bit combinations. The QuadFALC will detect the following “fixed” SA6-bit combinations:
SA61,SA62,SA63,SA64=1000; 1010; 1100; 1110; 1111. All other possible 4 bit combinations are grouped to status “X”.

A valid SA6-bit combination must occur three times in a row. The corresponding status bit in this register will be set. Even if the detected status will be active for a short time the status bit remains active until this register is read. Reading the register will reset all pending status information.
With any change of state of the SA6-bit combinations an interrupt status ISR0.SA6SC will be generated.
During the basicframe asynchronous state updating of this register and interrupt status ISR0.SA6SC is disabled. In multiframe format the detection of the SA6-bit combinations can be done either synchronous or asynchronous to the submultiframe (FMR3.SA6SY). In synchronous detection mode updating of register RSA6S is done in the multiframe synch. state (FRS0.LMFA=0). In asynchr. detection mode updating is independent to the multiframe synchronous state.

S_X… **Receive Sa6-Bit Status_X**

If none of the fixed SA6-bit combinations are detected this bit will be set.

S_F… **Receive Sa6-Bit Status: “1111”**

Receive SA6-bit status “1111” is detected for three times in a row in the SA6-bit positions.

S_E… **Receive Sa6-Bit Status: “1110”**

Receive SA6-bit status “1110” is detected for three times in a row in the SA6-bit positions.

S_C… **Receive Sa6-Bit Status: “1100”**

Receive SA6-bit status “1100” is detected for three times in a row in the SA6-bit positions.

S_A… **Receive Sa6-Bit Status: “1010”**

Receive SA6-bit status “1010” is detected for three times in a row in the SA6-bit positions.

S_8… Receive Sa6-Bit Status: “1000”

Receive SA6-bit status “1000” is detected for three times in a row in the SA6-bit positions.

Receive Signaling Pointer 1 (Read)

Value after RESET: 00_H

	7							0	
RSP1	RS8C	RS7C	RS6C	RS5C	RS4C	RS3C	RS2C	RS1C	(x62)

RS8C…RS1C Receive Signaling Register RS1-8 Changed

A one in each bit position indicates that the received signaling data in the corresponding RS1-8 registers are updated. Bit RS1C is the pointer for register RS1,... while RS8C points to RS8.

Receive Signaling Pointer 2 (Read)

Value after RESET: 00_H

	7							0	
RSP2	RS16C	RS15C	RS14C	RS13C	RS12C	RS11C	RS10C	RS9C	(x63)

RS16C…RS9C Receive Signaling Register RS9-16 Changed

A one in each bit position indicates that the received signaling data in the corresponding RS9-16 registers are updated. Bit RS9C is the pointer for register RS9,... while RS16C points to RS16.

Signaling Status Register (Read)

	7							0	
SIS	XDOV	XFW	XREP		RLI	CEC	SFS		(x64)

XDOV… Transmit Data Overflow

More than 32 bytes have been written to the XFIFO.
This bit is reset by:

– a transmitter reset command XRES

– or when all bytes in the accessible half of the XFIFO have been moved in the inaccessible half.

XFW… **Transmit FIFO Write Enable**

Data can be written to the XFIFO.

XREP… **Transmission Repeat**

Status indication of CMDR.XREP.

RLI… **Receive Line Inactive**

Neither FLAGs as Interframe Time Fill nor frames are received via the signaling timeslot.

CEC… **Command Executing**

0… No command is currently executed, the CMDR register can be written to.

1… A command (written previously to CMDR) is currently executed, no further command can be temporarily written in CMDR register.

Note: CEC will be active at most 2.5 periods of the current system data rate.

SFS… **Status Freeze Signaling**

0… freeze signaling status inactive.

1… freeze signaling status active

Receive Signaling Status Register (Read)

	7							0	
RSIS	VFR	RDO	CRC16	RAB	HA1	HA0		LA	(x65)

RSIS relates to the last received HDLC frame; it is copied into RFIFO when end-of-frame is recognized (last byte of each stored frame).

VFR… **Valid Frame**

Determines whether a valid frame has been received.

1… valid

0… invalid

An invalid frame is either

– a frame which is not an integer number of 8 bits (n × 8 bits) in length (e.g. 25 bits), or

– a frame which is too short taking into account the operation mode selected via MODE (MDS2-0) and the selection of receive CRC ON/OFF (CCR2.RCRC) as follows:
  - MDS2-0 = 011 (16 bit Address), RCRC = 0 : 4 bytes; RCRC = 1 : 3-4 bytes
  - MDS2-0 = 010 (8 bit Address), RCRC = 0 : 3 bytes; RCRC = 1 : 2-3 bytes

Note: Shorter frames are not reported.

RDO… Receive Data Overflow

A RFIFO data overflow has occurred during reception of the frame.

Additionally, an interrupt can be generated (refer to ISR1.RDO/IMR1.RDO).

CRC16… CRC16 Compare/Check

0… CRC check failed; received frame contains errors.

1… CRC check o.k.; received frame is error-free.

RAB… Receive Message Aborted

The received frame was aborted from the transmitting station. According to the HDLC protocol, this frame must be discarded by the receiver station.

HA1, HA0… High Byte Address Compare

Significant only if 2-byte address mode has been selected.

In operating modes which provide high byte address recognition, the QuadFALC compares the high byte of a 2-byte address with the contents of two individually programmable registers (RAH1, RAH2) and the fixed values FE_H and FC_H (broadcast address).

Dependent on the result of this comparison, the following bit combinations are possible:

00… RAH2 has been recognized

01… Broadcast address has been recognized

10… RAH1 has been recognized C/R = 0 (bit 1)

11… RAH1 has been recognized C/R = 1 (bit 1)

Note: If RAH1, RAH2 contain identical values, a match is indicated by ‘10’ or ‘11’.

LA… **Low Byte Address Compare**

Significant in HDLC modes only.

The low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared with two registers. (RAL1, RAL2).

0… RAL2 has been recognized

1… RAL1 has been recognized

Receive Byte Count Low (Read)

	7							0	
RBCL	RBC7							RBC0	(x66)

Together with RBCH (bits RBC11 - RBC8), indicates the length of a received frame (1…4095 bytes). Bits RBC4-0 indicate the number of valid bytes currently in RFIFO. These registers must be read by the CPU following a RME interrupt.

Received Byte Count High (Read)

Value after RESET: 000_{xxxxx}

	7							0	
RBCH				OV	RBC11			RBC8	(x67)

OV… **Counter Overflow**

More than 4095 bytes received.

RBC11 – RBC8… **Receive Byte Count (most significant bits)**

Together with RBCL (bits RBC7…RBC0) indicate the length of the received frame.

Interrupt Status Register 0 (Read)

Value after RESET: 00_H

	7							0	
ISR0	RME	RFS	T8MS	RMB	CASC	CRC4	SA6SC	RPF	(x68)

All bits are reset when ISR0 is read.

If bit GCR.VIS is set to ‘1’, interrupt statuses in ISR0 may be flagged although they are masked via register IMR0. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

RME… **Receive Message End**

One complete message of length less than 32 bytes, or the last part of a frame at least 32 bytes long is stored in the receive FIFO, including the status byte.

The complete message length can be determined reading the RBCH, RBCL registers, the number of bytes currently stored in RFIFO is given by RBC4–0. Additional information is available in the RSIS register.

RFS… **Receive Frame Start**

This is an early receiver interrupt activated after the start of a valid frame has been detected, i.e. after an address match (in operation modes providing address recognition), or after the opening flag (transparent mode 0) is detected, delayed by two bytes. After an RFS interrupt, the contents of

- RAL1
- RSIS - bits 3-1

are valid and can be read by the CPU.

T8MS… **Receive Time Out 8 msec**

Only active if multiframing is enabled.

The framer has found the doubleframing (basic framing) FRS0.LFA = 0 and is searching for the multiframing. This interrupt will be set to indicate that no multiframing could be found within a time window of 8 msec. In multiframe synchronous state this interrupt will be not generated. Refer also to Floating multiframe alignment window.

RMB… **Receive Multiframe Begin**

This bit is set with the beginning of a received CRC multiframe related to the internal receive line timing.

In CRC multiframe format FMR2.RFS1 = 1 or in doubleframe format FMR2.RFS1/0 = 01 this interrupt occurs every 2 msec. If FMR2.RFS1/0 = 00 this interrupt will be generated every doubleframe (512 bits).

CASC… **Received CAS Information Changed**

This bit is set with the updating of a received CAS multiframe information in the registers RS1-16. If the last received CAS information changed from the previous received updating is started. This interrupt will only occur in the TS0 and TS16 synchronous state. The registers RS1-16 should be read within the next 2 ms otherwise the contents may be lost.

CRC4… **Receive CRC4 Error**

0... No CRC4 error occurs.

1... The CRC4 check of the last received submultiframe failed.

SA6SC… **Receive SA6-Bit Status Changed**

With every change of state of the received SA6-bit combinations this interrupt will be set.

RPF… **Receive Pool Full**

32 bytes of a frame have arrived in the receive FIFO. The frame is not yet completely received.

Interrupt Status Register 1 (Read)

	7							0	
ISR1	LLBSC	RDO	ALLS	XDU	XMB		XLSC	XPR	(x69)

All bits are reset when ISR1 is read.

If bit GCR.VIS is set to ‘1’, interrupt statuses in ISR1 may be flagged although they are masked via register IMR1. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

LLBSC… **Line Loop Back Status Change**

Depending on bit LCR1.EPRM the source of this interrupt status changed:

LCR1.EPRM=0: This bit is set to one, if the LLB actuate signal or the LLB deactuate signal, resp., is detected over a period of 25 msec with a bit error rate less than 1/100.

The LLBSC bit is also set to one, if the current detection status is left, i.e., if the bit error rate exceeds 1/100.

The actual detection status can be read from the RSP.LLBAD and RSP.LLBDD, resp.

PRBS Status Change

LCR1.EPRM=1: With any change of state of the PRBS synchronizer this bit will be set. The current status of the PRBS synchronizer is indicated in RSP.LLBAD.

RDO… Receive Data Overflow

This interrupt status indicates that the CPU does not respond quickly enough to an RPF or RME interrupt and that data in RFIFO has been lost. Even when this interrupt status is generated, the frame continues to be received when space in the RFIFO is available again.

Note: Whereas the bit RSIS.RDO in the frame status byte indicates whether an overflow occurred when receiving the frame currently accessed in the RFIFO, the ISR1.RDO interrupt status is generated as soon as an overflow occurs and does not necessarily pertain to the frame currently accessed by the processor.

ALLS… All Sent

This bit is set if the last bit of the current frame is completely sent out and XFIFO is empty.

XDU… Transmit Data Underrun

Transmitted frame was terminated with an abort sequence because no data was available for transmission in XFIFO and no XME was issued.

Note: Transmitter and XFIFO are reset and deactivated if this condition occurs. They are re-activated not before this interrupt status register has been read. Thus, XDU should not be masked via register IMR1.

XMB… Transmit Multiframe Begin

This bit is set every 2 ms with the beginning of a transmitted multiframe related to the internal transmit line interface timing.
Just before setting this bit registers XS1-16 are copied in the transmit

shift registers. The registers XS1-16 are empty and has to be updated otherwise the contents will be retransmitted.

XLSC… Transmit Line Status Change

XLSC is set to one with the rising edge of the bit FRS1.XLO or with any change of bit FRS1.XLS.

The actual status of the transmit line monitor can be read from the FRS1.XLS and FRS1.XLO.

XPR… Transmit Pool Ready

A data block of up to 32 bytes can be written to the transmit FIFO. XPR enables the fastest access to XFIFO. It has to be used for transmission of long frames, back-to-back frames or frames with shared flags.

Interrupt Status Register 2 (Read)

	7							0	
ISR2	FAR	LFA	MFAR	T400MS	AIS	LOS	RAR	RA	(x6A)

All bits are reset when ISR2 is read.

If bit GCR.VIS is set to ‘1’, interrupt statuses in ISR2 may be flagged although they are masked via register IMR2. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

FAR… Frame Alignment Recovery

The framer has reached doubleframe synchronization. Set when bit FSR0.LFA is reset. It is set also after alarm simulation is finished and the receiver is still synchron.

LFA… Loss of Frame Alignment

The framer has lost synchronization and bit FRS0.LFA is set. It will be set during alarm simulation.

MFAR… Multiframe Alignment Recovery

Set when the framer has found two CRC-multiframes at an interval of n x 2 ms (n = 1, 2, 3, …) without a framing error. At the same time bit FRS0.LMFA is reset.

It is set also after alarm simulation is finished and the receiver is still synchron. Only active if CRC-multiframe format is selected.

T400MS… Receive Time Out 400 msec

Only active if multiframing is enabled.

The framer has found the doubleframing (basic framing) FRS0.LFA = 0 and is searching for the multiframing. This interrupt will be set to indicate that no multiframing could be found within a time window of 400 msec after basic framing has been achieved. In multiframe synchronous state this interrupt will not be generated.

AIS… Alarm Indication Signal

This bit is set when an alarm indication signal is detected and bit FRS0.AIS is set. It will be set during alarm simulation.
If GCR.SCI is set high this interrupt status bit will be set with every change of state of FRS0.AIS.

LOS… Loss of Signal

This bit is set when a loss of signal alarm is detected in the received bitstream and FRS0.LOS is set. It will be set during alarm simulation. If GCR.SCI is set high this interrupt status bit will be set with every change of state of FRS0.LOS.

RAR… Remote Alarm Recovery

Set if a remote alarm in TS0 is cleared and bit FRS0.RA is reset. It is set also after alarm simulation is finished and no remote alarm is detected.

RA… Remote Alarm

Set if a remote alarm in TS0 is detected and bit FRS0.RA is set. It will be set during alarm simulation.

Interrupt Status Register 3 (Read)

	7							0	
ISR3	ES	SEC	LMFA16	AIS16	RA16		RSN	RSP	(x6B)

All bits are reset when ISR3 is read.

If bit GCR.VIS is set to ‘1’, interrupt statuses in ISR3 may be flagged although they are masked via register IMR3. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

ES… **Errored Second**

This bit is set if at least one enabled interrupt source via ESM is set during the time interval of one second. Interrupt sources of ESM register:
LFA = Loss of frame alignment detected (FRS0.LFA)
FER = Framing error received
CER = CRC error received
AIS = Alarm indication signal (FRS0.AIS)
LOS = Loss of signal (FRS0.LOS)
CVE = Code violation detected
SLIP = Receive Slip positive/negative detected
EBE = E- Bit error detected (RSP.RS13/15)

SEC… **Second Timer**

The internal one second timer has expired. The timer is derived from clock RCLK.

LMFA16… **Loss of Multiframe Alignment TS 16**

Multiframe alignment of timeslot 16 has been lost if two consecutive multiframe pattern are not detected or if in 16 consecutive timeslot 16 all bits are reset.
If register GCR.SCI is high this interrupt status bit will be set with every change of state of FRS1.TS16LFA.

AIS16… **Alarm Indication Signal TS 16 Status Change**

The alarm indication signal AIS in timeslot 16 for the 64 kbit/s channel associated signaling is detected or cleared. A change in bit FRS1.TS16AIS will set this interrupt. (This bit is set if the incoming TS 16 signal contains less than 4 zeros in each of two consecutive TS16-multiframe periods.)

RA16… **Remote Alarm TS 16 Status Change**

A change in the remote alarm bit in CAS multiframe alignment word is detected.

RSN… **Receive Slip Negative**

The frequency of the receive route clock is greater than the frequency of the receive system interface working clock based on 2.048 MHz. A frame will be skipped. It will be set during alarm simulation.

RSP… **Receive Slip Positive**

The frequency of the receive route clock is less than the frequency of the receive system interface working clock based on 2.048 MHz. A frame will be repeated. It will be set during alarm simulation.

Interrupt Status Register 4 (Read)

	7							0	
ISR4	XSP	XSN							(x6C)

All bits are reset when ISR4 is read.

If bit GCR.VIS is set to ‘1’, interrupt statuses in ISR4 may be flagged although they are masked via register IMR4. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

XSP… **Transmit Slip Positive**

The frequency of the transmit clock is less than the frequency of the transmit system interface working clock based on 2.048 MHz. A frame will be repeated.

XSN… **Transmit Slip Negative**

The frequency of the transmit clock is greater than the frequency of the transmit system interface working clock based on 2.048 MHz. A frame will be skipped.

Global Interrupt Status Register (Read)

Value after RESET: 00_H

	7							0	
GIS				ISR4	ISR3	ISR2	ISR1	ISR0	(x6E)

This status register points to pending interrupts sourced by ISR4 ... ISR0.

Channel Interrupt Status Register (Read)

Value after RESET: 00_H

	7							0	
CIS					GIS4	GIS3	GIS2	GIS1	(6F)

This status register points to pending interrupts sourced by the GIS registers of each channel.

GIS4 ... register GIS of FALC4
GIS3 ... register GIS of FALC3
GIS2 ... register GIS of FALC2
GIS1 ... register GIS of FALC1

Receive CAS Register (Read)

Value after RESET: not defined

	7							0	
RS1	0	0	0	0	X	Y	X	X	(x70)
RS2	A1	B1	C1	D1	A16	B16	C16	D16	(x71)
RS3	A2	B2	C2	D2	A17	B17	C17	D17	(x72)
RS4	A3	B3	C3	D3	A18	B18	C18	D18	(x73)
RS5	A4	B4	C4	D4	A19	B19	C19	D19	(x74)
RS6	A5	B5	C5	D5	A20	B20	C20	D20	(x75)
RS7	A6	B6	C6	D6	A21	B21	C21	D21	(x76)
RS8	A7	B7	C7	D7	A22	B22	C22	D22	(x77)
RS9	A8	B8	C8	D8	A23	B23	C23	D23	(x78)
RS10	A9	B9	C9	D9	A24	B24	C24	D24	(x79)
RS11	A10	B10	C10	D10	A25	B25	C25	D25	(x7A)
RS12	A11	B11	C11	D11	A26	B26	C26	D26	(x7B)
RS13	A12	B12	C12	D12	A27	B27	C27	D27	(x7C)
RS14	A13	B13	C13	D13	A28	B28	C28	D28	(x7D)
RS15	A14	B14	C14	D14	A29	B29	C29	D29	(x7E)
RS16	A15	B15	C15	D15	A30	B30	C30	D30	(x7F)

Receive CAS Register 1-16

Each register except RS1 contains the received CAS bits for two timeslots. The received CAS multiframe will be compared with the previously received one. If the contents changed a CAS multiframe changed interrupt (ISR0.CASC) is generated and informs the user that a new multiframe has to be read within the next 2 ms. If requests for reading the RS1-16 register are ignored, the received data may be lost. RS1 contains frame 0 of the CAS multiframe. MSB is received first.

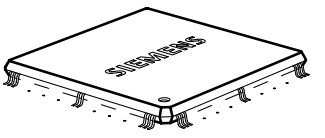
Additionally a receive signaling data change pointer indicates an update of register RS1-16 . Refer also to register RSP1/2.
Access to RS1-16 registers is only valid if the serial receive signaling access on the system highway is disabled.

SIEMENS

Quad Framing and Line Interface Component for E1/T1 QuadFALC — PEB 22554

CMOS

QuadFALC in T1 / J1 Mode



P-TQFP-144

5 Features T1 / J1

Quad Line Interface

- High density, generic interface for all E1 / DS1 / DSX-1 / J1 applications
- Analog receive and transmit circuitry for long / short haul applications
- Data and clock recovery using an integrated digital phase locked loop
- Maximum line attenuation up to -36 dB at 772 kHz adaptively controlled receive equalization network adjusts up to 6200 feet (pulp 22AWG) in length, noise - and crosstalk -filter, line attenuation status
- Programmable Line Build-Out for CSU signals according to ANSI T1. 403+ FCC68 0dB, -7.5dB, -15dB, -22.5 dB
- Low transmitter output impedance for high transmit return loss
- Tri-state function of the analog Transmit Line Outputs
- Programmable transmit pulse shape
- Transmit line monitor protecting the device from damage
- Jitter specifications of ITU-T I.431, G.703 and AT&T TR 62411 met
- Crystal-less wander and jitter attenuation/compensation
- Low frequency reference clock: 1.544 MHz
- Power down function per channel
- Dual rail or single rail digital inputs and outputs
- Unipolar NRZ for interfacing fibre optical transmission routes
- Selectable line codes (B8ZS, AMI with ZCS)
- Loss of signal indication with programmable thresholds according to ITU-T G.775 and ANSI T1. 403
- Clock generator for jitter free system / transmit clocks per channel
- Local loop and remote loop for diagnostic purposes
- Low power device , single power supply: 3.3 V

Type	Version	Ordering Code	Package
PEB 22554-H	V1.1		P-TQFP-144(SMD)

Quad Frame Aligner

- Frame alignment/synthesis for 1.544 MBit/s according to ITU-T G.704 and JT G.704
- Programmable formats : 4-Frame Multiframe (F4, FT), 12-Frame Multiframe (F12, D3/4), Extended Superframe (ESF), Remote Switch Mode (F72, SLC96)
- Selectable conditions for recover and loss of frame alignment
- Performs synchronization in ESF format acc. to NTT requirements
- Error checking via CRC6 procedures according to ITU-T G. 706 and JT G. 706
- Supports the alternate CRC6 algorithm acc. to the 'japanese standard' JT G. 706
- Alarm and performance monitoring per second
  16 bit counter for CRC-, framing errors, code violations, Errored blocks, PRBS bit errors
- Insertion and extraction of alarms (AIS, Remote (Yellow) Alarm, …)
- Yellow Alarm generation/checking according to 'japanese standard ' JT-G.704
- IDLE code insertion for selectable channels
- Flexible system clock frequency different for receiver and transmitter
- Supports programmable system data rates: 2.048 , 4.096, 8.192, 16.384 MBit/s and 1.544, 3.088, 6.176, 12.352 MBit/s with independent receive / transmit shifts
- Mux of 4 channels into a single rail 8.192 or 6.176 MBit/s data bus and v.v.
  with byte - or bitinterleaved formats
- Supports fractional T1 access
- Elastic store for receive and transmit route clock wander and jitter compensation; controlled slip capability and slip indication;
- Programmable elastic buffer size: 2 frames / 1 frame / short buffer / bypass
- Provides different time-slot mapping modes
- Flexible transparent modes
- Programmable In-Band Loop Code detection / generation according to TR 62411
- Channel loop back , line loop back or Payload loop back capabilities (AT&T TR 54016)
- Pseudo random signal generator and monitor
- Support for different data link schemes
- Clear channel capabilities

Quad Signaling Controller

- HDLC controller
  Bit stuffing, CRC check and generation, flag generation, flag and address recognition, handling of bit oriented functions
- DL-channel protocol for ESF format according to ANSI T1.403 specification or according to AT&T TR54016.
- Robbed-bit signaling with last look capability, enhanced CAS-BR register access and freeze signaling indication
- Provides access to serial signaling data streams

- DL-access for F72 (SLC96) format
- CAS controller
- Transparent Mode
- FIFO buffers (64 bytes deep) for efficient transfer of data packets.
- Time-slot assignment
  Any combination of time slots selectable for data transfer independent of signaling mode. Useful for fractional T1 applications.

MP Interface

- 8/16 bit microprocessor bus interface (Intel or Motorola type)
- All registers directly accessible (byte or word access)
- Multiplexed and non-multiplexed address bus operations
- Hard / software reset options
- Extended interrupt capabilities
- One second timer (internal /external access)

General

- Boundary scan standard IEEE 1149.1
- P-TQFP-144 package (body size 20*20)
- 3.3 V power supply
- Typical power consumption 700 mW

5.1 Logic Symboly

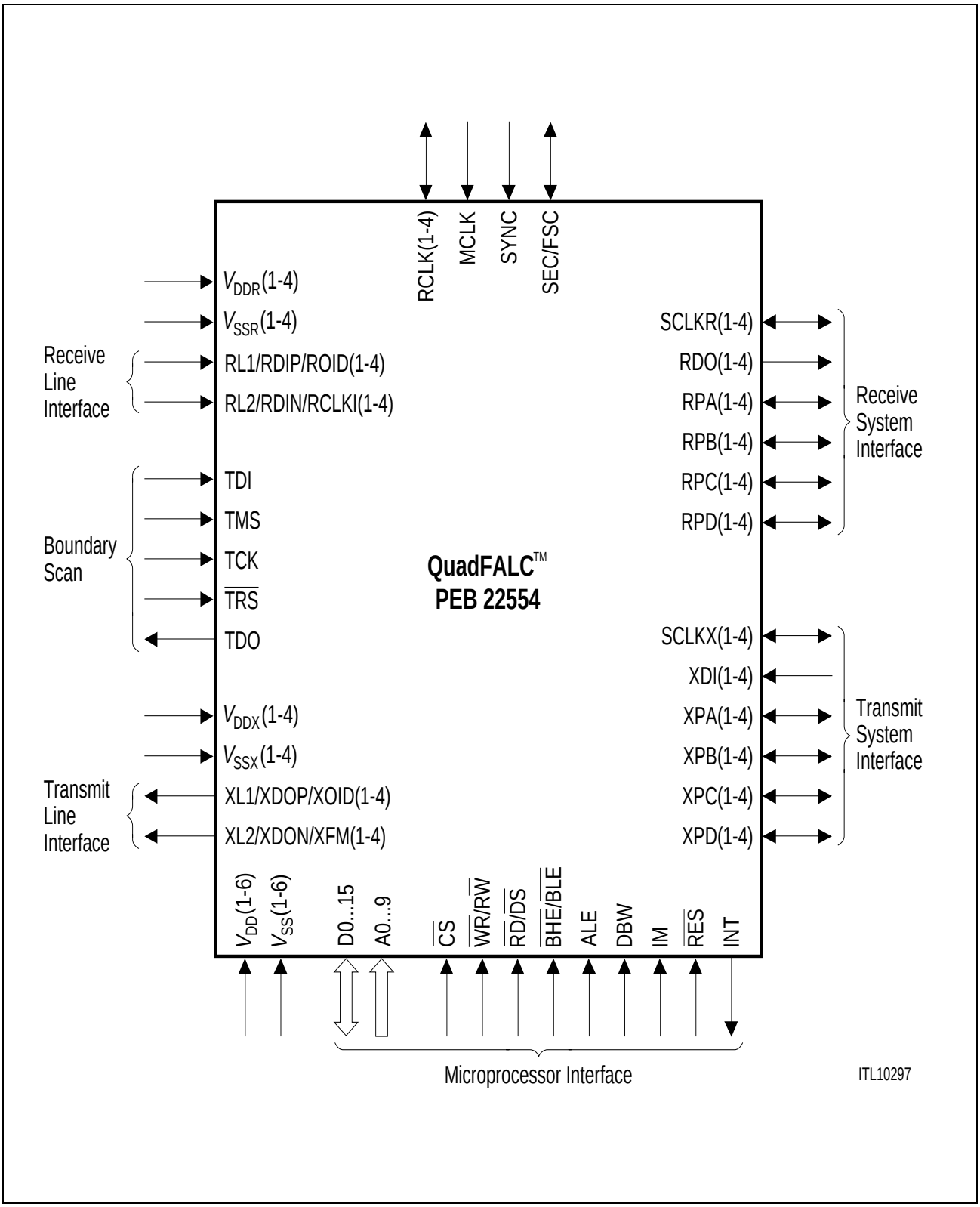


Figure 34
QuadFALC Logic Symbol

5.2 Typical Applications

The figures below show multiple link applications realized with the QuadFALC.

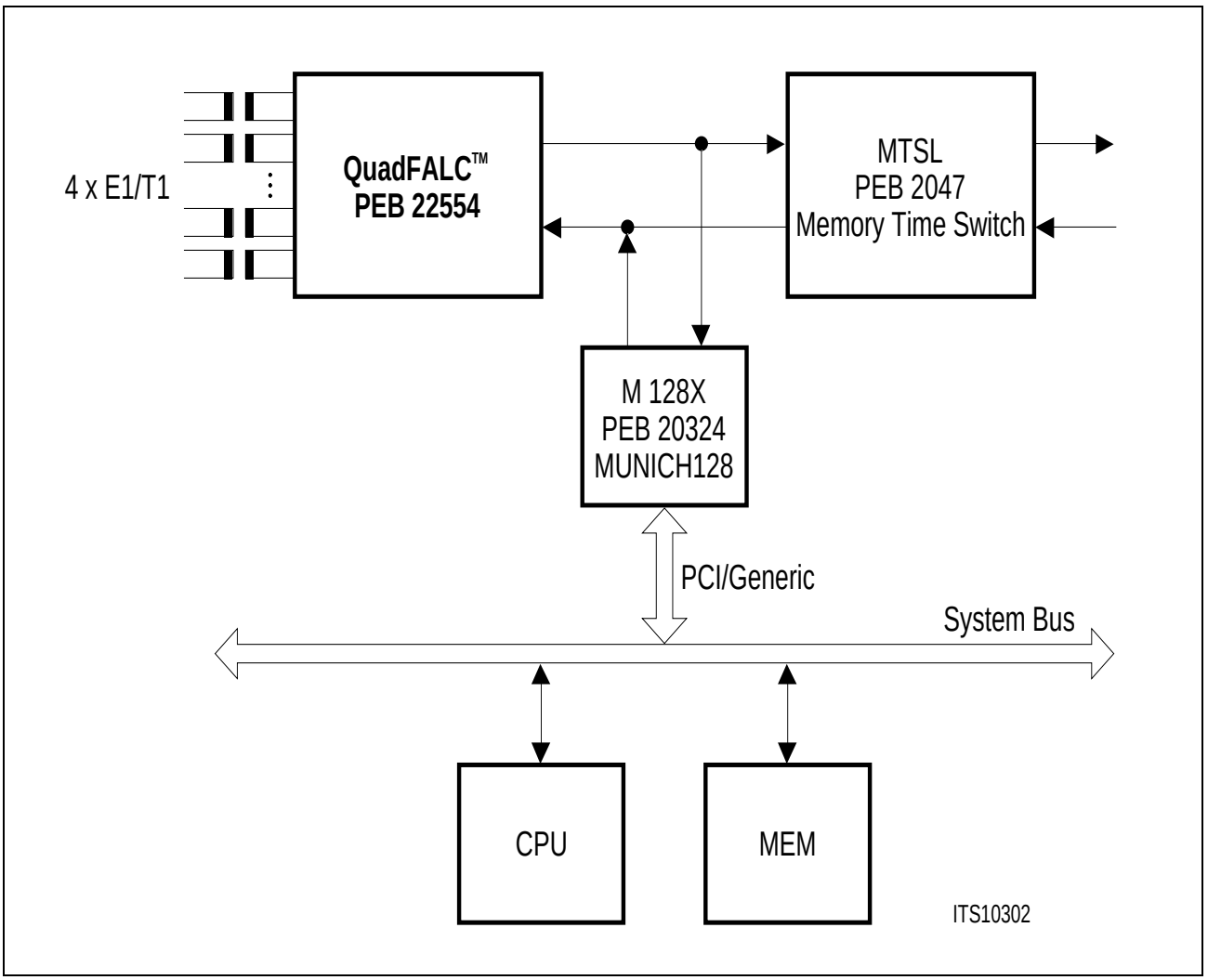


Figure 35
4 Channel E1 Interface for Frame Relay Applications

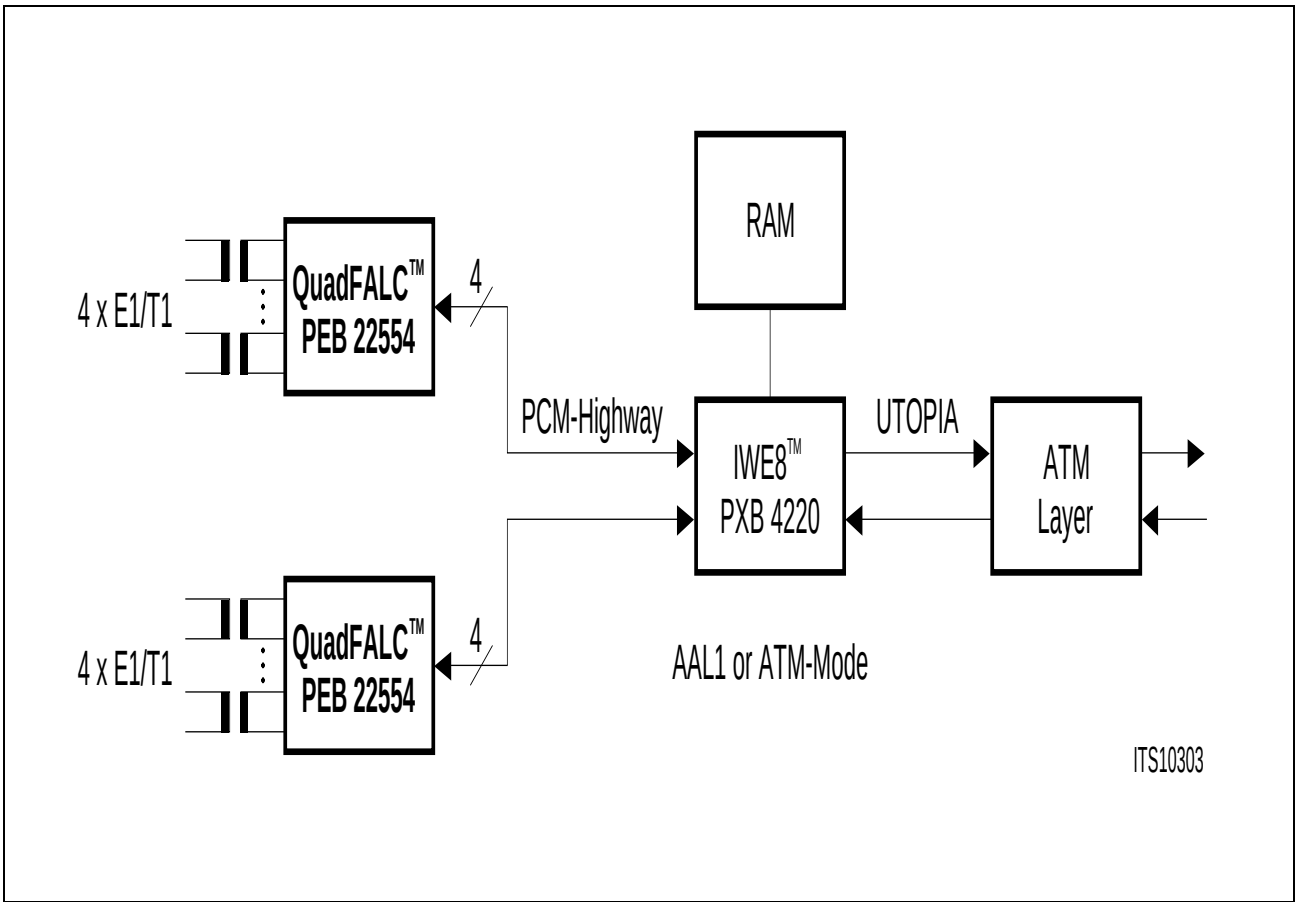


Figure 36
8 Channel E1 Interface to the ATM Layer

6 Pin Descriptions T1

6.1 Pin Diagram

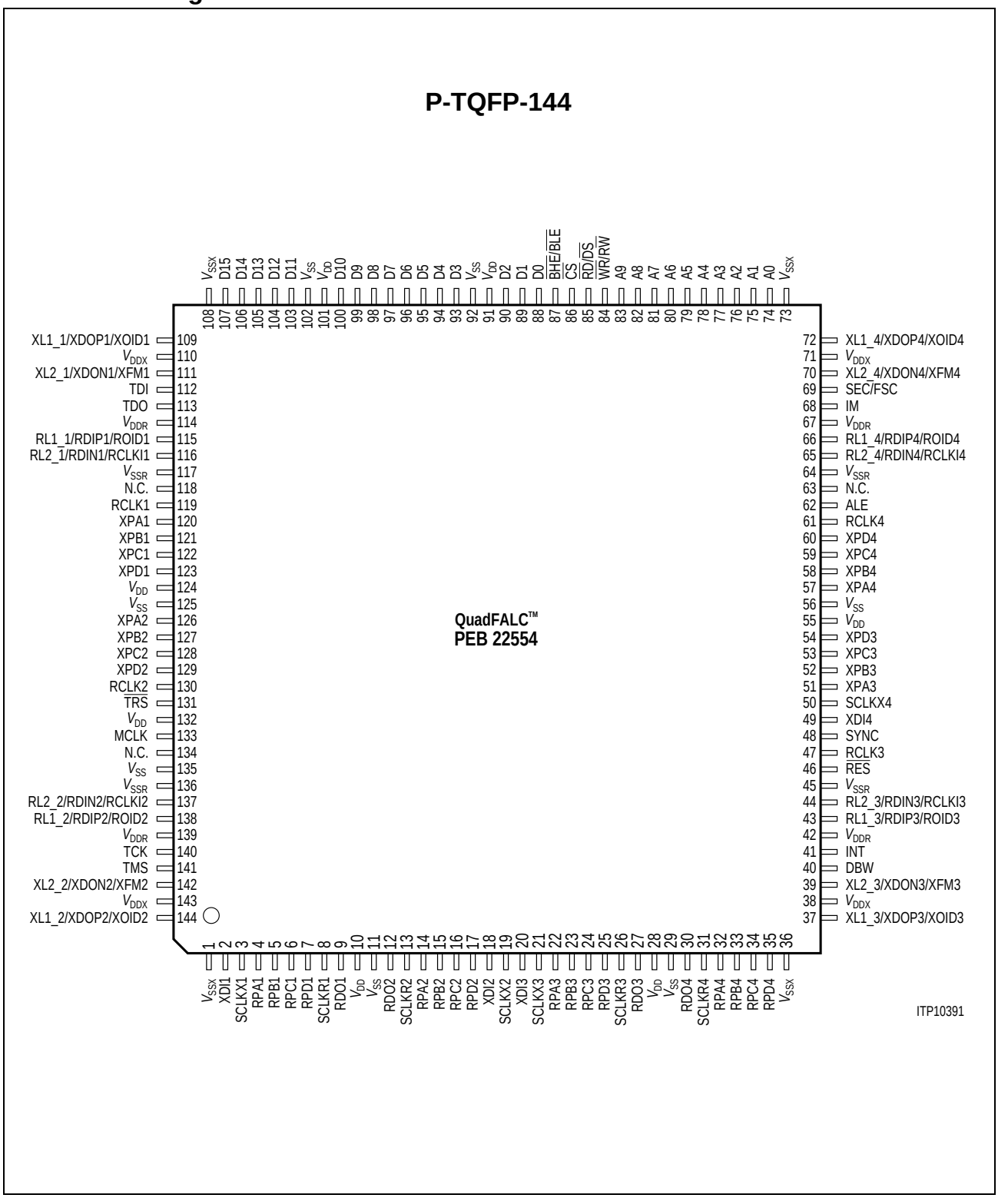


Figure 37
Pin Configuration of QuadFALC

6.2 Pin Definitions and Function

Pin No.	Symbol	Input (I) Output (O)	Function
83 - 74	A9 … A0	I	**Address Bus** Address bus selects one of the internal registers for read or write.
107 -103 100 - 93 90 - 88	D15 … D11 D10 … D3 D2 … D0	I/O	**Data Bus** Bi-directional three-state data lines which interface with the system's data bus. Their configuration is controlled by the level of pin DBW: – 8-bit mode (DBW = 0): D0 … D7 are active. D8 … D15 are in high impedance and have to be connected to V_{DD} or V_{SS}. – 16-bit mode (DBW = 1): D0 … D15 are active. In case of byte transfers, the active half of the bus is determined by A0 and $\overline{BHE}$/$\overline{BLE}$ and the selected bus interface mode (via pin IM). The unused half is in high impedance. For detailed information, refer to **chapter 7.2**.
62	ALE	I	**Address Latch Enable** A high on this line indicates an address on the external address/data bus. The address information provided on lines A0 … A9 is internally latched with the falling edge of ALE. This function allows the QuadFALC to be directly connected to a multiplexed address/data bus. In this case, pins A0 … A9 must be externally connected to the Data Bus pins.In case of demultiplexed mode this pin has to be connected directly to ground or V_{DD}. For detailed information, refer to **chapter 7.2**.

Note: All unused input pins have to be connected to a defined level V_{DD} or V_{SS}.

Note: PU = If not connected an internal pull-up transistor ensure high input level.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
85	$\overline{RD}/\overline{DS}$	I	**Read Enable** (Siemens/Intel bus mode) This signal indicates a read operation. When the QuadFALC is selected via $\overline{CS}$ the $\overline{RD}$ signal enables the bus drivers to output data from an internal register addressed via A0 … A9 on to Data Bus. For more information about control/status register and FIFO access in the different bus interface modes refer to **chapter 7.2**. **Data Strobe** (Motorola bus mode) This pin serves as input to control read/write operations.
84	$\overline{WR}/R\overline{W}$	I	**Write Enable** (Siemens/Intel bus mode) This signal indicates a write operation. When $\overline{CS}$ is active the QuadFALC loads an internal register with data provided via the Data Bus. For more information about control/status register and FIFO access in the different bus interface modes refer to **chapter 7.2**. **Read/Write Enable** (Motorola bus mode) This signal distinguishes between read and write operation.
86	$\overline{CS}$	I	**Chip Select** A low signal selects the QuadFALC for read/write operations.
46	RES	I	**Reset** A low signal on this pin forces the QuadFALC into reset state. During Reset the QuadFALC needs an active clock on pin MCLK. During Rese all bi-directional output stages (data bus) are in high-impedance state if signal $\overline{RD}$ is "high".

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
87	$\overline{\text{BHE}}/\overline{\text{BLE}}$	I	**Bus High Enable** (Siemens/Intel bus mode) If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the upper byte of the data bus (D8 … D15). In 8-bit bus interface mode this signal has no function and should be tied to V_{DD}. Refer to **chapter 7.2** for detailed information. **Bus Low Enable** (Motorola bus mode) If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the lower byte of the data bus (D0 … D7). In 8-bit bus interface mode this signal has no function and should be tied to V_{DD}. Refer to **chapter 7.2** for detailed information.
40	DBW	I	**Data Bus Width** (Bus Interface Mode) A low signal on this input selects the 8-bit bus interface mode. A high signal on this input selects the 16-bit bus interface mode. In this case word transfer to/from the internal registers is enabled. Byte transfers are implemented by using A0 and $\overline{\text{BHE}}/\overline{\text{BLE}}$.
41	INT	O/oD	**Interrupt Request** INT serves as general interrupt request which may include all interrupt sources. These interrupt sources can be masked via registers IMR0 … 5. Interrupt status is reported via registers GIS (Global Interrupt Status) and ISR0 … 5. Output characteristics (push-pull active low/high, open drain) are determined by programming the IPC register.
68	IM	I	**Interface Mode** The level at this pin defines the bus interface mode: A low signal on this input selects the INTEL interface mode. A high signal on this input selects the Motorola interface mode.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
115, 138, 43, 66	RL1(1-4)	I	**Line Receiver 1** Analog Input from the external transformer. Selected if LIM1.DRS = 0.
	RDIP(1-4)	I	**Receive Data Input Positive** Digital input for received dual rail PCM(+) route signal which will be latched with the internal generated Receive Route Clock. An internal DPLL will extract the Receive Route Clock from the incoming data pulse. The duty cycle of the receiving signal has to be closely to 50 %. The Dual Rail mode is selected if LIM1.DRS = 1 and FMR0.RC1 = 1. Input sense is selected by bit RC0.RDIS (after Reset: active low).
	ROID(1-4)	I	**Receive Optical Interface Data** Unipolar data received from fibre optical interface with 1.544 MBit/s. Latching of data is done with the falling edge of RCLKI. Input sense is selected by bit RC0.RDIS. The Single Rail mode is selected if LIM1.DRS = 1 and FMR0.RC1 = 0.
116, 137, 44, 65	RL2(1-4)	I	**Line Receiver 2** Analog Input from the external transformer. Selected if LIM1.DRS = 0.
	RDIN(1-4)	I	**Receive Data Input Negative** Input for received dual rail PCM(-) route signal which will be latched with the internal generated Receive Route Clock. An internal DPLL will extract the Receive Route Clock from the incoming data pulse. The duty cycle of the receiving signal has to be closely to 50 %. The dual rail mode is selected if LIM1.DRS = 1 and FMR0.RC1 = 1. Input sense is selected by bit RC0.RDIS (after Reset: active low).
	RCLKI(1-4)	I	**Receive Clock Input** Receive clock input for the optical interface if LIM1.DRS = 1 and FMR0.RC1/0 = 00. Clock frequency: 1544 kHz

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
42, 67, 114, 132, 139	V_{DDR}	I	**Positive Power Supply** for the analog receiver
45, 64, 117,135, 136	V_{SSR}	I	**Power Supply Ground** for the analog receiver
111, 142, 39, 70	XL2(1-4)	O	**Transmit Line 2** Analog output for the external transformer. Selected if LIM1.DRS = 0. After Reset this pin is in a high impedance state until register FMR0.XC1 is set to one.
	XDON(1-4)	O	**Transmit Data Output Negative** This digital output for transmitted dual rail PCM(-) route signals can provide – half bauded signals with 50% duty cycle (LIM0.XFB = 0) or – full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data will be clocked off on the positive transitions of XCLK in both cases. Output sense is selected by bit LIM0.XDOS (after Reset: active low). The dual rail mode is selected if LIM1.DRS = 1 and FMR0.XC1 = 1. After Reset this pin is in a high impedance state until register LIM1.DRS is set to one.
	XFM(1-4)	O	**Transmit Frame Marker** This digital output marks the first bit of every frame. This function is only available in the optical interface mode LIM1.DRS=1 and FMR0.XC1 = 0. The data will be clocked off on the positive transitions of XCLK. After Reset this pin is in a high impedance state until register LIM1.DRS is set to one. In remote loop configuration the XFM marker is not valid.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
109, 144, 37, 72	XL1(1-4)	O	**Transmit Line 1** Analog output for the external transformer. Selected if LIM1.DRS = 0. After Reset this pin is in a high impedance state until register FMR0.XC1 is set to one.
	XDOP(1-4)	O	**Transmit Data Output Positive** This digital output for transmitted dual rail PCM(+) route signals can provide – half bauded signals with 50% duty cycle (LIM0.XFB = 0) or – full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data will be clocked off on the positive transitions of XCLK in both cases. Output sense is selected by bit LIM0.XDOS (after Reset: active low). The dual rail mode is selected if LIM1.DRS = 1 and FMR0.XC1 = 1. After Reset this pin is in a high impedance state until register LIM1.DRS is set to one.
	XOID(1-4)	O	**Transmit Optical Interface Data** Unipolar data sent to fibre optical interface with 1.544 MBit/s which will be clocked off on the positive transitions of XCLK. Clocking off data in NRZ code is done with 100 % duty cycle. Data in CMI code are shifted out with 50 % or 100 % duty cycle according to the CMI coding. Output sense is selected by bit LIM0.XDOS (after Reset: data is sent active high). The single rail mode is selected if LIM1.DRS = 1 and FMR0.XC1 = 0. After Reset this pin is in a high impedance state until register LIM1.DRS is set to one.
38, 71, 110, 143	VDDX	I	**Positive Power Supply** for analog transmitter
1, 36, 73, 108	V_{SSX}	I	**Power Supply Ground** for analog transmitter

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
133	MCLK	I	**Reference Clock 1.544 MHz** A reference clock of 1.544 MHz +/- 50 ppm must be provided to this pin.
134	NC		**Not connected**
48	SYNC	I + PU	**Clock Synchronization** If a clock is detected at the SYNC pin the DCO-Rs of the QuadFALC synchronizes to this clock 1.544 MHz or 2.048 MHz (if LIM1.DCOC = 1). This pin has an integrated pull up resistor.
69	SEC	I +PU	**Second Timer Input** A pulse with logical one for at least two 1.544 MHz cycles will trigger the internal second timer.
	FSC	O	Enabled with GPC1.FSS2-0 an **8-kHz Frame Synchronization Pulse** is output via this pin. The synchronization pulse is active high / low for one 1.544 / 2.048 MHz cycle (pulse width = 648 / 488 ns).
	SEC	O	**Second Timer Output** Activated high every second for two 1.544 MHz clock cycles. Enabled with GPC1.CSFP1-0.
119, 130, 47, 61	RCLK(1-4)	I/O+PU	**Receive Clock** After Reset this port is configured to an input. Setting of bit PC5.CRPwill switch this port to an output. Input function not defined. Output function: CMR1.RS1/0 = 00: Receive Clock extracted from the incoming data pulses. Frequency: 1544 kHz CMR1.RS1/0 = 01: RCLK is set high in case of loss of signal (FRS0.LOS=1). Optional one of the dejittered system clocks sourced by DCO-R is clocked out. Clock frequency: 1544 / 6176 or 2048 / 8192 kHz. Selected by CMR1.RS1/0=11. Wih GPC1.R1S1/0 one of the four RCLK(1-4) is output on RCLK1.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
8, 13, 26, 31	SCLKR (1-4)	I/O + PU	**System Clock Receive** Working clock for the receive system interface with a frequency of 16.384 / 8.192 / 4.096 / 2.048 or 12.352 /6.176 / 3.088 / 1.544 MHz. If the receive elastic store is bypassed SIC1.RBS1/0 the clock supplied on this pin is ignored. If SCLKR is configured to an output, the internal working clock of the receive system interface sourced by DCO-R or RCLK is output. In system interface multiplex mode a 16.384 / 12.352 or 8.192 / 6.176 MHz clock has to be provided on SCLKR1, which is a common clock for all 4 rec. system interfaces.
9, 12, 27, 30	RDO(1-4)	O	**Receive Data Out** Received data which is sent to the system highway. Clocking off data is done with the rising or falling edge (SIC3.RESR) of SCLKR(1-4) or RCLK(1-4), if the receive elastic store is bypassed. The delay between the beginning of time-slot 0 and the initial edge of SCLKR(1-4) (after $\overline{\text{SYPR}}$ goes active) is determined by the values of registers RC1 and RC0. If received data is shifted out with higher data, the active channel phase is defined by bits SIC2.SICS2-0. In system interface multiplex mode all 4 received datastreams are merged into a single datastream byte or bit interleaved on RDO1.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
4 -7, 14 -17, 22 - 25, 32 - 35	RP(A-D)1 RP(A-D)2 RP(A-D)3 RP(A-D)4	I/O + PU	**Receive Multifunction Port A-D** Depending on programming of bits PC(1-4).RPC(2-0) this multifunction ports carries information to the system interface or from the system to the QuadFALC. After Reset these ports are configured to be inputs. With the selection of the pinfunction the in/output configuration is also achieved. Depending on bit SIC3.RESR all outputs / inputs of the receive system interface are updated / sampled with the rising or falling edge of SCLKR.
		I + PU	**Synchronous Pulse Receive ($\overline{\text{SYPR}}$)** Enabled with PC(1-4).RPC(2-0) = 000 (reset configuration). Defines the beginning of time-slot 0 at system highway port RDO in conjunction with the values of registers RC0/1. In system interface multiplex mode $\overline{\text{SYPR}}$ has to be provided at port RPA1 for all 4 channels and defines the beginning of time-slot 0 on port RDO1/RSIG1. Pulse Cycle: Integer multiple of 125 µs.
		O	**Receive Frame Marker (RFM)** Enabled with PC(1-4).RPC(2-0) = 001. CMR2.IRSP = 0: The receive frame marker could be active high for a 1.544 / 2.048 MHz period during any bit position of the current frame. IProgramming is done with registers RC1/0. CMR2.IRSP = 1: Internal generated frame synchronization pulse generated by the DCO-R circuitry. Together with registers RC1/0 the frame begin on the receive system interface is defined. This frame synchronization pulse is active low 1.544 / 2.048 MHz period.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
4 -7, 14 -17, 22 - 25, 32 - 35	RP(A-D)1 RP(A-D)2 RP(A-D)3 RP(A-D)4	O	**Receive Multiframe Begin (RMFB)** Enabled with PC(1-4).RPC(2-0) = 010. The function depends on programming bit XC0.MFBS: MFBS = 1: RMFB marks the beginning of every received multiframe (RDO). MFBS = 0: Marks the beginning of every received superframe. Additional pulses every 12 frames are provided when using ESF or F72 format.
		O	**Receive Signaling Marker (RSIGM)** Enabled with PC(1-4).RPC(2-0) = 011. – Marks the time-slots which are defined by register RTR1-4 of every received frame on port RDO. – When using the CAS-BR signaling scheme (bit XC0.BRM = 1), the robbed bit of each channel every six frames is marked, if it is enabled via register XC0.BRM = 1.
		O	**Receive Signaling Data (RSIG)** Enabled with PC(1-4).RPC(2-0) = 100. The received CAS signaling data is sourced by this pin. Time-slots on RSIG correlates directly to the time-slot assignment on RDO. In system interface multiplex mode all four received signaling datastreams are merged into a single datastream byte or bit interleaved and is transmitted on port RPB1.
		O	**Data Link Bit Receive (DLR)** Enabled with PC(1-4).RPC(2-0) = 101. Marks the DL-bit position within the data stream on RDO.
		O	**Freeze Signaling (FREEZE)** Enabled with PC(1-4).RPC(2-0) = 110. The freeze signaling status is active high by detecting a Loss of Signal alarm, or a Loss of Frame Alignment or a receive slip (pos. or neg.). It will hold high for at least one complete multiframe after the alarm disappears. Setting SIC2.FFS enforces a high on pin FREEZE.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
4 -7, 14 -17, 22 - 25, 32 - 35	RP(A-D)1 RP(A-D)2 RP(A-D)3 RP(A-D)4	O	**Receive Frame Synchronous Pulse ($\overline{\text{RFSP}}$)** Enabled with PC(1-4).RPC(2-0) = 111. Active low framing pulse derived from the received PCM route signal. During loss of synchronization (bit FRS0.LFA), this pulse is suppressed (not influenced during alarm simulation). Pulse frequency: 8 kHz, Pulse width: 648 ns
3, 19, 21, 50	SCLKX (1-4)	I/O + PU	**System Clock Transmit** Working clock for the transmit system interface with a frequency of 16.384 / 8.192 / 4.096 / 2.048 or 12.352 /6.176 / 3.088 / 1.544 MHz. In system interface multiplex mode a 16.384 /12.352 or 8.192 / 6.176 MHz clock has to be provided on SCLKX1, which is a common clock for all 4 transmit system interfaces.
2, 18, 20, 49	XDI(1-4)	I	**Transmit Data In** Transmit data received from the system highway. Latching of data is done with rising or falling transitions of SCLKX according to bit SIC3.RESX. The delay between the beginning of time-slot 0 and the initial edge of SCLKX (after $\overline{\text{SYPX}}$ goes active) is determined by the registers XC1/0. In system interface multiplex mode latching of datastream containing the 4 frames is done byte or bit interleaved on port XDI1. In higher data rates sampling of data is defined by bits SIC2.SICS2-0.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
120 - 123 126 - 129 51 - 54 57 - 60	XP(A-D)1 XP(A-D)2 XP(A-D)3 XP(A-D)4	I/O + PU	**Transmit Multifunction Port A-D** Depending on programming of bits PC(1-4).XPC(2-0) this multifunction ports carries information to the system interface or from the system to the QuadFALC. After Reset these ports are configured to inputs. With the selection of the pinfunction the in/output configuration is also achieved. Depending on bit SIC3.RESX all outputs / inputs of the transmit system interface are updated / sampled with the rising or falling edge of SCLKX.
		I + PU	**Synchronous Pulse Transmit ($\overline{SYPX}$)** Defines the beginning of time-slot 0 at system highway port XDI in conjunction with the values of registers XC0/1. In system interface multiplex mode $\overline{SYPX}$ has to be provided at port XPA1 for all 4 channels and defines the beginning of time-slot 0 on port XDI1/XSIG1. Enabled with PC(1-4).XPC(2-0) = 000 (reset configuration). Pulse Cycle: Integer multiple of 125 µs.
		I + PU	**Transmit Multiframe Synchronization (XMFS)** Enabled with PC(1-4).XPC(2-0) = 001 this port defines the frame and multiframe begin on the transmit system interface ports XDI and XSIG. Depending on PC5.CXMFS the signal on XMFS is active high or low. For correct operation of XMFS no $\overline{SYPX}$ pin function should be selected for the remaining multifunction ports of the same channel. In system interface multiplex mode XMFS has to be provided at port XPB1 for all 4 channels. ***Note:*** *A new multiframe position has been settled at least one multiframe after pulse XMFS has been supplied.*

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
120 - 123 126 - 129 51 - 54 57 - 60	XP(A-D)1 XP(A-D)2 XP(A-D)3 XP(A-D)4	I + PU	**Transmit Signaling Data (XSIG)** Enabled with PC(1-4).XPC(2-0) = 010. Input for transmit signaling data received from the signaling highway. Optionally (SIC3.TTRF) sampling of XSIG data is controlled by the active high XSIGM marker. In higher data rates sampling of data is defined by bits SIC2.SICS2-0. In system interface multiplex mode latching of the datastream containing the 4 signaling multiframes is done byte or bit interleaved on port XPC1.
		I +PU	**Transmit Clock (TCLK)** Enabled with PC(1-4).XPC(2-0) = 011. A 1.544 / 6.176 MHz clock has to be sourced by the system if the internal generated transmit clock (DCO-X) should not be used. Optional this input functions as a clock synchronization for the DCO-X circuitry with a frequency of 1.544 MHz.
		O	**Transmit Multiframe Begin (XMFB)** Enabled with PC(1-4).XPC(2-0) = 100. The function depends on programming bit XC0.MFBS MFBS = 1: XMFB marks the beginning of every transmitted multiframe (XDI). MFBS = 0: Marks the beginning of every transmitted superframe. Additional pulses every 12 frames are provided when using ESF or F72 format. XMFB is active high for one 2.048 or 1.544 MBit/s period.
		O	**Transmit Signaling Marker (XSIGM)** Enabled with PC(1-4).XPC(2-0) = 101. – Marks the transmit time-slots which are defined by register TTR1-4 of every frame transmitted via port XDI. – When using the CAS-BR signaling scheme, the robbed bit of each channel every six frames is marked, if it is enabled via register XC0.BRM = 1.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
120 - 123 126 - 129 51 - 54 57 - 60	XP(A-D)1 XP(A-D)2 XP(A-D)3 XP(A-D)4	O O	**Data Link Bit Transmit (DLX)** Enabled with PC(1-4).XPC(2-0) = 110. This output provides a 4 kHz signal which marks the DL-bit position within the data stream on XDI. **Transmit Clock (XCLK)** Enabled with PC(1-4).XPC(2-0) = 111. Transmit line clock, frequency: 1.544 MHz. Derived from SCLKX/R, RCLK or internally generated by the DCO-X circuitry.
11, 29, 56, 92, 102, 125,	V_{SS}	I	**Power Ground** Supply for digital subcircuits (0 V) For correct operation, all six pins have to be connected to ground.
10, 28, 55, 91, 101, 124,	V_{DD}	I	**Positive Power Supply** for the digital subcircuits (3.3 V) For correct operation, all six pins have to be connected to positive power supply.
112	TDI	I + PU	**Test Data Input** for JTAG Boundary Scan acc. to IEEE Std. 1149.1
113	TDO	O	**Test Data Output** for Boundary Scan
141	TMS	I + PU	**Test Mode Select** for Boundary Scan
140	TCK	I + PU	**Test Clock** for Boundary Scan
131	$\overline{\text{TRS}}$	I + PU	**Test Reset** for Boundary Scan (active low) If the JTAG Boundary Scan is not used this pin can be connected to pin $\overline{\text{RES}}$ or VSS.
63, 118	RSVD	I/O + PU	Reserved

7 Functional Description T1 / J1

7.1 Functional Block Diagram

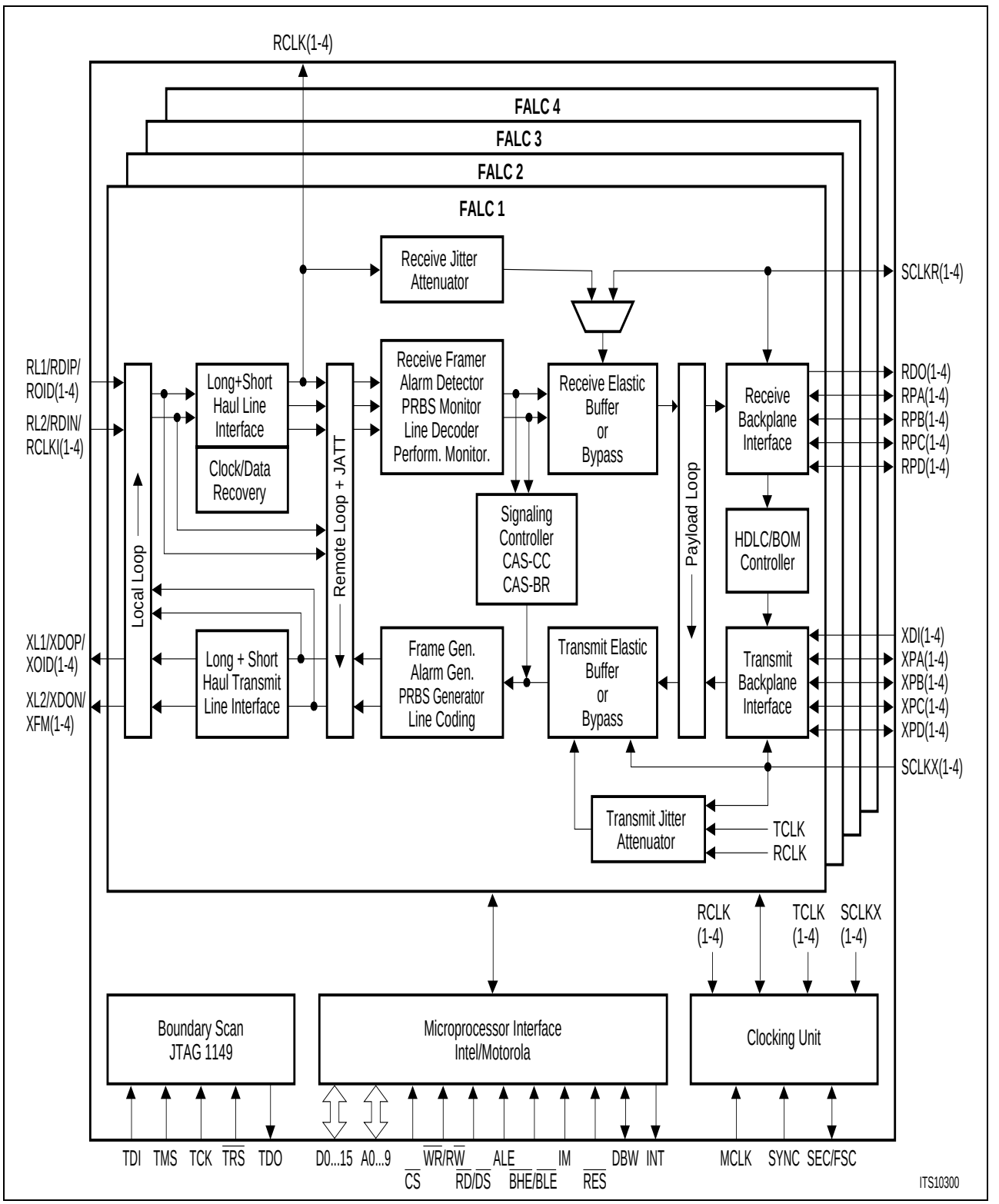


Figure 38 Functional Block Diagram PEB 22554

7.2 Microprocessor Interface

The communication between the CPU and the QuadFALC is done via a set of directly accessible registers. The interface may be configured as Siemens/Intel or Motorola type with a selectable data bus width of 8 or 16 bits.

The CPU transfers data to/from the QuadFALC (via 64 byte deep FIFOs per direction and channel), sets the operating modes, controls function sequences, and gets status information by writing or reading control/status registers. All accesses can be done as byte or word accesses if enabled. If 16-bit bus width is selected, access to lower/upper part of the data bus is determined by address line A0 and signal $\overline{BHE}$/$\overline{BLE}$ as shown in **table 13** and **14**.

In **table chapter Table 15** is shown how the ALE (address latch enable) line is used to control the bus structure and interface type. The switching of ALE allows the QuadFALC to be directly connected to a multiplexed address/data bus.

Mixed Byte/Word Access to the FIFOs

Reading from or writing to the internal FIFOs (RFIFO and XFIFO of each channel) can be done using a 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. Randomly mixed byte/word access to the FIFOs is allowed without any restrictions.

Table 13
Data Bus Access (16-Bit Intel Mode)

$\overline{BHE}$	A0	Register Access	QuadFALC Data Pins Used
0	0	FIFO word access Register word access (even addresses)	D0 – D15
0	1	Register byte access (odd addresses)	D8 – D15
1	0	Register byte access (even addresses)	D0 – D7
1	1	No transfer performed	None

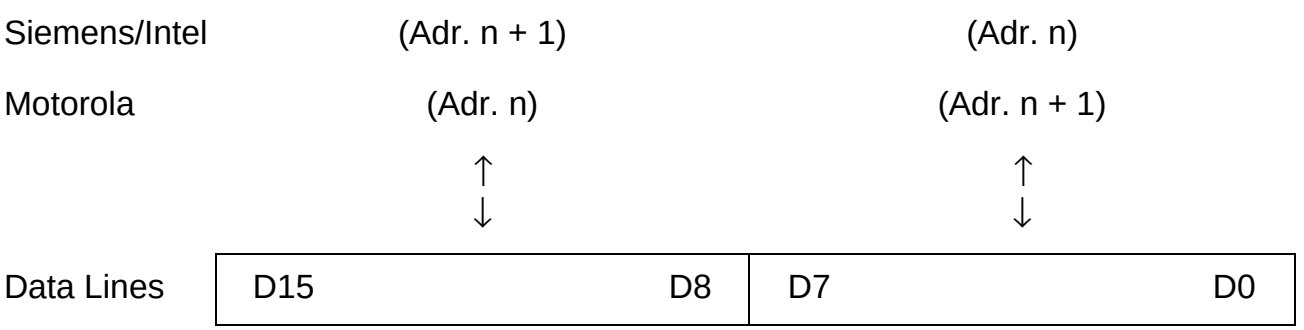
Table 14
Data Bus Access (16-Bit Motorola Mode)

$\overline{\text{BLE}}$	A0	Register Access	QuadFALC Data Pins Used
0	0	FIFO word access Register word access (even addresses)	D0 – D15
0	1	Register byte access (odd addresses)	D0 – D7
1	0	Register byte access (even addresses)	D8 – D15
1	1	No transfer performed	None

Table 15
Selectable Bus and Microprocessor Interface Configuration

ALE	IM	Microprocessor Interface	Bus Structure
GND/VDD	1	Motorola	demultiplexed
GND/VDD	0	Intel	demultiplexed
switching	0	Intel	multiplexed

The assignment of registers with even/odd addresses to the data lines in case of 16-bit register access depends on the selected microprocessor interface mode:



n: even address

Complete information concerning register functions is provided in – Detailed Register Description.

FIFO Structure

In transmit and receive direction of the signaling controller 64-byte deep FIFOs for each channel are provided for the intermediate storage of data between the system internal highway and the CPU interface. The FIFOs are divided into two halves of 32-bytes. Only one half is accessible to the CPU at any time.

In case 16-bit data bus width is selected by fixing pin DBW to logical ‘1’ word access to the FIFOs is enabled. Data output to bus lines D0-D15 as a function of the selected interface mode is shown in **figure 39** and **40**. Of course, byte access is also allowed.The effective length of the accessible part of RFIFO may be changed from 32 bytes (RESET value) down to 2 bytes independent for each channel.

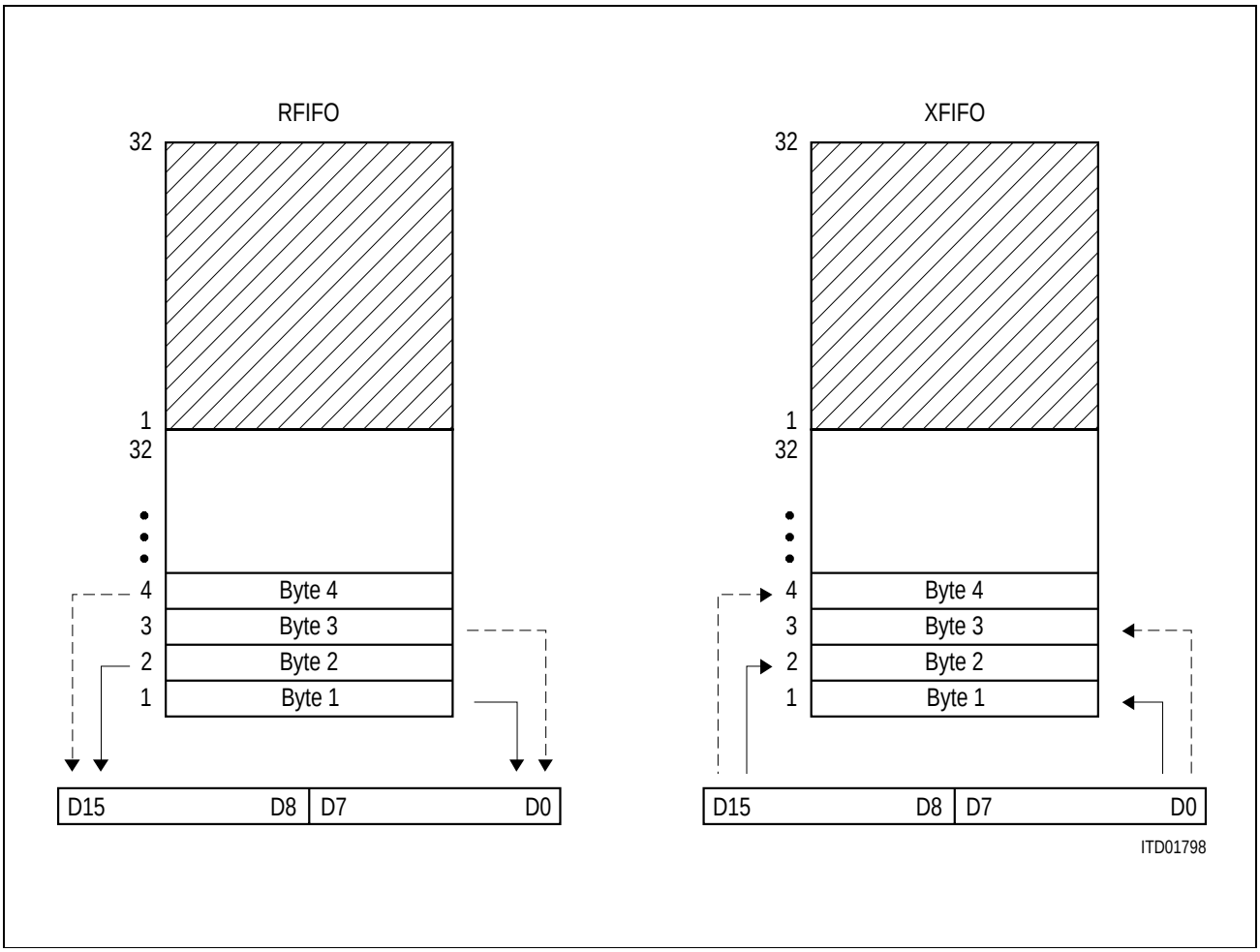


Figure 39
FIFO Word Access (Intel Mode)

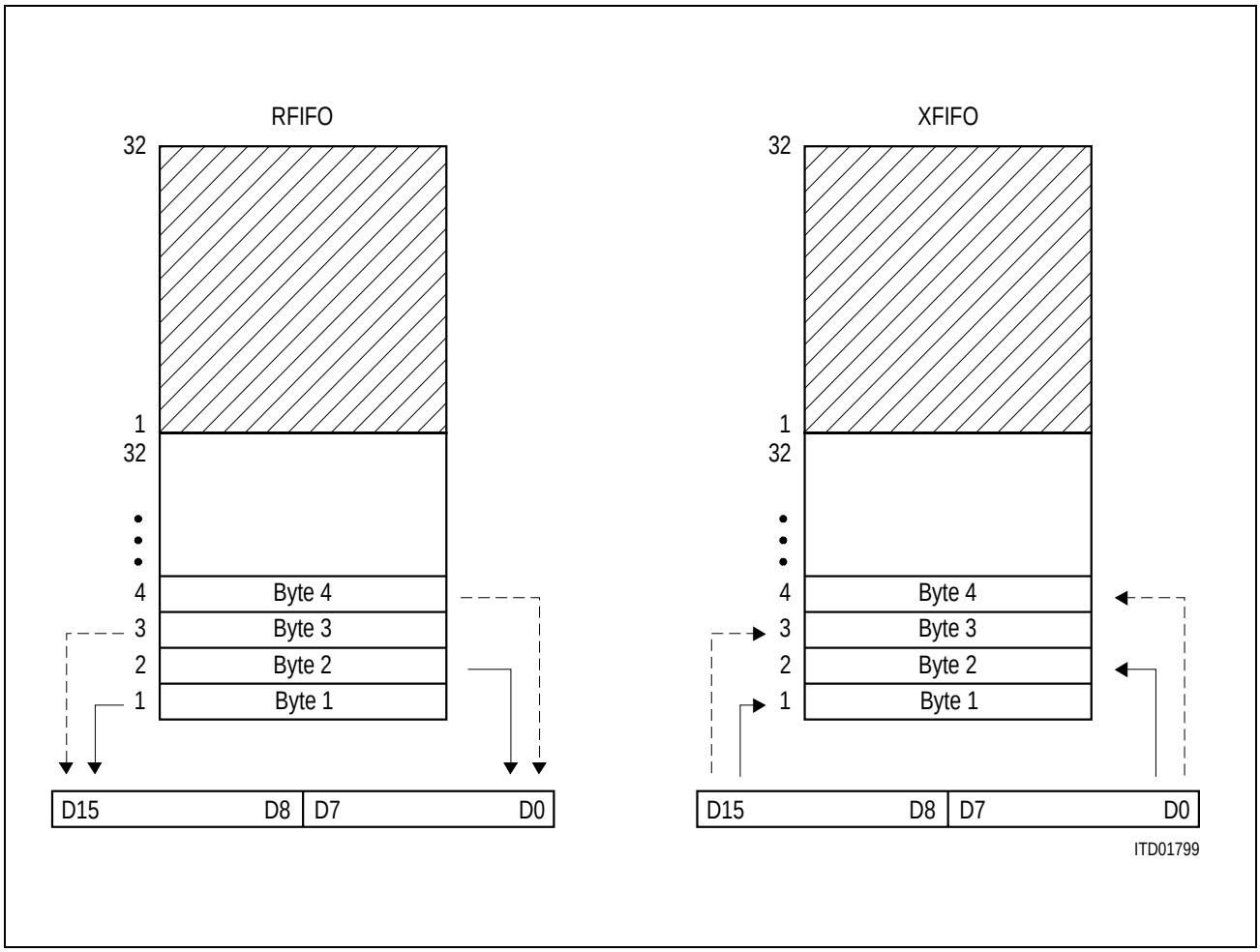


Figure 40
FIFO Word Access (Motorola Mode)

Interrupt Interface

Special events in the QuadFALC are indicated by means of a single interrupt output with programmable characteristics (open drain, push-pull; IPC register), which requests the CPU to read status information from the QuadFALC, or to transfer data from/to QuadFALC.

Since only one INT request output is provided, the cause of an interrupt must be determined by the CPU by reading the QuadFALC's interrupt status registers (CIS, GIS, ISR0-4) that means the interrupt on pin INT and the interrupt status bits are reset by reading the interrupt status registers. Register ISR0-4 are from type "Clear on Read".

The structure of the interrupt status registers is shown in **figure 41**.

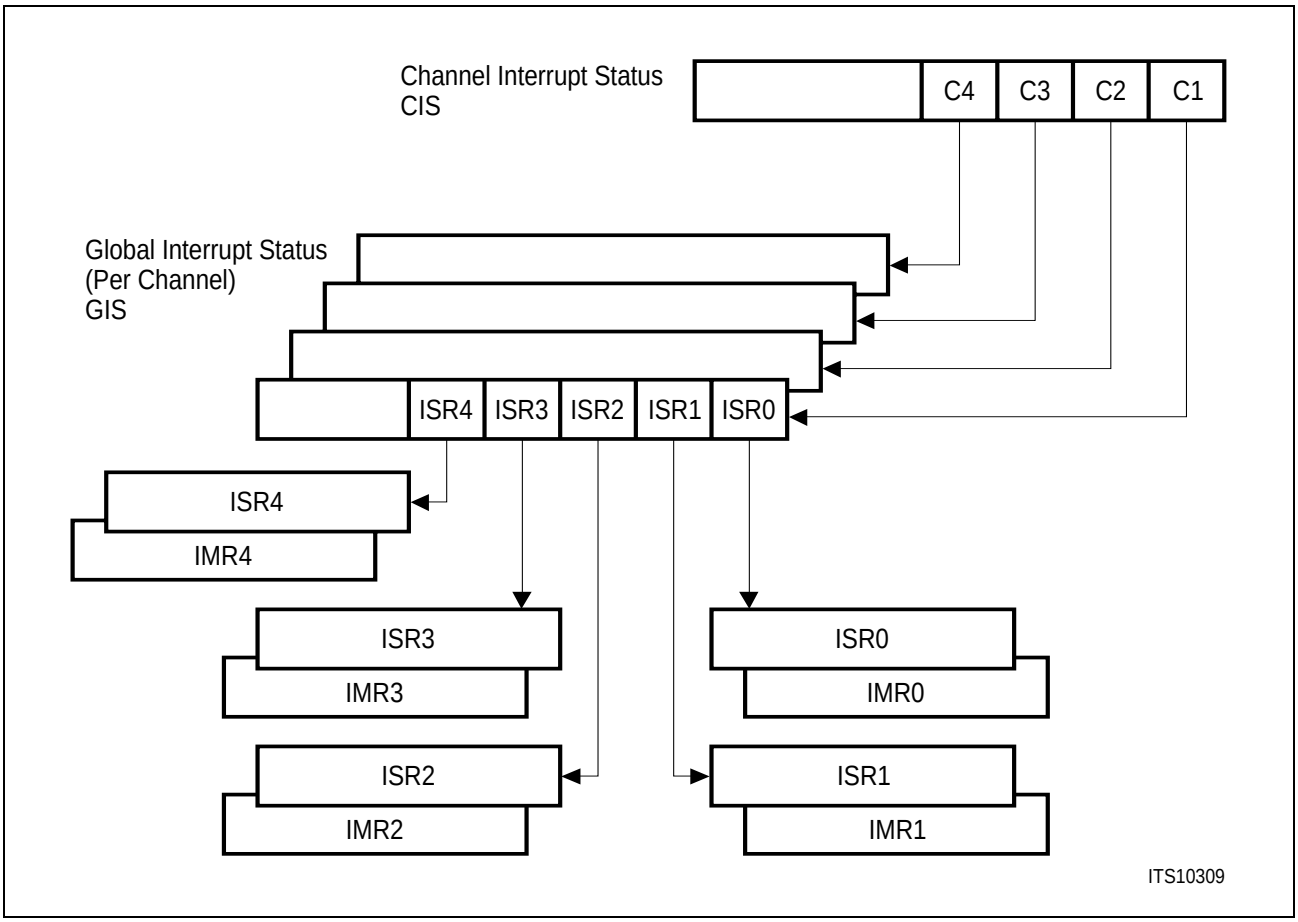


Figure 41
QuadFALC Interrupt Status Register Structure

Each interrupt indication of registers ISR0-4 can be selectively masked by setting the corresponding bit in the corresponding mask registers IMR0-4. If the interrupt status bits are masked, they neither generate an interrupt at INT nor are they visible in ISR0-4.

CIS, the non-maskable Channel Interrupt Status Register, serves as a pointer to pending channel related global interrupt status registers. After the QuadFALC has requested an interrupt by activating its INT pin, the CPU should first read the Channel Interrupt Status

register CIS to identify the requesting channel. The global interrupt status register serves itself as a pointer to pending interrupt status registers ISR0 -4 for each channel. After reading the assigned global interrupt status register and the assigned interrupt status registers ISR0- 4, the pointer in the GIS and CIS registers are cleared or updated if another interrupt requires service.

If **all** pending interrupts are acknowledged by reading (CIS and GIS are reset), pin INT goes inactive.

Updating of interrupt status registers ISR0…4 , GIS and CIS is only prohibited during read access.

Masked Interrupts Visible in Status Registers

The channel and global interrupt status registers indicates those interrupt status registers with active interrupt indications.

An additional mode may be selected via bit GCR.VIS.

In this mode, masked interrupt status bits neither generate an interrupt on pin INT nor are they visible in CIS and GIS, **but are displayed in the respective interrupt status register(s) ISR0..4**.

This mode is useful when some interrupt status bits are to be polled in the individual interrupt status registers.

Notes:

- *In the visible mode, all active interrupt status bits, whether the corresponding actual interrupt is masked or not, are reset when the interrupt status register is read. Thus, when polling of some interrupt status bits is desired, care must be taken that unmasked interrupts are not lost in the process.*
- *All unmasked interrupt statuses are treated as before.*

Please note that whenever polling is used, all interrupt status registers concerned have to be polled individually (no “hierarchical” polling possible), since GIS only contains information on actually generated - i.e. unmasked-interrupts.

7.3 Boundary Scan Interface

Identification Register:	32 bit
Version:	1_H
Part Number:	$004D_H$
Manufacturer:	083 H

In QuadFALC a Test Access Port (TAP) controller is implemented. The essential part of the TAP is a finite state machine (16 states) controlling the different operational modes

of the boundary scan. Both, TAP controller and boundary scan, meet the requirements given by the JTAG standard: IEEE 1149.1. **Figure 42** gives an overview.

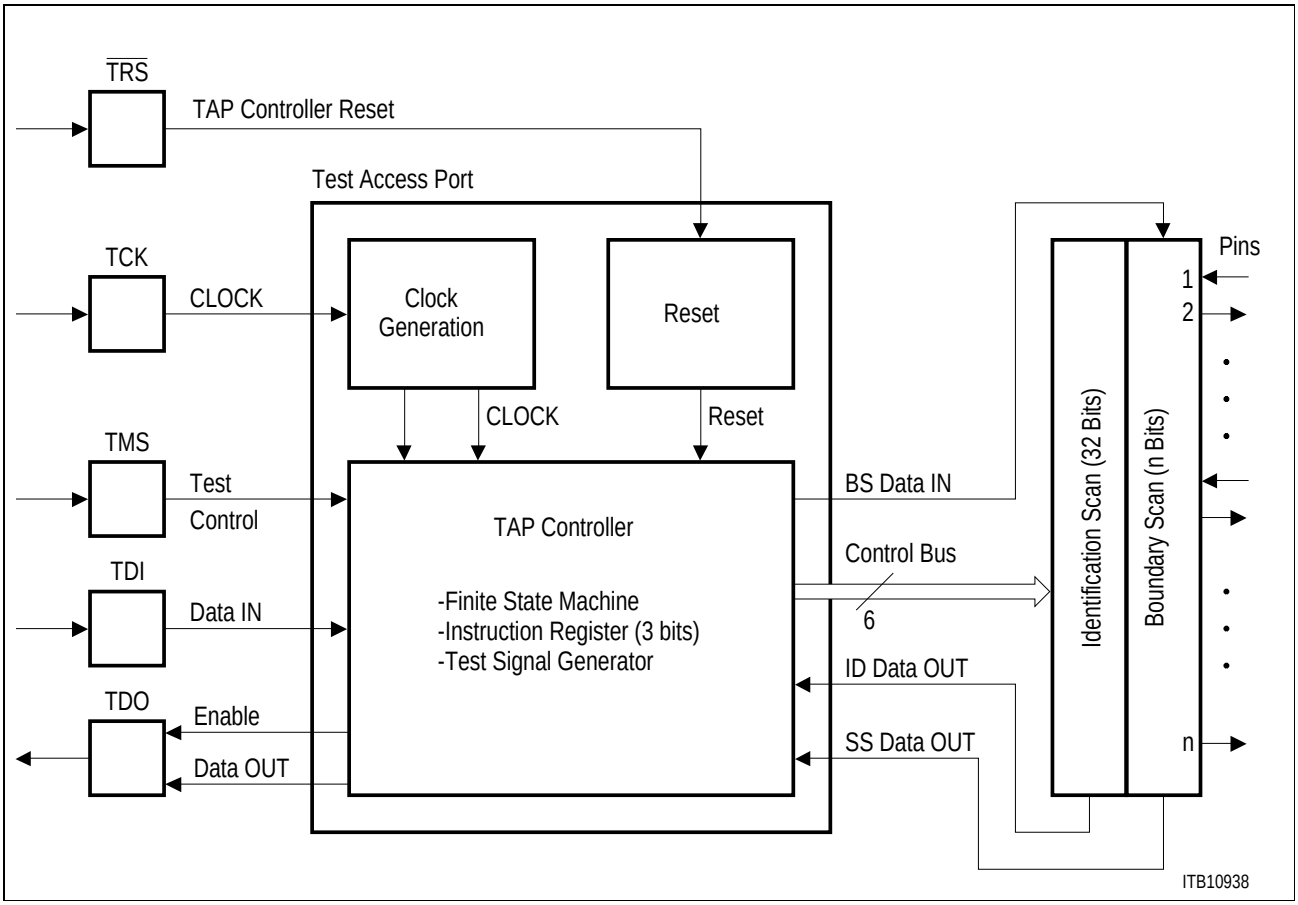


Figure 42
Block Diagram of Test Access Port and Boundary Scan

Test handling is performed via the pins TCK (Test Clock), TMS (Test Mode Select), TDI (Test Data Input) and TDO (Test Data Output). Test data at TDI are loaded with a 4-MHz clock signal connected to TCK. ‘1’ or ‘0’ on TMS causes a transition from one controller state to an other; constant ’1’ on TMS leads to normal operation of the chip.

If no boundary scan testing is planned TMS and TDI do not need to be connected since pull-up transistors ensure high input levels in this case. Nevertheless it would be a good practice to put the unused inputs to defined levels. In this case, if the JTAG is not used: TMS = TCK = ‘1’.

After switching on the device (V_{DD} = 0 to 3.3 V) pin $\overline{\text{TRS}}$ has to reset which forces the TAP controller into test logic reset state.

7.4 Receive Path

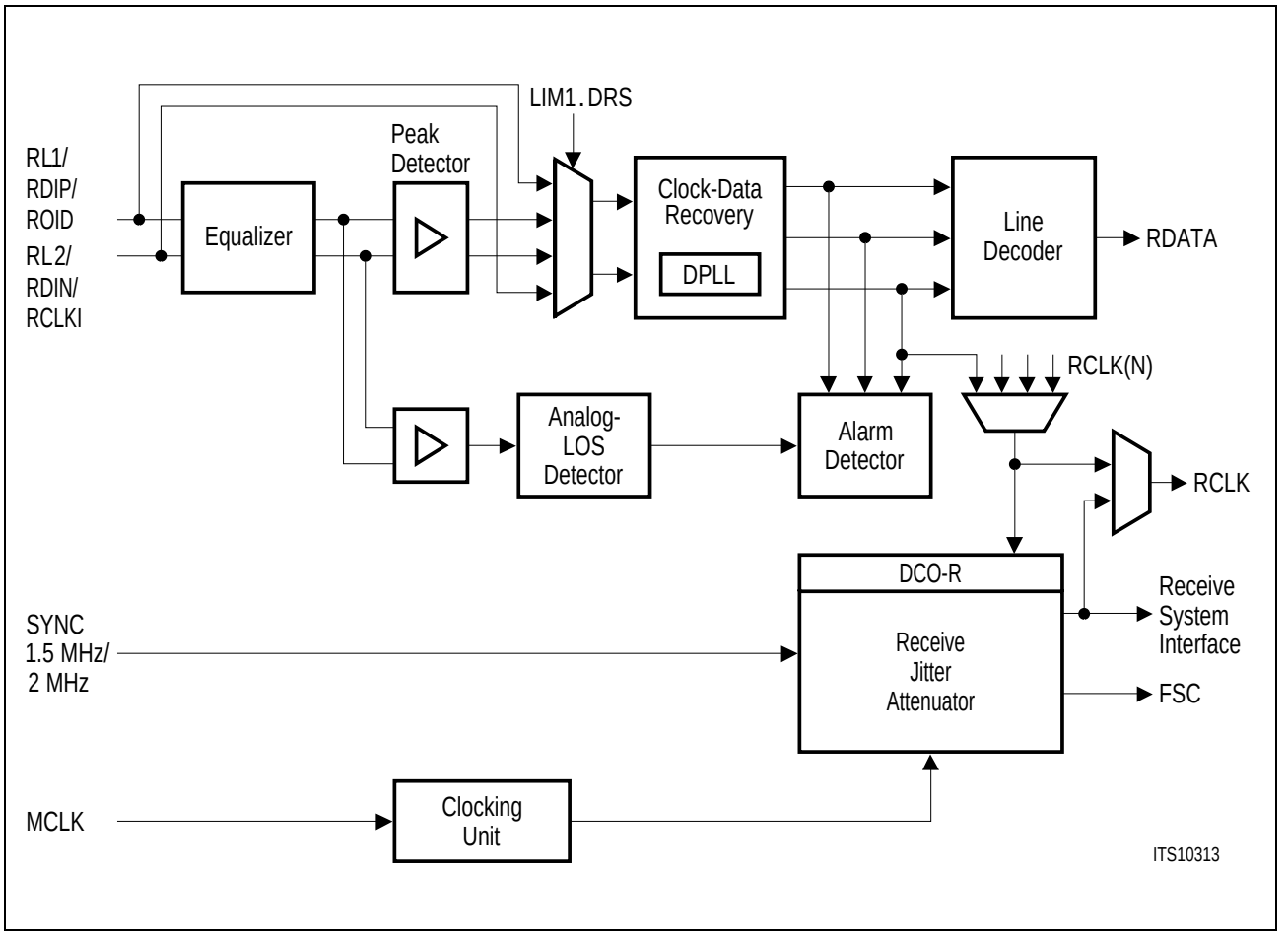


Figure 43
Receive Clock System

Receive Line Interface

For data input, three different data types are supported:

- Ternary coded signals received at multifunction ports RL1 and RL2 from a -36 dB ternary interface. The ternary interface is selected if LIM1.DRS is reset.
- Digital dual rail signals received at ports RDIP and RDIN. The dual rail interface is selected if LIM1.DRS and FMR0.RC1 is set.
- Unipolar data at port ROID received from a fibre optical interface. The optical interface is selected if LIM1.DRS is set and FMR0.RC1 is reset.

Receive Short and Long Haul Interface

The QuadFALC has now an integrated short- and long- haul line interface, comprising a receive equalization network, noise filtering and programmable line build-outs (LBO).

Receive Equalization Network

The QuadFALC automatically recovers the signals received on pins RL1/2 in a range of up to -36 dB. The maximum reachable length with a 22 AWG twisted-pair cable is 2000 m. After Reset the QuadFALC is in „Short Haul“ mode, received signals are recovered up to -10 dB of cable attenuation. Switching in „Long Haul“ mode is done by setting of register LIM0.EQON.
The integrated receive equalization network recovers signals with up to -36 dB of cable attenuation. Noise filters eliminate the higher frequency part of the received signals. The incoming data is peak detected and sliced at 55% of the peak value to produce the digital data stream. The received data is then forwarded to the clock & data recovery unit.

Receive Line Attenuation Indication

Status register RES reports the current receive line attenuation in a range from 0 to -36 dB in 25 steps of approximately 1.4 dB each. The least significant 5 bits of this register indicate the cable attenuation in dB. These 5 bits are only valid in conjunction with the most significant two bits (RES.EV1/0 = 01) .

Receive Clock and Data Recovery

The analog received signal at port RL1/2 is equalized and then peak-detected to produce a digital signal. The digital received signal at port RDIP/N is directly forwarded to the DPLL. The receive clock and data recovery extracts the route clock RCLK from the data stream received at the RL1/2, RDIP/RDIN or ROID lines and converts the data stream into a single rail, unipolar bit stream. The clock and data recovery works with the internally generated high frequency clock based on MCLK. Normally the clock that is output via pin RCLK is the recovered clock from the signal provided by RL1/2 or RDIP/N has a duty cycle close to 50 %. The free run frequency is defined by MCLK = 1.544 MHz in periods with no signal. The intrinsic jitter generated in the absence of any input jitter is not more than 0.035 UI. In digital bipolar line interface mode the clock and data recovery will accept only HDB3 coded signals with 50 % duty cycle.

Receive Line Coding

The B8ZS line code or the AMI (ZCS) coding is provided for the data received from the ternary or the dual rail interface. All code violations that do not correspond to zero substitution rules will be detected. The detected errors increment the code violation counter (16 bits length). In case of the optical interface a selection between the NRZ code and the CMI Code (1T2B) with B8ZS postprocessing is provided. If CMI code (1T2B) is selected the receive route clock will be recovered from the data stream. The 1T2B decoder does not correct any errors. In case of NRZ coding data will be latched with the falling edge of pin RCLKI.

The detected errors increment the code violation counter (16 bits length).

When using the optical interface with NRZ coding, the decoder is by-passed and no code violations will be detected.

Additionally, the receive line interface contains the alarm detection for Alarm Indication Signal AIS (Blue Alarm) and the Loss of Signal LOS (Red Alarm).

The signal at the ternary interface is received at both ends of a transformer.

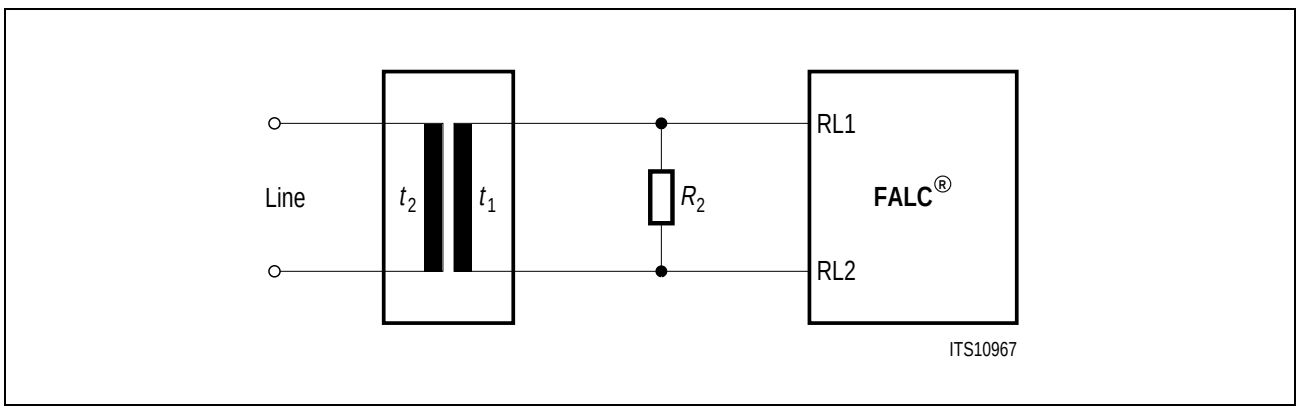


Figure 44
Receiver Configuration

Table 16
Recommended Receiver Configuration Values

Parameter	Characteristic Impedance 100 Ω
	DS1
R_1 (± 1 %) [Ω]	100
$t_2 : t_1$	1 : 1

Loss of Signal Detection

There are different definitions for detecting Loss of Signal alarms (LOS) in the ITU-T G.775 and AT&T TR 54016. The QuadFALC covers all these standards. The LOS indication is performed by generating an interrupt (if not masked) and activating a status bit. Additionally a LOS status change interrupt is programmable via register GCR.SCI.

- Detection:
  An alarm will be generated if the incoming data stream has no pulses (no transitions) for a certain number (N) of consecutive pulse periods. “No pulse” in the digital receive interface means a logical zero on pins RDIP/RDIN/ROID. A pulse with an amplitude less than Q dB below nominal is the criteria for “no pulse” in the analog receive interface (LIM1.DRS=0). The receive signal level Q is programmable via three control bits LIM1.RIL2-0 in a range of about 900 to 50 mV differential voltage between pins RL1/2. The number N may be set via a 8 bit register PCD. The contents of the PCD register will be multiplied by 16, which results in the number of pulse periods, or better,

the time which has to suspend until the alarm has to be detected. The range results therefore from 16 to 4096 pulse periods.

- Recovery:
  In general the recovery procedure starts after detecting a logical ‘one’ (digital receive interface) or a pulse (analog receive interface) with an amplitude more than Q dB (defined by LIM1.RIL2-0) of the nominal pulse. The value in the 8 bit register PCR defines the number of pulses (1 to 255) to clear the LOS alarm. Additional recovery conditions may be programmed by register LIM2.

Receive Jitter Attenuator

The receive jitter attenuator is placed for each channel in the receive path. The working clock is an internally generated high frequency clock based on the clock provided on pin MCLK (1.544 MHz). The jitter attenuator meets the requirements of PUB 62411, PUB 43802, TR-TSY 009,TR-TSY 253, TR-TSY 499 and Rec. I.431, G.703 and G. 824.

The internal PLL circuitry DCO-R generates an „jitterfree“ output clock which is directly dependent on the phase difference of the incoming clock and the jitter attenuated clock.The receive jitter attenuator could be either synchronized to the extracted receive clock RCLK or to a 1.544 or 2.048 MHz clock provided on pin SYNC. The received data is written into the receive elastic buffer with RCLK and are read out with the dejittered clock sourced by DCO-R. The jitter attenuated clock could be output via pins RCLK or SCLKR. Optionally a 8 kHz clock is provided on pin SEC/FSC.

The DCO-R circuitry attenuates the incoming jittered clock starting at 6 Hz jitter frequency with 20 dB per decade fall off. Wander with a jitter frequency below 6 Hz will be passed unattenuated. The intrinsic jitter in the absence of any input jitter is < 0.02UI.

For some applications it might be useful starting of jitter attenuation at lower frequencies. Therefore the corner frequency is switchable by the factor of ten downto 0.6 Hz (LIM2.SCF).

The DCO-R circuitry is automatically centered to the nominal bit rate if the reference clock on pin SYNC / RCLK is missed for two 2.048 or 1.544 MHz clock periods. This center function of DCO-R may be optionally disabled (CMR2.DCF = 1) in order to accept a gapped reference clock.

In analog line interface mode the RCLK is always running. Only in digital line interface mode with single rail data (NRZ) a gapped clock on pin RCLK may occur.

The receive jitter attenuator works in two different modes:

- Slave mode
  In Slave mode (LIM0.MAS = 0) the DCO1 will be synchronized to the recovered route clock. In case of LOS the DCO-R switches automatically to Master mode. If bit CMR1.DCS is set automatic switching from RCLK to SYNC is disabled.
- Master mode
  In Master mode (LIM0.MAS = 1) the jitter attenuator is in free running mode if on pin SYNC no clock is supplied. If a clock with a frequency of 1.544 MHz (LIM1.DCOC = 0) or 2.048 MHz (LIM1.DCOC = 1) is applied at the SYNC input the DCO-R will synchronize to this input.

The following table shows the clock modes with the corresponding synchronization sources.

Mode	Internal LOS Active	SYNC Input	System Clocks
Master	independent	Fixed to VDD	DCO-R centered, if CMR2.DCF =0. (CMR2.DCF should not be set)
Master	independent	1.544 or 2.048 MHz	Synchronized on SYNC input (external 1.544 or 2.048MHz)
Slave	no	Fixed to VDD	Synchronized on Line RCLK1-4 , selected by CMR1.DRSS1/0
Slave	no	1.544 or 2.048 MHz	Synchronized on Line RCLK1-4 , selected by CMR1.DRSS1/0
Slave	yes	Fixed to VDD	CMR1.DCS = 0: DCO-R is centered, if CMR2.DCF = 0. (CMR2.DCF should not be set)
			CMR1.DCS = 1: Synchronized on Line RCLK1-4, selected by CMR1.DRSS1/0
Slave	yes	1.544 or 2.048 MHz	CMR1.DCS = 0: Synchronized on SYNC input (external 1.544 or 2.048 MHz)
			CMR1.DCS = 1: Synchronized on Line RCLK1-4, selected by CMR1.DRSS1/0

The jitter attenuator meets the jitter transfer requirements of the PUB 62411, PUB 43802, TR-TSY 009,TR-TSY 253, TR-TSY 499 and Rec. I.431 and G. 703.(refer to **figure 45**).

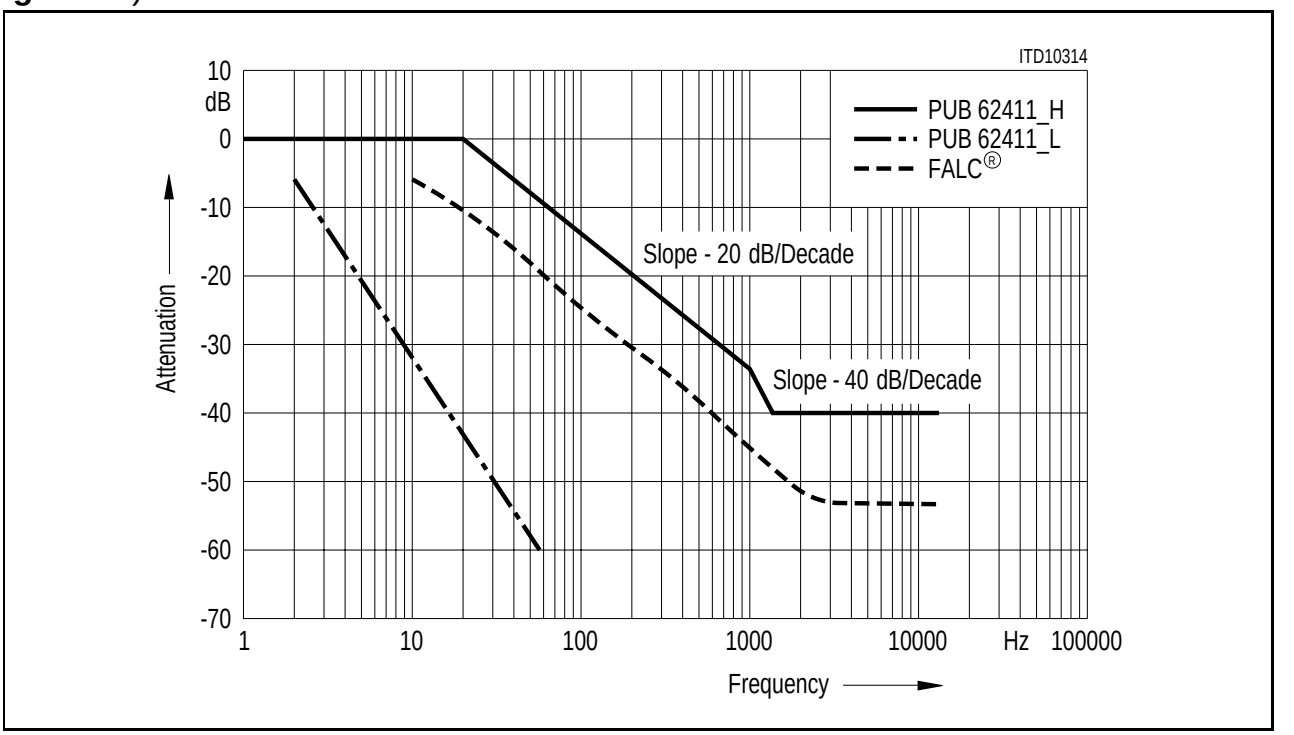


Figure 45
Jitter Attenuation Performance

Jitter Tolerance

The QuadFALC receiver's tolerance to input jitter complies to ITU and Bellcore requirements for T1 applications.

Figure 46 shows the curves of different input jitter specifications stated below as well as the QuadFALC performance.

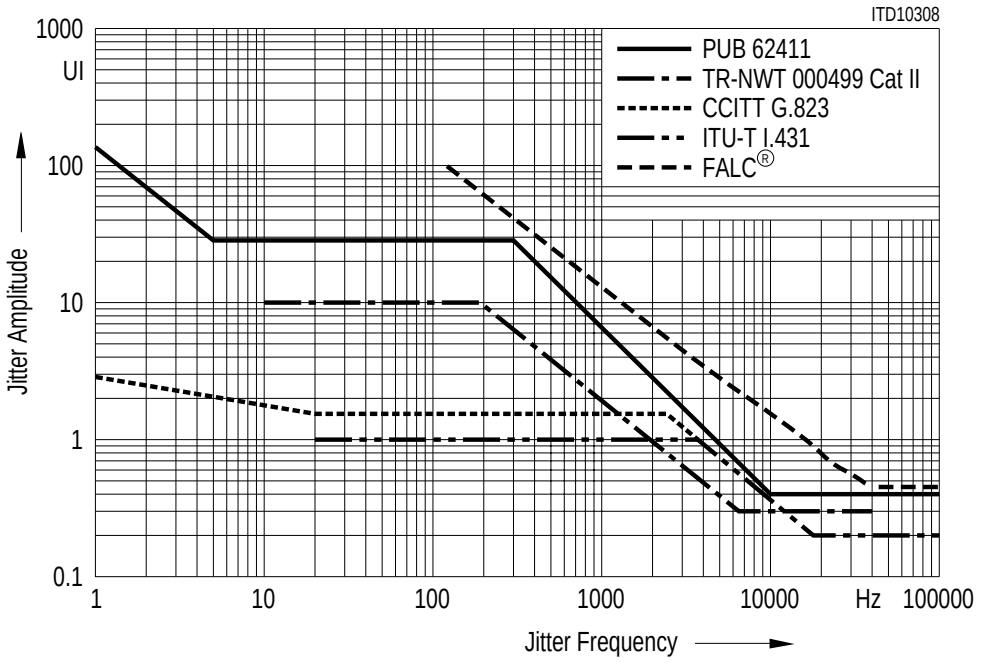


Figure 46
Jitter Tolerance

Output Jitter

According to the input jitter defined by PUB62411 the QuadFALC generates the output jitter, which is specified in table below.

Specification	Measurement Filter Bandwidth		Output Jitter (UI peak to peak)
	Lower Cutoff	Upper Cutoff	
PUB 62411	10 Hz	8 kHz	< 0.015
	8 kHz	40 kHz	< 0.015
	10 Hz	40 kHz	< 0.015
	Broadband		< 0.02

Transmit jitter attenuator

The transmit jitter attenuator DCO-X circuitry generates a „jitterfree“ transmit clock for each channel and meets the following requirements: PUB 62411, PUB 43802, TR-TSY 009,TR-TSY 253, TR-TSY 499 and Rec. I.431 and G.703. The DCO-X circuitry works internally with the same high frequency clock as the receive jitter attenuator it does. It synchronizes either to the working clock of the transmit backplane interface or the clock provided by pin TCLK or the receive clock RCLK (remote loop / loop-timed). The DCO-X attenuates the incoming jitter starting at 6 Hz with 20 dB per decade fall off. With the jitter attenuated clock, which is directly dependent on the phase difference of the incoming clock and the jitter attenuated clock, data is read from the transmit elastic buffer (2 frames) or from the JATT buffer (2 frames, remote loop) Wander with a jitter frequency below 6 Hz are passed transparentely.

The DCO-X accepts gapped clocks which are used in ATM or SDH/SONET applications. The jitter attenuated clock is output on pin XCLK.

The transmit jitter attenuator could be disabled. In that case data is read from the transmit elastic buffer with the clock sourced by pin TCLK (1.544 or 6.176 MHz). Synchronization between SCLKX and TCLK has to done externally.

In the loop-timed clock configuration (LIM2.ELT) the DCO-X circuitry generates a transmit clock which is frequency synchronized to RCLK. In this configuration the transmit elastic buffer has to be enabled.

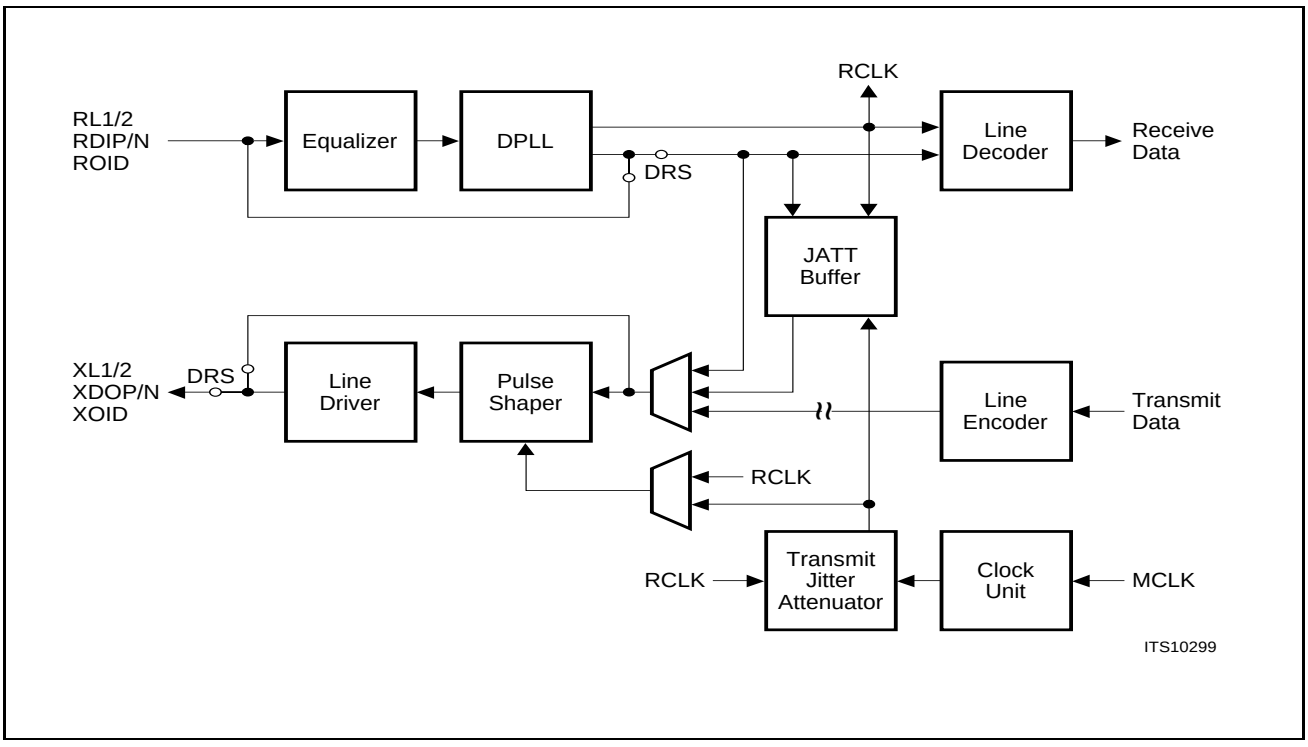


Figure 47
Clocking in Remote Loop Configuration

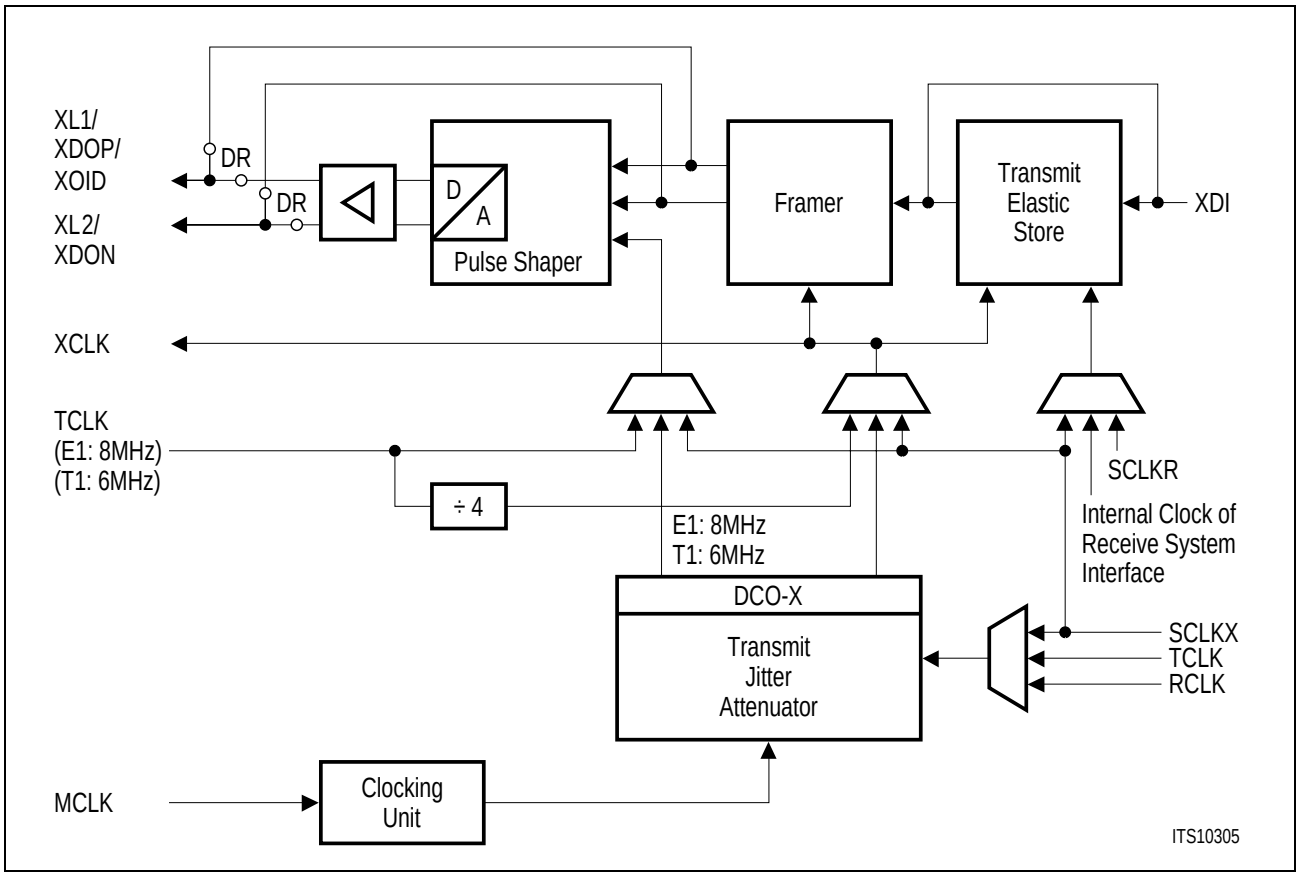


Figure 48
Transmit Clock System

Note: DR = Dual Rail Interface
DCO-X Digital Controlled Oscillator Transmit

Framer/Synchronizer

The following functions are performed:

- Synchronization on pulse frame
- Synchronization on multiframe
- Error indication when synchronization is lost. In this case, AIS is automatically sent to the system side and Remote Alarm to the remote end if en/disabled.
- Initiating and controlling of resynchronization after reaching the asynchronous state. This may be automatically done by the QuadFALC or user controlled via the microprocessor interface.
- Detection of remote alarm (yellow alarm) indication from the incoming data stream.
- Separation of service bits and data link bits. This information is stored in special status registers.
- Detection of framed or unframed in band Loop Up/Down Code
- Generation of various maskable interrupt statuses of the receiver functions.

- Generation of control signals to synchronize the CRC checker, and the receive elastic buffer.

If programmed and applicable to the selected multiframe format, CRC checking of the incoming data stream is done by generating check bits for a CRC multiframe according to the CRC 6 procedure (refer to **ITU-T Rec. G.704**). These bits are compared with those check bits that are received during the next CRC multiframe. If there is at least one mismatch, the CRC error counter (16 bit) will be incremented.

Receive Elastic Buffer

The received bit stream is stored in the receive elastic buffer. The memory is organized as a two-frame elastic buffer with a maximum size of 2 × 193 bit. The size of the elastic buffer may be independently configured for the receive and transmit direction. Programming of the receive buffer size is done by SIC1.RBS1/0 :

- RBS1/0 = 00 : two frame buffer or 386 bits
  Maximum of wander amplitude (peak-to-peak): (1 UI = 648 ns)
  System interface clocking rate: modulo 2.048 MHz:
  142 UI in channel translation mode 0
  78 UI in channel translation mode 1
  System interface clocking rate: modulo 1.544 MHz:
  max. wander: 126 UI
  average delay after performing a slip: 1 frame or 193 bits
- RBS1/0 = 01 : one frame buffer or 193 bits
  System interface clocking rate: modulo 2.048 MHz:
  Max. wander : 80 UI in channel translation mode 0
  Max. wander : 50 UI in channel translation mode 1
  System interface clocking rate: modulo 1.544 MHz:
  max. wander: 74 UI
  average delay after performing a slip: 96 bits
- RBS1/0 = 10 : short buffer or 96 bits :
  System interface clocking rate: modulo 2.048 MHz:
  Max. wander : 28 UI in channel translation mode 0; channel translation mode 1 not supported
  System interface clocking rate: modulo 1.544 MHz:
  max. wander: 38 UI
  average delay after performing a slip: 48 bits
- RBS1/0 = 11 : Bypass of the receive elastic buffer

The functions are:

- Clock adaption between system clock (SCLKR) and internally generated route clock (RCLK).
- Compensation of input wander and jitter.

- Frame alignment between system frame and receive route frame
- Reporting and controlling of slips

Controlled by special signals generated by the receiver, the unipolar bit stream is converted into bit-parallel, time-slot-serial data which is circularly written to the elastic buffer using internally generated Receive Route Clock (RCLK).

Reading of stored data is controlled by the System Clock sourced by SCLKR or by the receive jitter attenuator and the Synchronous Pulse ($\overline{SYPR}$) in conjunction with the programmed offset values for the receive time-slot/clock-slot counters. After conversion into a serial data stream, the data is given out via port RDO. If the receive buffer is bypassed programming of the time-slot offset is disabled and data is clocked off with RCLK instead of SCLKR.

The 24 received time-slots are translated into the 32 system time-slots in two different channel translation modes (FMR1.CTM). Unequipped time-slots will be set to 'FF_H'. Refer to **table 17**.

In one frame or short buffer mode the delay through the receive buffer is reduced to an average delay of 96 or 48 bits. In bypass mode the time-slot assigner is disabled. In this case $\overline{SYPR}$ programmed as input is ignored. Slips will be performed in all buffer modes except the bypass mode. After a slip is detected the read pointer is adjusted to one half of the current buffer size.

The following table gives an overview of the receive buffer operating mode .

Buffer Size (SIC1.RBS1/0)	**TS Offset program.** (RC1/0) + $\overline{SYPR}$ = input	**Slip perform.**
bypass[1)]	disabled	no
short buffer	not recommended, recom. $\overline{SYPR}$ = output	yes
1 frame	not recommended, recom. $\overline{SYPR}$ = output	yes
2 frames	enabled	yes

1) In bypass mode the clock provided on pin SCLKR is ignored. Clocking is done with RCLK.

Figure 49 gives an idea of operation of the receive elastic buffer:
A slip condition is detected when the write pointer (W) and the read pointer (R) of the memory are nearly coincident, i.e. the read pointer is within the slip limits (S +, S –). If a slip condition is detected, a negative slip (one frame or one half of the current buffer size

is skipped) or a positive slip (one frame or one half of the current buffer size is read out twice) is performed at the system interface, depending on the difference between RCLK and the current working clock of the receive backplane interface. i.e. on the position of pointer R and W within the memory. A positive / negative slip is indicated in the interrupt status bits ISR3.RSP and ISR3.RSN.

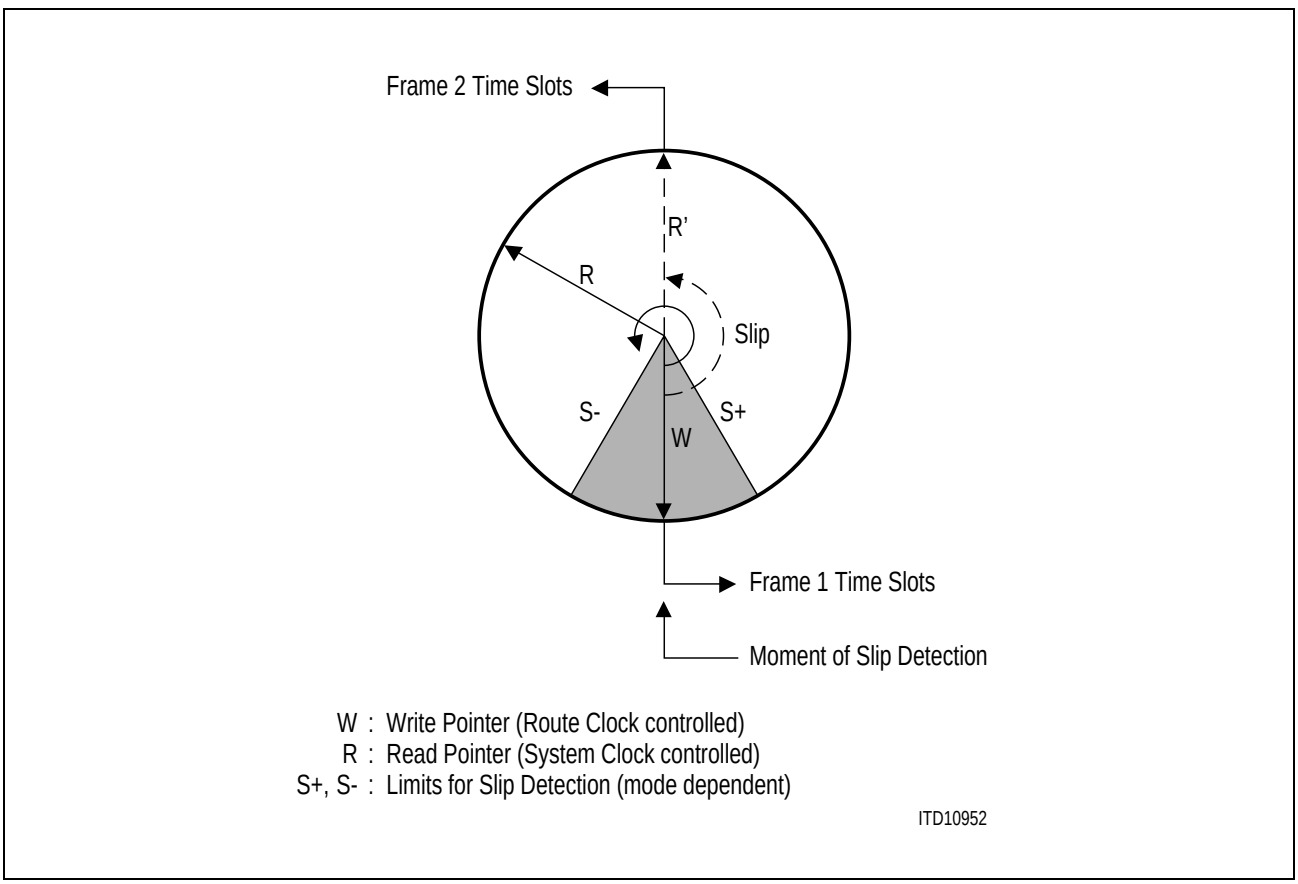


Figure 49
The Receive Elastic Buffer as Circularly Organized Memory

Speech Channels		Time-Slots
C. Translation Mode 0	C. Translation Mode 1	
FS/DL	FS/DL	0
1	1	1
2	2	2
3	3	3
–	4	4
4	5	5
5	6	6
6	7	7
–	8	8
7	9	9
8	10	10
9	11	11
–	12	12
10	13	13
11	14	14
12	15	15
–	16	16
13	17	17
14	18	18
15	19	19
–	20	20
16	21	21
17	22	22
18	23	23
–	24	24
19	–	25
20	–	26
21	–	27
–	–	28
22	–	29
23	–	30
24	–	31

Table 17
Channel Translation Modes

- : FF_H

Receive Signaling Controller

Each of the four signaling controller may be programmed to operate in various signaling modes. The QuadFALC will perform the following signaling and data link methods:

- **HDLC/SDLC or LAPD Access**
  In case of common channel signaling the signaling procedure HDLC/SDLC or LAPD according to Q.921 will be supported. The signaling controller of the QuadFALC performs the FLAG detection , CRC checking, address comparisson and zero bit-removing. The received data flow and the address recognition features may be performed in very flexible way, to satisfy almost any practical requirements. Depending on the selected address mode, the QuadFALC may perform a 1 or 2 byte address recognition. If a 2-byte address field is selected, the high address byte is compared with the fixed value FEH or FCH (group address) as well as with two individually programmable values in RAH1 and RAH2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address will be interpreted as COMMAND/RESPONSE bit (C/R) and will be excluded from the address comparison. Buffering of receive data is done in a 64 byte deep RFIFO. Refer also to **chapter 8.1**.
  In signaling controller transparent mode, fully transparent data reception without HDLC framing is performed, i.e. without FLAG recognition, CRC checking or bit-stuffing. This allows user specific protocol variations.
  The QuadFALC offers the flexibility to extract data during certain time-slots. Any combination of time-slots may be programmed independently for the receive and transmit direction.

- **CAS-Bit Robbing**
  The signaling information is carried in the LSB of every sixth frame for each time-slot. The signaling controller samples the bit stream either on the receive line side or if external signaling is enabled on the receive system side via port RSIG. Receive signaling data is stored in the registers RS1-12.
  Optionally the complete CAS multiframe may be transmitted on pin RSIG. The signaling data is clocked out with the working clock of the receive highway (SCLKR) in conjunction with the rec. synchron. pulse ($\overline{\text{SYPR}}$). Data on RSIG will be transmitted in the last 4 bits per time-slot and are time-slot aligned to the data on RDO. In ESF format the A,B,C,D bits are placed in the bit positions 5-8 per time-slot. In F12/72 format the A and B bits are repeated in the C and D bit positions. The first 4 bits per time-slot could be optionally fixed high or low. The FS/DL time-slot is transmitted on RDO and RSIG. During IDLE time-slots no signaling information is transmitted. Data on RSIG are only valid if the freeze signaling status is inactive. With FMR1.SAIS an all ones may be transmitted on RDO and RSIG.

  Updating of the received signaling information is controlled by the freeze signaling status. The freeze signaling status is automatically activated if a Loss of Signal, or a Loss of Frame Alignment or a receive slip occures. The current freeze status is output

on port FREEZ (RPA-D) and indicated by register SIS.SFS. If SIS.SFS is active updating of the registers RS1-12 is disabled. Optionally automatic freeze signaling may be disabled by setting bit SIC3.DAF.
To relieve the µP load from always reading the complete RS1-12 buffer every 3 msec the QuadFALC notifies the µP via interrupt ISR0.RSC only when signaling changes from one multiframe to the next. Additionally the QuadFALC generates a receive signaling data change pointer (RSP1/2) which directly points to the updated RS1-12 register. .

- **Bit Oriented Messages in ESF-DL Channel**
  The QuadFALC supports the DL-channel protocol for ESF format according to ANSI T1.403 specification or according to AT&T TR54016. The HDLC- and Bit Oriented Message (BOM) -Receiver may be switched ON/OFF independently. If the QuadFALC is used for HDLC formats only, the BOM receiver has to be switched off. If HDLC- and BOM-receiver has been switched on (MODE.HRAC/BRAC), an automatic switching between HDLC and BOM mode is enabled. If eight or more consecutive ones are detected, the BOM mode is entered. Upon detection of a flag in the data stream, the QuadFALC switches back to HDLC-mode. In BOM-mode, the following byte format is assumed (the left most bit is received first).
  111111110xxxxxx0
  Three different BOM reception modes may be programmed (CCR1.BRM+ CCR2.RBFE). If CCR2.RFBE is set, the BOM-receiver will only accept BOM frames after detecting 7 out of 10 equal BOM pattern. Buffering of receive data is done in a 64 byte deep RFIFO. Refer also to **chapter 8.1.4**
- 4 **kbit/s Data Link Access in F72 Format**
  The DL-channel protocol is supported as follows:
  - access is done on a multiframe basis via registers RDL1-3,
  - the DL bit information from frame 26 to 72 is stored in the Receive FIFO of the signaling controller.

7.5 System Interface

The QuadFALC offers a flexible feature for system designers where for transmit and receive direction different system clocks and system pulses are necessary. The interface to the receive system highway is realized by two data buses, one for the data RDO and one for the signaling data RSIG. The receive highway is clocked via pin SCLKR, while the interface to the transmit system highway is independently clocked via pin SCLKX. The frequency of these working clocks and the data rate of 2.048 / 4.096 / 8.192 / 16.384 / 1.544 / 3.088 / 6.192 / 12.352 MBit/s for the receive and transmit system interface is programmable by SIC1.SSC1/0, SIC2.SSC2 and SIC1.SSD1, FMR1.SSD0. Selectable system clock and data rates and their valid combinations are shown in the table below.

Table 18
System Clocking and Data Rates

System Data Rate	Clock Rate 1.544 / 2.048 MHz	Clock Rate 3.088 / 4.096 MHz	Clock Rate 6.176 / 8.192 MHz	Clock Rate 12.352 / 16.384 MHz
1.544/ 2.048 MBit/s	x	x	x	x
3.088/ 4.096 MBit/s	--	x	x	x
6.176/ 8.192 MBit/s	--	--	x	x
12.352 / 16.384 MBit/s	--	--	--	x

x = valid , -- = invalid

Generally the data or marker on the system interface are clocked off or latched on the rising or falling edge (SIC3.RESR/X) of the SCLKR/X clock. Some clocking rates allow transmitting of time-slots in different channel- phases. Each channel-phase which should be active on ports RDO, XDI, RP(A-D) and XP(A-D) is programmable by bit SIC2.SICS2-0, the remaining channel-phases are cleared or ignored.
The signals on pin $\overline{\text{SYPR}}$ in conjunction with the assigned timeslot offset in register RC0 and RC1 will define the beginning of a frame on the receive system highway.The signal on pin $\overline{\text{SYPX}}$ in conjunction with the assigned timeslot offset in register XC0 and XC1 will define the beginning of a frame on the transmit system highway.

Adjusting the frame begin (time-slot 0, bit 0) relative to $\overline{\text{SYPR/X}}$ is possible in the range of 0 - 125 µsec. The minimum shift of varying the time-slot 0 begin could be programmed between 1 bit and 1/8 bit depending of the system clocking and data rate. e.g. with a clocking / data rate of 2.048 MHz shifting is done bitwise, while running the QuadFALC with 16.384 MHz and 2.048 MBit/s data rate it is done by 1/8 bit.

A receive frame marker RFM could be activated during any bit position of the entire frame. Programming is done with registers RC1/0. The pin function RFM is selected by PC(1-4).RPC(2-0) = 001. The RFM selection disables the internal time-slot assigner, no offset programming is performed. The receive frame marker is active high for one 1.544 / 2.048 MHz cycle and is clocked off with the rising or falling edge of the clock which is in/output on port SCLKR.

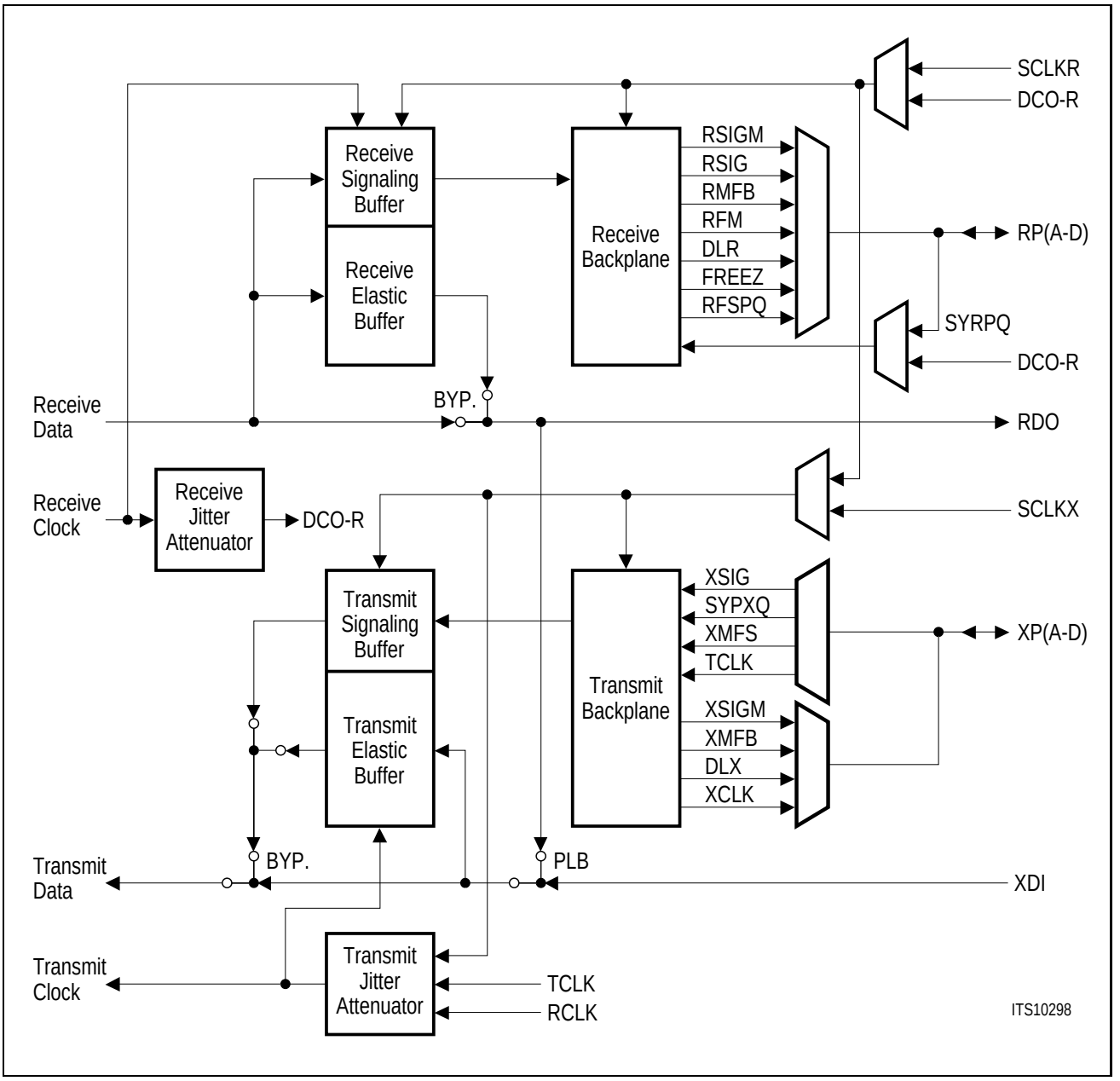


Figure 50
System Interface

System Interface Multiplex Mode

Setting this bit enables a single rail data stream of 16.384 or 8.192 or 12.352 or 6.176 MBit/s containg all four T1 frames. The receive system interface for all four channels is running with the clock provided on SCLKR1 and the frame sync pulse provided on $\overline{\text{SYPR1}}$. The transmit system interface is running with SCLKX1 and $\overline{\text{SYPX1}}$. Data will be transmitted / accepted in a byte or bit interleaved format. Bit interleaving is valid with the 16.384 / 8.192 / 12.352 or 6.176 MHz clocking rates. However byte interleaving is only

applicable with the 16.384 or 8.192 MHz clock. All four channels have to be configured equally with the following parameters:

- clocking rate : 16.384 / 8.192 / 12.352 / 6.176 MHz , SIC1.SSC1/0 and SIC2.SSC2
- data rate : 16.384 / 8.192 / 12.352 / 6.176 MBit/s, SIC1.SSD1, FMR1.SSD0
- time-slot offset programming : RC1/0 , XC1/0
- receive buffer size : SIC1.RBS1/0 = 00 (2 frames)

The multiplexed data stream is internal logically ored. Therefore the selection of the active channel phase have to be configured different for each single channel FALC. Programming is done with SIC2.SICS2-0.

In system interface multiplex mode signals on RDO2-4 and RSIG2-4 are undefined, while signals on SCLKR2-4, $\overline{\text{SYPR}}$2-4, SCLKX2-4, $\overline{\text{SYPX}}$2-4, XDI2-4 and XSIG2-4 are ignored.

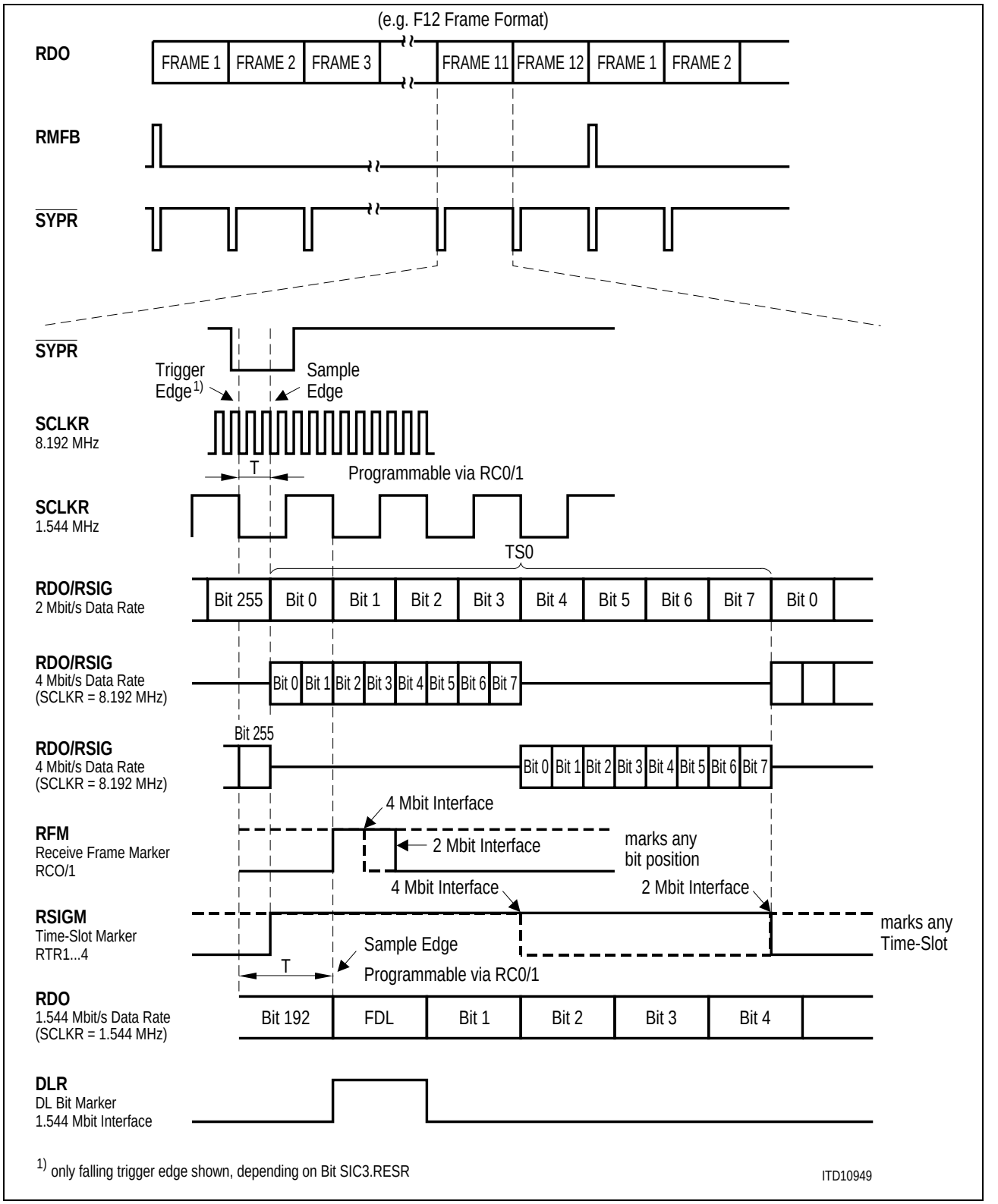


Figure 51
Receive System Interface Clocking

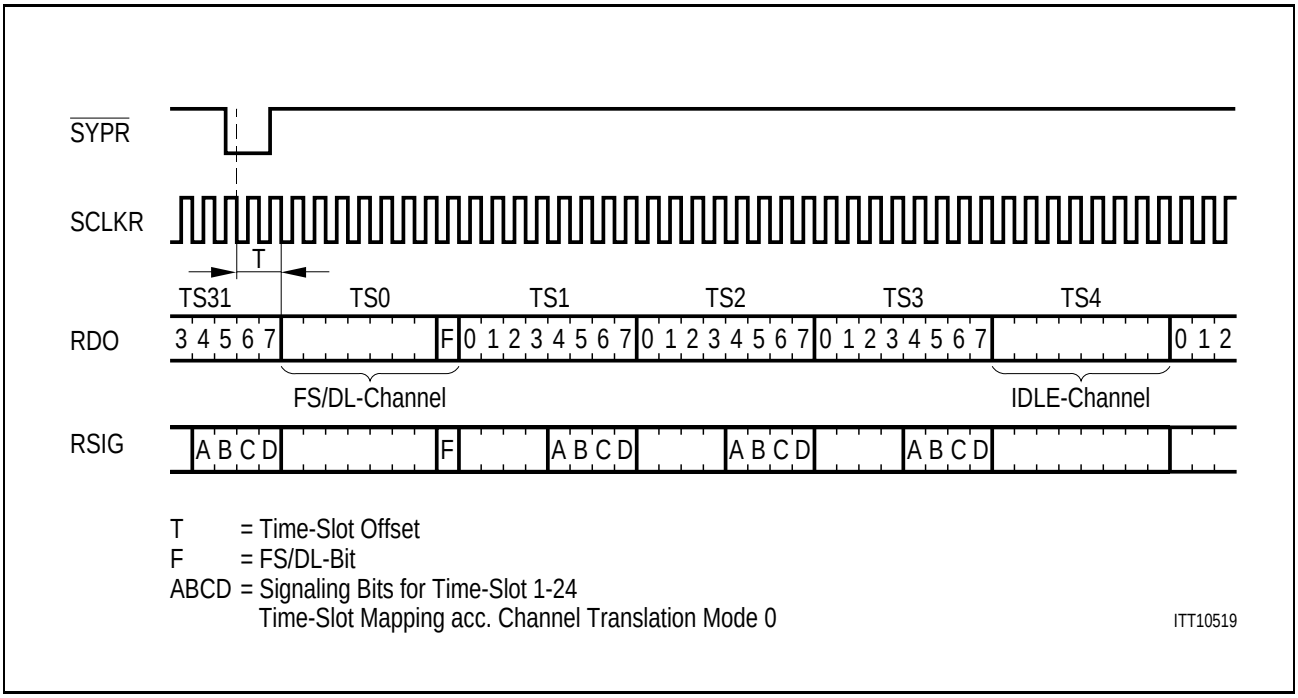


Figure 52
2.048 MHz Receive Signaling Highway

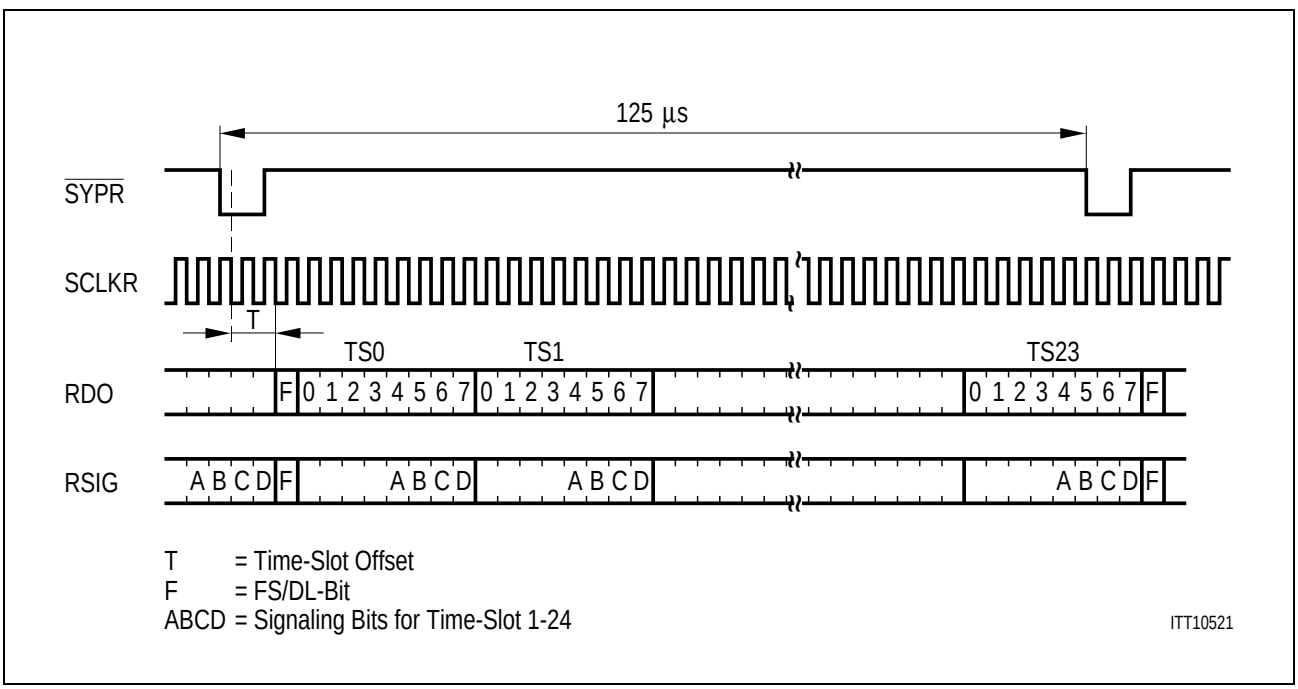


Figure 53
1.544 MHz Receive Signaling Highway

Time-Slot Assigner

The QuadFALC offers the flexibility to connect data during certain time-slots, as defined by registers RTR1-4 and TTR1-4, to the RFIFO and XFIFO, respectively. Any combinations of time-slots can be programmed for the receive and transmit directions. If CCR1.EITS = 1 the selected time-slots (RTR1-4) will be stored in the RFIFO of the signaling controller and the XFIFO contents will be inserted into the transmit path as controlled by registers TTR1-4.

Table 19
Time-Slot Assigner

		Time-Slots
Receive Time-Slot Register	**Transmit Time-Slot Register**	
RTR1.7	TTR1.7	0
RTR1.6	TTR1.6	1
RTR1.5	TTR1.5	2
RTR1.4	TTR1.4	3
RTR1.3	TTR1.3	4
RTR1.2	TTR1.2	5
RTR1.1	TTR1.1	6
RTR1.0	TTR1.0	7
RTR2.7	TTR2.7	8
RTR2.6	TTR2.6	9
RTR2.5	TTR2.5	10
RTR2.4	TTR2.4	11
RTR2.3	TTR2.3	12
RTR2.2	TTR2.2	13
RTR2.1	TTR2.1	14
RTR2.0	TTR2.0	15
RTR3.7	TTR3.7	16
RTR3.6	TTR3.6	17
RTR3.5	TTR3.5	18
RTR3.4	TTR3.4	19
RTR3.3	TTR3.3	20
RTR3.2	TTR3.2	21
RTR3.1	TTR3.1	22

Table 19
Time-Slot Assigner <NotBold> (cont'd)

		Time-Slots
Receive Time-Slot Register	**Transmit Time-Slot Register**	
RTR3.0	TTR3.0	23
RTR4.7	TTR4.7	24
RTR4.6	TTR4.6	25
RTR4.5	TTR4.5	26
RTR4.4	TTR4.4	27
RTR4.3	TTR4.3	28
RTR4.2	TTR4.2	29
RTR4.1	TTR4.1	30
RTR4.0	TTR4.0	31

The format for receive FS/DL data transmission in time-slot 0 via the system interface is as shown in figure below. In order to get an undisturbed receiption even in the asynchronous state bit FMR2.DAIS has to be set.

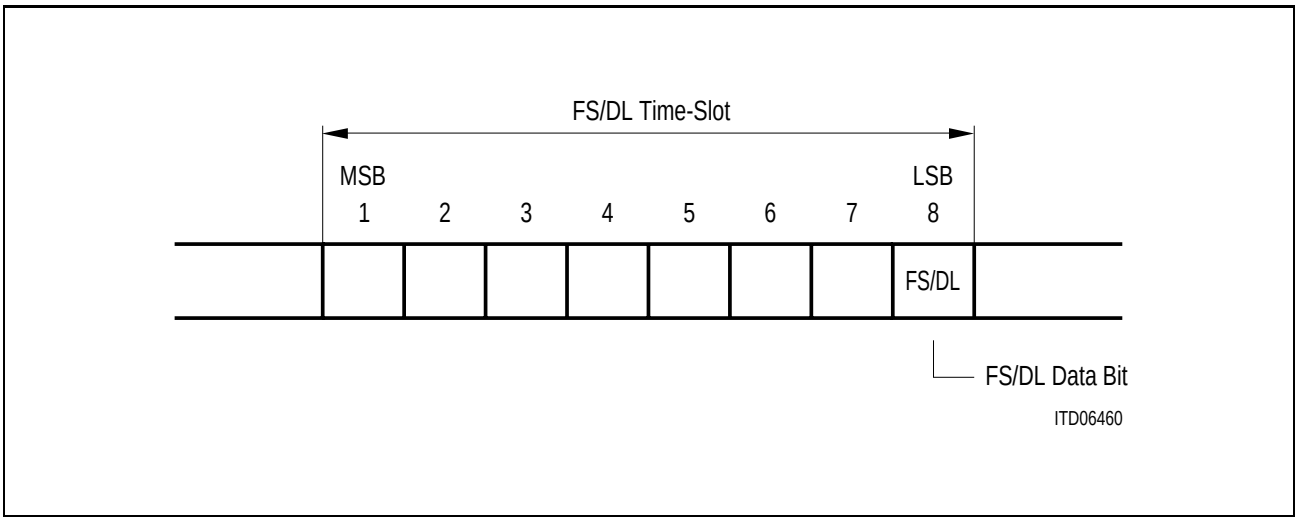


Figure 54
Receive FS/DL Bits in Time-Slot 0 on RDO

7.6 Transmit Path

Compared to the receive paths the inverse functions are performed for the transmit direction.

The interface to the transmit system highway is realized by two data buses, one for the data XDI and one for the signaling data XSIG. The time-slot assignment is equivalent to the receive direction. All unequipped (idle) time-slots will be ignored.

Latching of data is controlled by the System Clock (SCLKX or SCLKR) and the Synchronous Pulse ($\overline{\text{SYPX}}$ / XMFS) in conjunction with the programmed offset values for the Transmit Time-slot/Clock-slot Counters XC1/0. The frequency of the working clock 2.048 / 4.096 / 8.192 / 16.384 MHz or 1.544 / 3.088 / 6.176 / 12.352 MHz for the transmit system interface is programmable by SIC1.SSC1/0 and SIC2.SSC2. Refer also **table 18**

The received bit stream on ports XDI and XSIG could be multiplexed internally on a time-slot basis, if enabled by SIC3.TTRF = 1. The data received at port XSIG could be sampled if the transmit signaling marker XSIGM is active high. Data at port XDI will be sampled if XSIGM is low for the respective time-slot. Programming the XSIGM marker is done with registers TTR1-4.

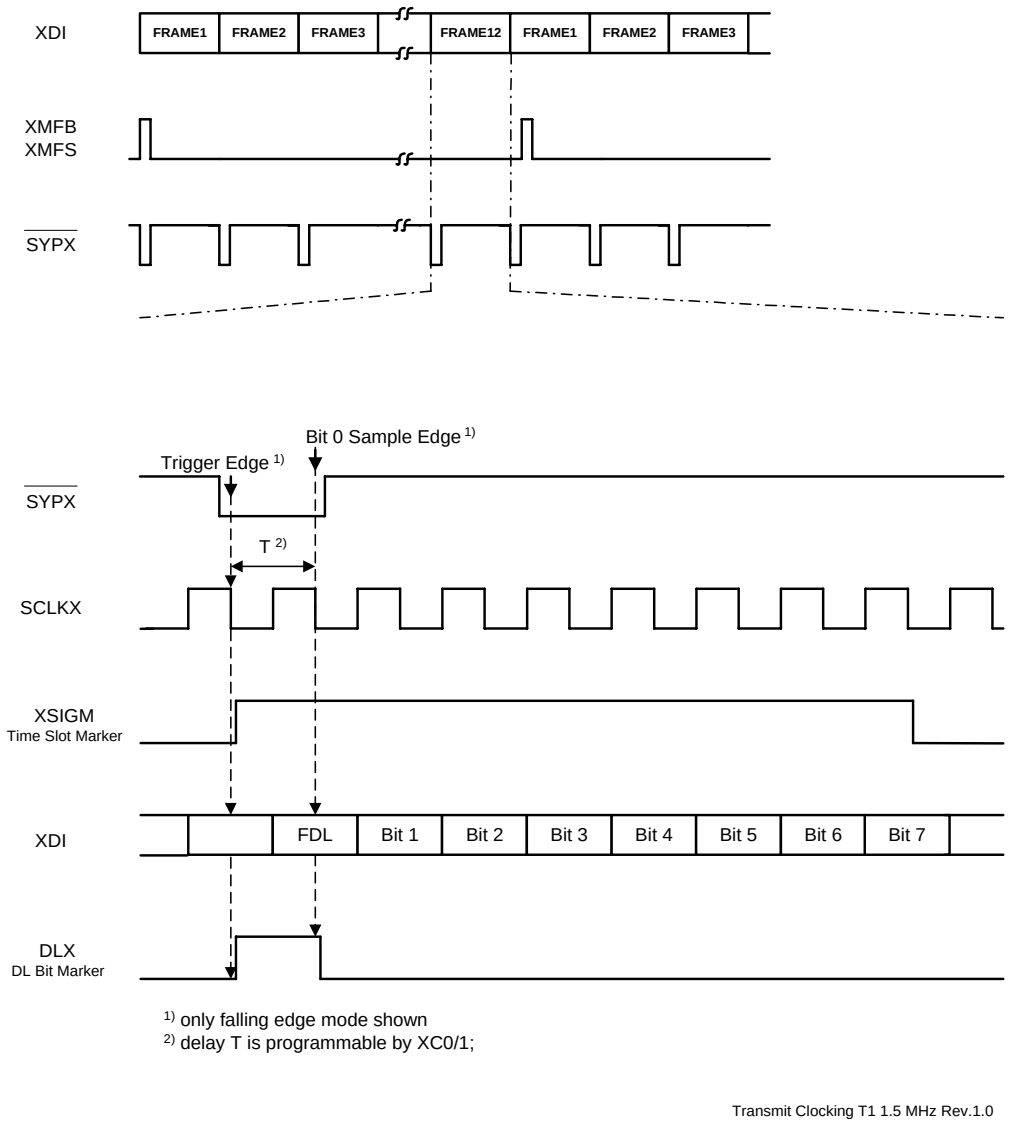


Figure 55
Transmit System Interface Clocking: 1.544 MHz

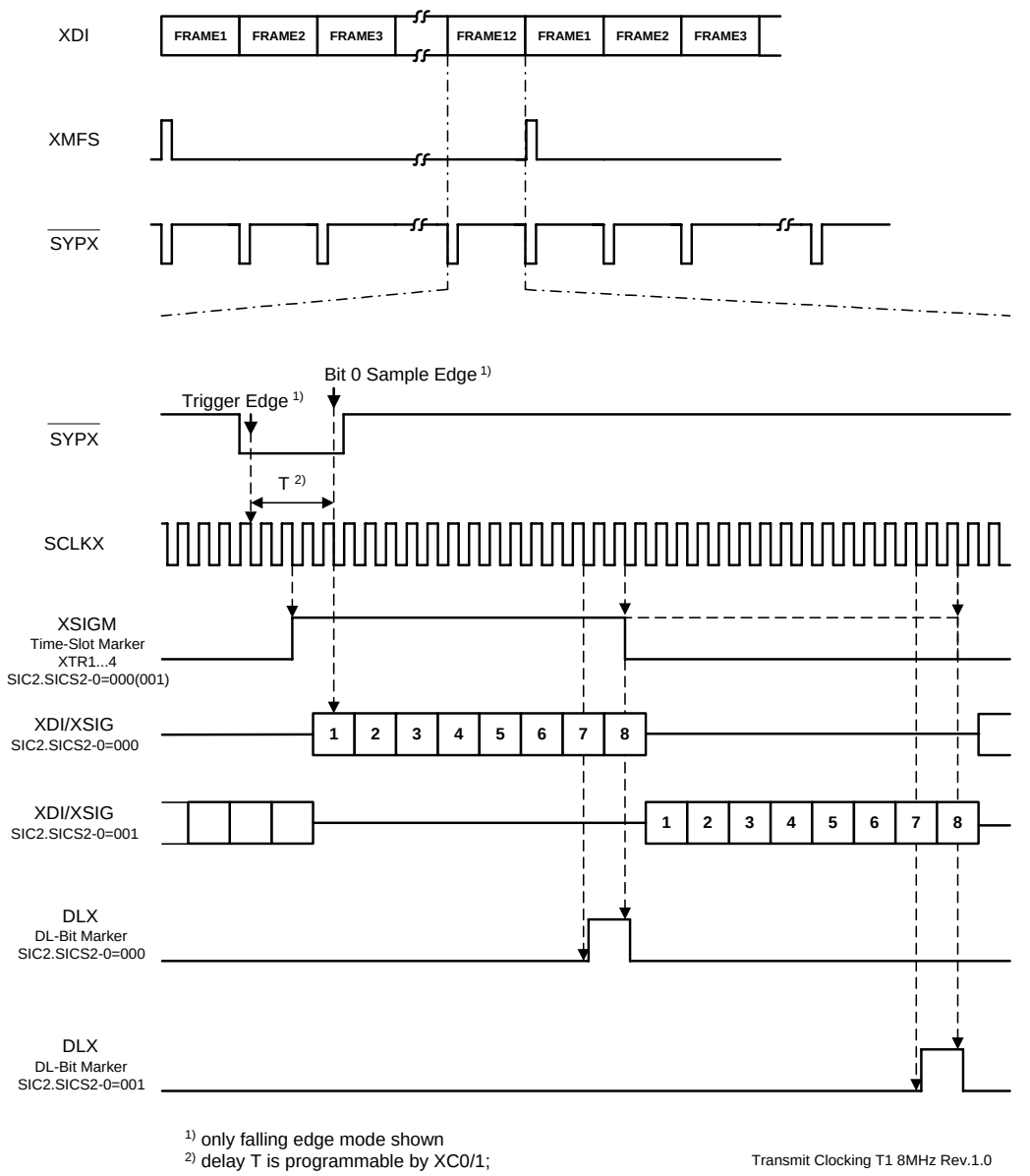


Figure 56
Transmit System Interface Clocking: 8.192 MHz and 4.096 MBit/s

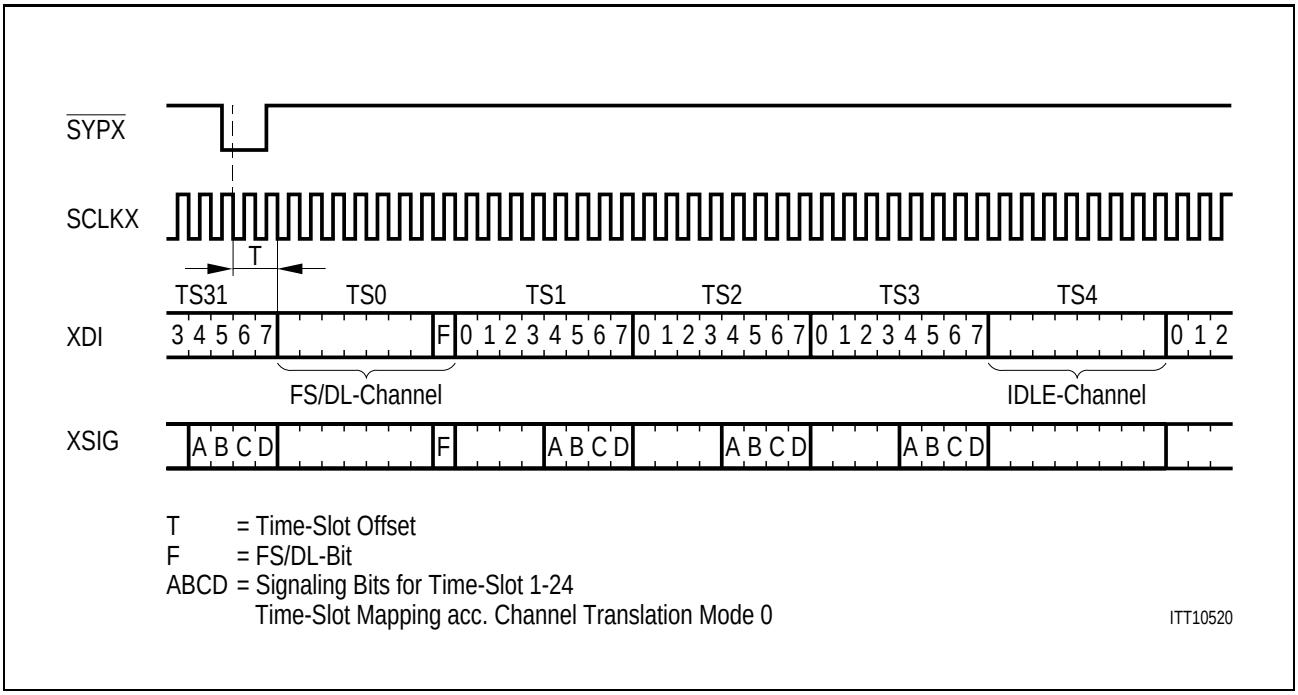


Figure 57
2.048 MHz Transmit Signaling Clocking

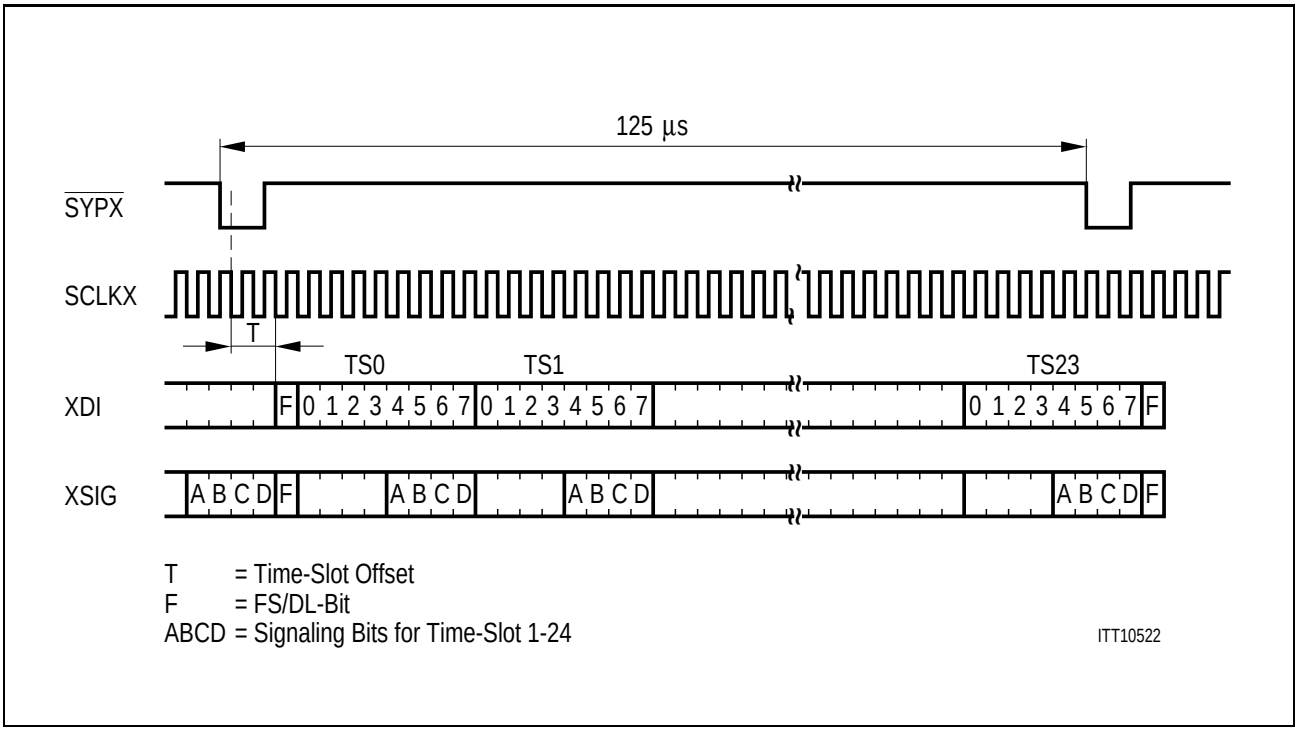


Figure 58
1.544 MHz Transmit Signaling Highway

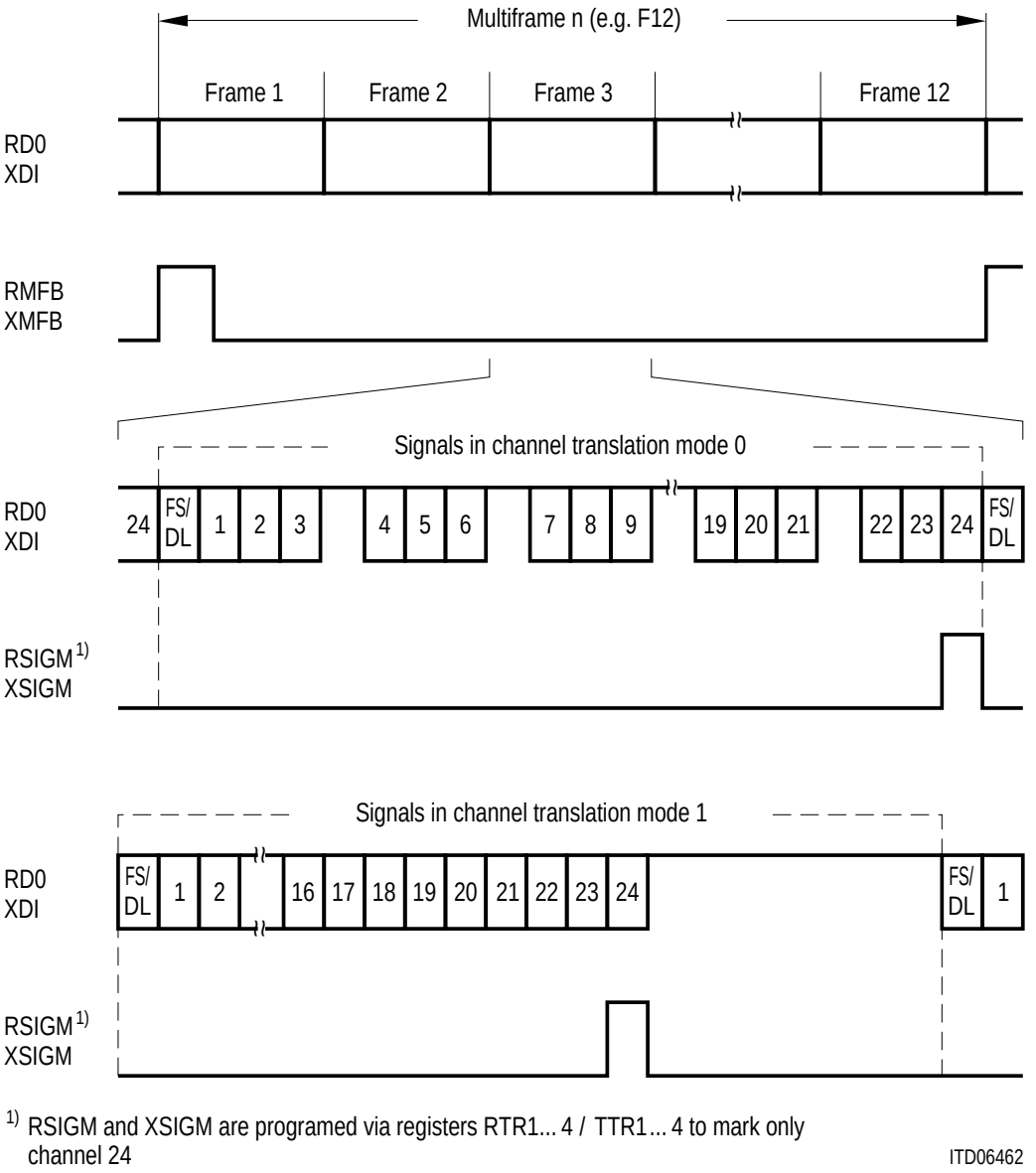
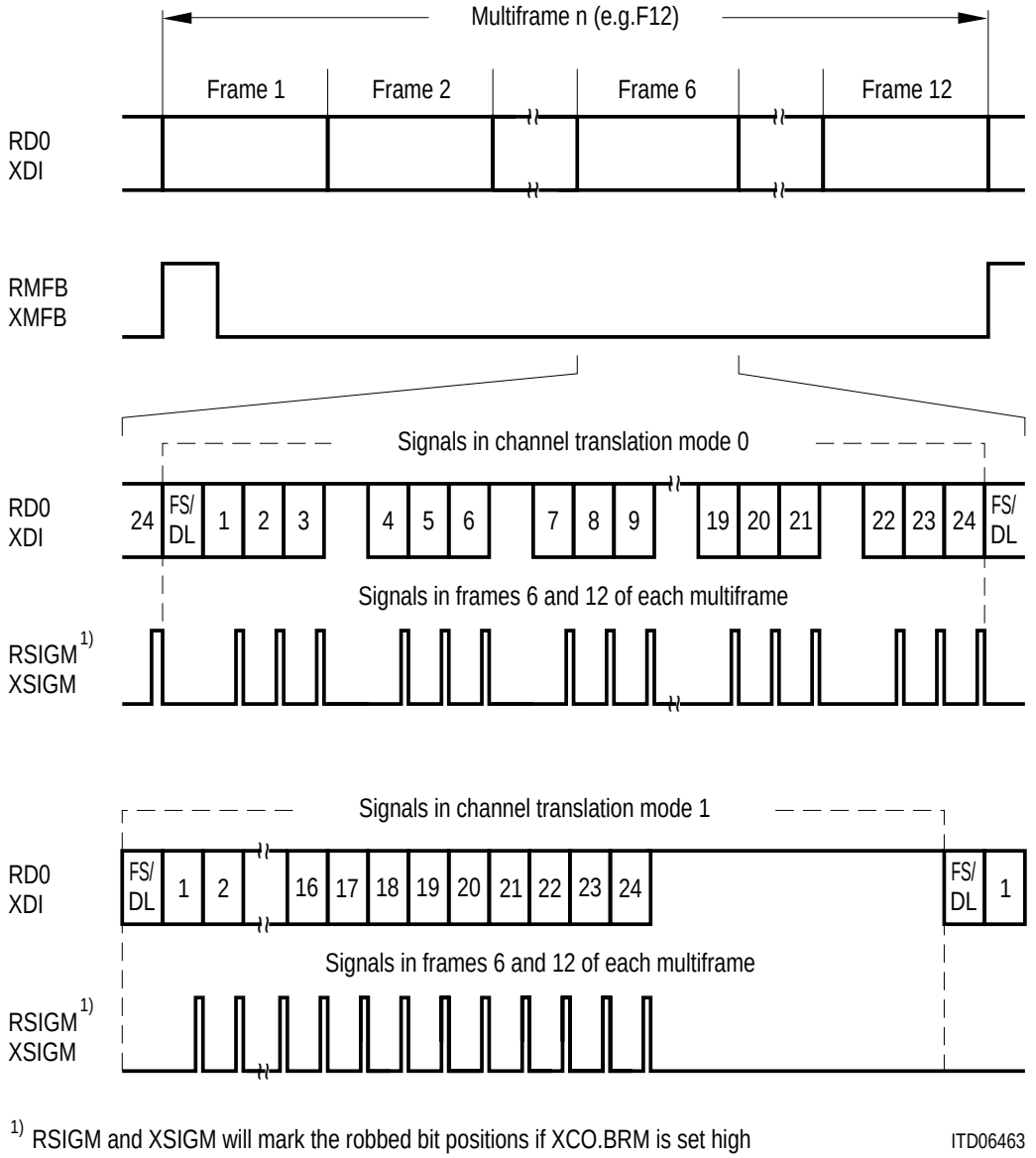


Figure 59
Signaling Marker for CCS/CAS-CC Applications



1) RSIGM and XSIGM will mark the robbed bit positions if XCO.BRM is set high

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Figure 60
Signaling Marker for CAS-BR Applications

Transmit Direction

FS/DL data on system transmit highway (XDI), time-slot 0.

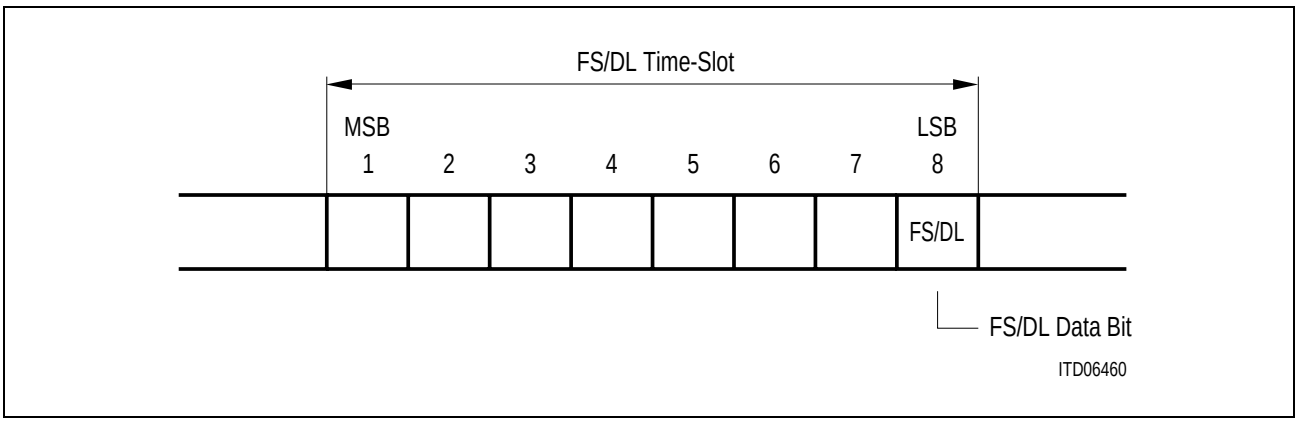


Figure 61
Transmit FS/DL Bits on XDI

Transmit Signaling Controller

Similar to the receive signaling controller the same signaling methods and the same time-slot assignment are provided. The QuadFALC will perform the following signaling and data link methods:

- **HDLC or LAPD access**
  The transmit signaling controller of the QuadFALC performs the FLAG generation, CRC generation, zero bit-stuffing and programmable IDLE code generation. Buffering of transmit data is done in the 64 byte deep XFIFO. The signaling information will be internally multiplexed with the data applied to port XDI or XSIG.
  In signaling controller transparent mode, fully transparent data transmission without HDLC framing is performed. Optionally the QuadFALC supports the continuous transmission of the XFIFO contents.
  Operating in HDLC or BOM mode “flags” or “idle” may be transmitted as interframe timefill. The QuadFALC offers the flexibility to insert data during certain time-slots. Any combinations of time-slots may be programmed separately for the receive and transmit directions.
- **CAS Bit Robbing**
  The signaling controller inserts the bit stream either on the transmit line side or if external signaling is enabled on the transmit system side. Signaling data may be sourced internally from registers XS1-12 or externally at port XSIG, which is selected by register PC1-4.
  In external signaling mode the signaling data is sampled with the working clock of the transmit system interface (SCLKX) in conjunction with the transmit synchronous pulse ($\overline{\text{SYPX}}$). Data on XSIG will be latched in the bit positions 5-8 per time-slot, bits 1-4 will

be ignored. The FS/DL bit is sampled on port XSIG and inserted in the outgoing data stream. The received CAS multiframe will be inserted frame aligned into the data stream on XDI. Data sourced by the internal signaling controller will overwrite the external signaling data.
Internal multiplexing of data and signaling data may be disabled on a per time-slot basis (Clear Channel Capability). This is also valid when using the internal and external signaling mode.

- **Data Link Access in ESF and F72 Format**
  The DL-channel protocol is supported as follows:
  - access is done on a multiframe basis via registers XDL1-3 or
  - HDLC access or transparent transmission (non HDLC mode) from XFIFO
  the signaling information stored in the XFIFO will inserted in the DL bits of frame 26 to 72 in F72 format or in every other frame in ESF format. Transmitting may be done on a multiframe boundary. Operating in HDLC or BOM mode “flags” or “idle” may be transmitted as interframe timefill.

Transmit Elastic Buffer

The transmit elastic store with a size of max. 2×193 bit (two -frames) serves as a temporary store for the PCM data to adapt the system clock (SCLKX) to the internally generated clock for the transmit data, and to re-translate time-slot structure used in the system to that of the line side. Its optimal start position is initiated when programming the transmit time-slot offset values. A difference in the effective data rates of system side and transmit side may lead to an overflow/underflow of the transmit memory: thus, errors in data transmission to the remote end may occur. This error condition (transmit slip) is reported to the microprocessor via interrupt status registers.
The received bit stream from pin XDI is optionally stored in the transmit elastic buffer. The memory is organized as the receive elastic buffer. Programming of the transmit buffer size is done by SIC1.XBS1/0 :

- XBS1/0 = 00 : bypass of the transmit elastic buffer
- XBS1/0 = 01 : one frame buffer or 193 bits
  Maximum of wander amplitude (peak-to-peak): (1 UI = 648 ns)
  System interface clocking rate: modulo 2.048 MHz:
  Max. wander : 80 UI in channel translation mode 0
  Max. wander : 50 UI in channel translation mode 1
  System interface clocking rate: modulo 1.544 MHz:
  max. wander: 74 UI
  average delay after performing a slip: 96 bits
- XBS1/0 = 10 : two frame buffer or 386 bits
  System interface clocking rate: modulo 2.048 MHz:
  142 UI in channel translation mode 0
  78 UI in channel translation mode 1

System interface clocking rate: modulo 1.544 MHz:
max. wander: 126 UI
average delay after performing a slip: 193 bits

- XBS1/0 = 11 : short buffer or 96 bits :
  System interface clocking rate: modulo 2.048 MHz:
  Max. wander : 28 UI in channel translation mode 0; channel translation mode 1 not supported
  System interface clocking rate: modulo 1.544 MHz:
  max. wander: 38 UI
  average delay after performing a slip: 48 bits

The functions of the transmit buffer are:

- Clock adaption between system clock (SCLKX/R) and internally generated transmit route clock (XCLK) or externally sourced TCLK.
- Compensation of input wander and jitter.
- Frame alignment between system frame and transmit route frame
- Reporting and controlling of slips

Writing of received data from XDI is controlled by SCLKX/R and $\overline{\text{SYPX}}$ / XMFS in conjunction with the programmed offset values for the transmit time-slot/clock-slot counters. Reading of stored data is controlled by the clock generated by DCO-X circuitry or the externally generated TCLK and the transmit framer. With the dejittered clock data is read from the transmit elastic buffer and are forwarded to the transmitter. Reporting and controlling of slips is automatically done according to the receive direction. Positive / negative slips are reported in interrupt status bits ISR4.XSP and ISR4.XSN.

A re-initialization of the transmit memory is done by re-programming the transmit time-slot counter XC1 and with the next $\overline{\text{SYPX}}$ pulse. After that, this memory has its optimal start position.

The frequency of the working clock for the transmit system interface is programmable by SIC1.SSC1/0 and SIC2.SSC2 in a range of 1.544 ... 12.352 MHz / 2.048 ... 16.384 MHz. Generally the data or marker on the system interface are clocked off or latched on the rising or falling edge (SIC3.SPS) of the SCLKX clock. Some clocking rates allow transmitting of time-slots / marker in different channel- phases. Each channel-phase which should be latched on ports XDI and XP(A-D) is programmable by bits SIC2.SICS2-0 , the remaining channel-phases are cleared resp. ignored

The following table gives an overview of the transmit buffer operating modes.

Buffer Size	TS Offset program.	Slip perform.
bypass	enabled	no

Buffer Size	TS Offset program.	Slip perform.
short buffer	disabled	yes
1 frame	enabled	yes
2 frames	enabled	yes

Transmitter

The serial bit stream is then processed by the transmitter which has the following functions:

- Frame/multiframe synthesis of one of the four selectable framing formats
- Insertion of service and data link information
- AIS generation (Blue Alarm)
- Remote alarm (yellow alarm) generation
- CRC generation and insertion of CRC bits
  CRC bits inversion in case of a previously received CRC error or in case of activating per control bit
- Generation of Loop Up/Down code
- IDLE code generation per DS0

The frame / multiframe boundries of the transmitter may be externally synchronized by using the $\overline{\text{SYPX}}$ / XMFS pin. Any change of the transmit time-slot assignment will subsequently produce a change of the framing bit positions on the line side. This feature is required if signaling- and data link - bits are routed through the switching network and are inserted in transmit direction via the system interface.

In loop-timed configuration (LIM2.ELT) disconnecting the control of the transmit system highway from the transmitter is done by setting FMR5.XTM. The transmitter is now in a free running mode without any possibility to actualize the multiframe position in case of changing the transmit time-slot assignment. The FS/DL bits are generated independent of the transmit system interface. For proper operation the transmit elastic buffer size should be programmed to 2 frames.

The contents of selectable time-slots may be overwritten by the pattern defined via register IDLE. The selection of “idle channels” is done by programming the three-byte registers ICB1 … ICB3.

If AMI coding with zero code suppression (B7-stuffing) is selected, “clear channels” without B7-stuffing can be defined by programming registers CCB1 … CCB3.

Transmit Line Interface

The analog transmitter transforms the unipolar bit stream to ternary (alternate bipolar) return to zero signals of the appropriate programmable shape. The unipolar data is provided by pin XDI and the digital transmitter.

Similar to the receive line interface three different data types are supported:

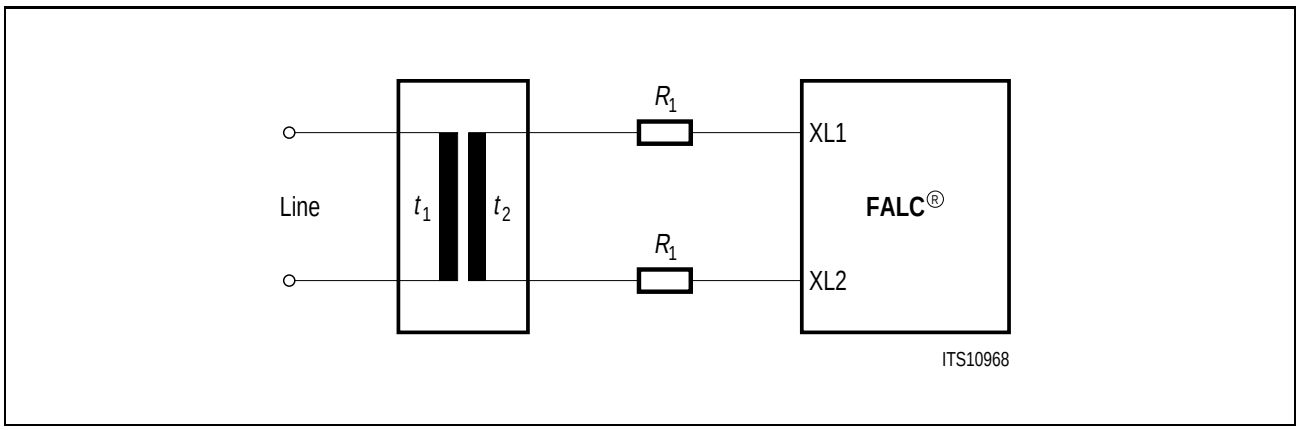


Figure 62
Transmitter Configuration

Table 20
Recommended Transmitter Configuration Values

Parameter	Characteristic Impedance 100 Ω
	DS1
R_1 (± 1 %) [Ω]	2
t2 : t1	1 : 2.4

- Ternary Signal
  Single rail data is converted into a ternary signal which is output on pins XL1 and XL2. Selection between B8ZS or simple AMI coding with zero code suppression (B7 stuffing) is provided. B7 stuffing may be disabled on a per time-slot basis (clear channel capability). Selected by FMR0.XC1/0 and LIM1.DRS = 0.
- Dual rail data PCM(+), PCM(-) at multifunction ports XDOP and XDON with 50 % or 100 % duty cycle and with programmable polarity. Line coding is done in the same way as in the ternary interface. Selected by FMR0.XC1=1 and LIM1.DRS = 1.
- Unipolar data on port XOID will be transmitted in NRZ (Non Return to Zero) with 100 % duty cycle or in CMI code with or without (SIC3.CMI) preprocessed by B8ZS coding to a fibre optical interface. Clocking off data is done with the rising edge of the transmit clock XCLK (1544 kHz) and with a programmable polarity. Selection is done by FMR0.XC1 = 0 and LIM1.DRS = 1.

Programmable Pulse Shaper and Line Build-Out

In long haul applications the transmit pulse masks are optionally generated according to FCC68 and ANSI T1. 403. To reduce the crosstalk on the received signals the QuadFALC offers the ability to place a transmit attenuator in the data path. Transmit attenuation is selectable from 0 , -7.5, -15 or -22.5 dB (register LIM2.LBO2/1).
ANSI T1. 403 defines only 0 -15 dB.

The QuadFALC includes a programmable pulse shaper to satisfy the requirements of ANSI T1. 102 , also various DS1, DSX-1 specifications are met. The amplitude of the pulse shaper is individually programmable via the microprocessor interface to allow a maximum of different pulse templates. The line length is selected by programming the registers XPM2-0 as shown for typical values in the table below. The values with transformer ratio: 1:2.4; cable: PULP 22AWG (100 Ω); serial resistors: 2 Ω. The XPM register values are given in decimal.

Range in m	XP04-XP00	XP14-XP10	XP24-XP20	XP34-XP30
	decimal			
0 - 35	29	27	10	3
25 - 65	29	28	10	3
55 - 95	31	28	10	2
85 - 125	31	27	13	2
115 - 155	31	26	13	2
145 - 185	31	26	13	3
175 - 210	31	25	14	3

The transmitter requires an external step up transformer to drive the line.

Transmit Line Monitor

The transmit line monitor compares the transmit line current on XL1 and XL2 with an on-chip transmit line current limiter. The monitor detects faults on the primary side of the transformer indicated by a highly increased transmit line current (more than 120 mA for at least 3 pulses) and protects the device from damage by setting the transmit line driver XL1/2 automatically in a high impedance state. Two conditions will be detected by the monitor: transmit line ones density (more than 31 consecutive zeros) indicated by FRS1.XLO and transmit line high currrent indicated by FRS1.XLS. In both cases a transmit line monitor status change interrupt will be provided.

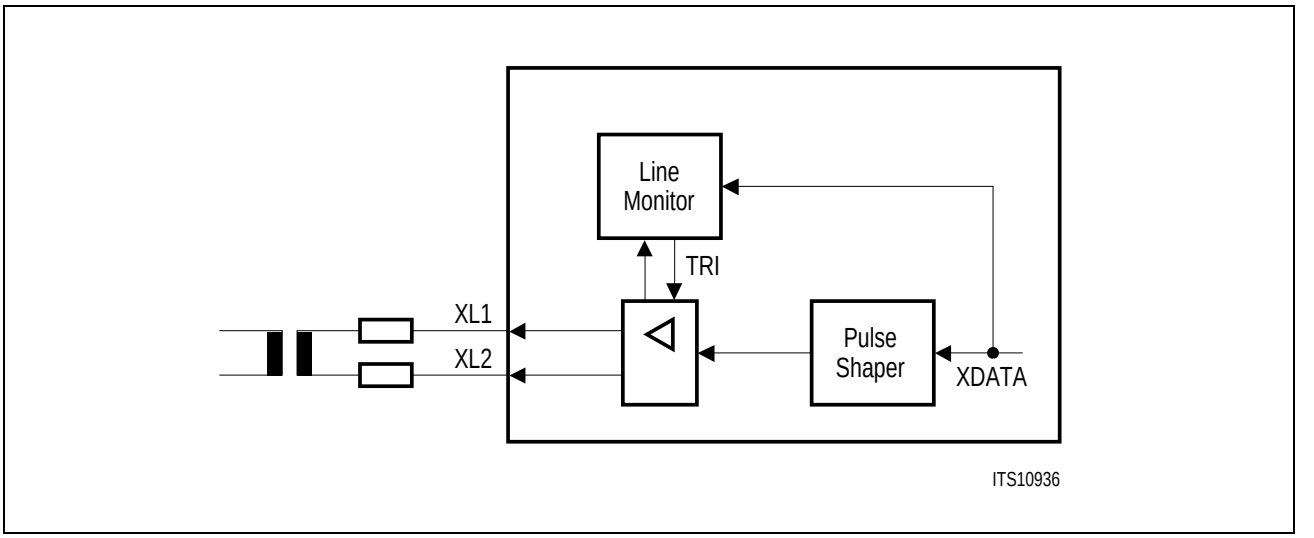


Figure 63
Transmit Line Monitor Configuration

7.7 Framer Operating Modes T1 / J1

General

Activated with bit FMR1.PMOD = 1.

PCM line bit rate	:	1.544 MBit/s
Single frame length	:	193 bit, No. 1 … 193
Framing frequency	:	8 kHz
Organization	:	24 time-slots, No. 1 … 24 with 8 bits each, No. 1 … 8 and one preceding F bit

Selection of one of the four permissible framing formats is performed by bits FMR4.FM1/0 . These formats are:

F4	:	4-frame multiframe
F12	:	12-frame multiframe (D4)
ESF	:	Extended Superframe
F72	:	72-frame multiframe (SLC96)

The operating mode of the QuadFALC is selected by programming the carrier data rate and characteristics, line code, multiframe structure, and signaling scheme.

The QuadFALC implements all of the standard and/or common framing structures PCM 24 (T1, 1.544 MBit/s) carriers. The internal HDLC-Controller supports all signaling procedures including signaling frame synchronization / synthesis in all framing formats.

After RESET, the QuadFALC must be programmed with FMR1.PMOD = 1 to enable the T1(PCM24) mode. Switching between the framing formats is done via bit FMR4.FM1/0 for the receiver and for the transmitter.

General Aspects of Synchronization

Synchronization status is reported via bit FRS0.LFA (Loss Of Frame Alignment). Framing errors (pulse frame and multiframe) are counted by the Framing Error Counter FEC.

Asynchronous state is reached if
2 out of 4 (bit FMR4.SSC1/0 = 00), or
2 out of 5 (bit FMR4.SSC1/0 = 01), or
2 out of 6 (bit FMR4.SSC1/0 = 10), or
4 consecutive multiframe pattern in ESF format are incorrect (bit FMR4.SSC1/0 = 11).
framing bits (terminal framing or multiframing) are incorrect. If auto-mode is enabled, counting of framing errors is interrupted.

The resynchronization procedure may be controlled by either one of the following procedure:

- Automatically (FMR4.AUTO = 1). Additionally, it may be triggered by the user by setting/resetting one of the bits FMR0.FRS (Force Resynchronization) or FMR0.EXLS (External Loss of Frame).
- User controlled, exclusively, via above control bits in the non-auto-mode (FMR4.AUTO = 0).

Addition for F12 and F72 Format

FT and FS bit conditions, i.e. pulse frame alignment and multiframe alignment can be handled separately if programmed via bit FMR2.SSP. Thus, a multiframe re-synchronization can be automatically initiated after detecting 2 errors out of 4/5/6 consecutive multiframing bits without influencing the state of the terminal framing.

In the synchronous state, the setting of FMR0.FRS or FMR0.EXLS resets the synchronizer and initiates a new frame search. The synchronous state is reached if there is only one definite framing candidate. In the case of repeated apparent simulated candidates, the synchronizer remains in the asynchronous state.

In asynchronous state, the function of FMR0.EXLS is the same as above. Setting bit FMR0.FRS induces the synchronizer to lock onto the next available framing candidate if there is one. Otherwise, a new frame search is started. This is useful in case the framing pattern that defines the pulseframe position is imitated periodically by a pattern in one of the speech/data channels.

The control bit FMR0.EXLS should be used first because it starts the synchronizer to search for a definite framing candidate.

To observe actions of the synchronizer, the Frame Search Restart Flag FRS0.FSRF is implemented. It toggles at the start of a new frame search if no candidate has been found at previous attempt.

When resynchronization is initiated, the following values apply for the time required to achieve the synchronous state in case there is one definite framing candidate within the data stream:

Table 21
Resynchronization Timing

Frame Mode	Avg.	Max.	Units
F4	1.0	1.5	ms
F12	3.5	4.5	
ESF	3.4	6.125	
F72	13.0	17.75	

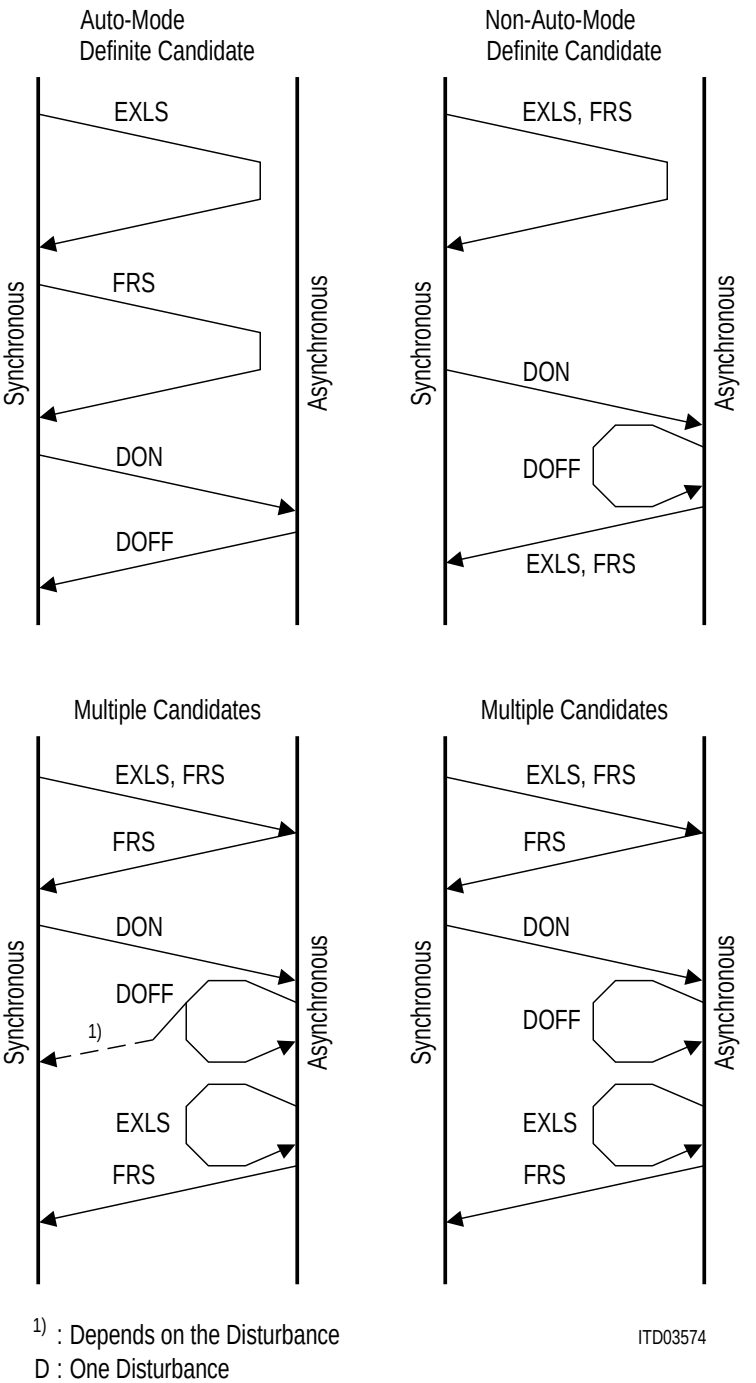


Figure 64
Influences on Synchronization Status

Figure 64 gives an overview of influences on synchronization status for the case of different external actions. Activation of auto-mode and non-auto mode is performed via bit FMR4.AUTO. Generally, for initiating resynchronization it is recommended to use bit: FMR0.EXLS first. In case where the synchronizer remains in the asynchronous state, bit FMR0.FRS may be used to enforce it to lock onto the next framing candidate, although it might be a simulated one.

7.7.1 4-Frame Multiframe

The allocation of the FT bits (bit 1 of frames 1 and 3) for frame alignment signal is shown in **table 22**.

The FS bit may be used for signaling.
Remote alarm (yellow alarm) is indicated by setting bit 2 to ‘0’ in each time-slot.

Table 22
4-Frame Multiframe Structure

Frame Number	F_T	F_S
1	1	
2	–	Service bit
3	0	
4	–	Service bit

Synchronization Procedure

For multiframe synchronization, the terminal framing bits (FT bits) are observed. The synchronous state is reached if at least one terminal framing candidate is definitely found, or the synchronizer is forced to lock onto the next available candidate (FMR0.FRS).

7.7.2 12-Frame Multiframe (D4 or SF Format)

Normally, this kind of multiframe structure only makes sense when using the CAS Robbed Bit Signaling. The multiframe alignment signal is located at the FS-bit position of every other frame (refer to **table 23**).

There are two possibilities of remote alarm (yellow alarm) indication:

- Bit 2 = 0 in each time-slot of a frame, selected with bit FMR0.SRAF = 0
- The last bit of the multiframe alignment signal (bit 1 of frame 12) changes from ‘0’ to ‘1’, selected with bit FMR0.SRAF = 1.

Synchronization Procedure

In the synchronous state terminal framing (FT bits) and multiframing (FS bits) are observed, independently. Further reaction on framing errors depends on the selected sync/resync procedure (via bit FMR2.SSP):

- FMR2.SSP = ‘0’: terminal frame and multiframe synchronization are combined.
  Two errors within 4/5/6 framing bits (via bits FMR4.SSC1/0) of one of the above will lead to the asynchronous state for terminal framing **and** multiframing. Additionally to the bit FRS0.LFA, loss of multiframe alignment is reported via bit FRS0.LMFA.
  The resynchronization procedure starts with synchronizing upon the terminal framing. If the pulseframing has been regained, the search for multiframe alignment is initiated. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.
- FMR2.SSP = ‘1’: terminal frame and multiframe synchronization are separated
  Two errors within 4/5/6 terminal framing bits will lead to the same reaction as described above for the “combined” mode.
  Two errors within 4/5/6 multiframing bits will lead to the asynchronous state only for the multiframing. Loss of multiframe alignment is reported via bit FRS0.LMFA. The state of terminal framing is not influenced.
  Now, the resynchronization procedure includes only the search for multiframe alignment. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.

Table 23
12-Frame Multiframe Structure

Frame Number	F_T	F_S	Signaling Channel Designation
1	1	–	
2	–	0	
3	0	–	
4	–	0	
5	1	–	
6	–	1	A
7	0	–	
8	–	1	
9	1	–	
10	–	1	
11	0	–	
12	–	0	B

7.7.3 Extended Superframe (F24, ESF Format)

The use of the first bit of each frame for the multiframe alignment word, the data link bits, and the CRC bits is shown in **table 24**.

Table 24
Extended Superframe Structure

Multiframe Frame Number	F Bits				Signaling Channel Designation
	Multiframe Bit Number	Assignments			
		FAS	DL	CRC	
1	0	–	m	–	
2	193	–	–	e_1	
3	386	–	m	–	
4	579	0	–	–	
5	772	–	m	–	
6	965	–	–	e_2	A
7	1158	–	m	–	
8	1351	0	–	–	
9	1544	–	m	–	
10	1737	–	–	e_3	
11	1930	–	m	–	
12	2123	1	–	–	B
13	2316	–	m	–	
14	2509	–	–	e_4	
15	2702	–	m	–	
16	2895	0	–	–	
17	3088	–	m	–	
18	3231	–	–	e_5	C
19	3474	–	m	–	
20	3667	1	–	–	
21	3860	–	m	–	
22	4053	–	–	e_6	
23	4246	–	m	–	
24	4439	1	–	–	D

Synchronization Procedures

For multiframe synchronization the FAS bits are observed. Synchronous state is reached if at least one framing candidate is definitely found, or the synchronizer is forced to lock onto the next available candidate (FMR0.FRS).

In the synchronous state the framing bits (FAS bits) are observed. The following conditions selected by FMR4.SSC1/0 will lead to the asynchronous state:

- two errors within 4/5/6 framing bits
- two or more erroneous framing bits within one ESF multiframe
- more than 320 CRC6 errors per second interval (FMR5.SSC2)
- 4 incorrect (1 out of 6) consecutive multiframes independent of CRC6 errors.

There are four multiframe synchronization modes selectable via FMR2.MCSP and FMR2.SSP.

- FMR2.MCSP/SSP = 00 : In the synchronous state, the setting of FMR0.FRS or FMR0.EXLS resets the synchronizer and initiates a new frame search. The synchronous state will be reached again, if there is only one definite framing candidate. In the case of repeated apparent simulated candidates, the synchronizer remains in the asynchronous state.
  In asynchronous state, setting bit FMR0.FRS induces the synchronizer to lock onto the next available framing candidate if there is one. At the same time the internal framing pattern memory will be cleared and other possible framing candidates are lost.

- FMR2.MCSP/SSP = 01: Synchronization is achieved when 3 consecutive multiframe pattern are correctly found independent of the occurence of CRC6 errors. If only one or two consecutive multiframe pattern were detected the QuadFALC will stay in the asynchronous state, searching for a possible additionally available framing pattern. This procedure will be repeated until the framer has found three consecutive multiframe pattern in a row.

- FMR2.MCSP/SSP = 10: This mode has been added in order to be able to choose multiple framing pattern candidates step by step. I.e. if in synchronous state the CRC error counter indicates that the synchronization might have been based on an alias framing pattern, setting of FMR0.FRS will lead to synchronization on the next candidate available. However, only the previously assumed candidate will discarded in the internal framing pattern memory. The latter procedure can be repeated until the framer has locked on the right pattern (no extensive CRC errors).
  The synchronizer will be completely reset and initiates a new frame search, if there is no multiframing found. In this case bit FSR0.FSRF toggles.

- FMR2.MCSP/SSP = 11: Synchronization including automatic CRC6 checking
  Synchronization is achieved when framing pattern are correctly found and the CRC6 checksum is received without an error. If the CRC6 check failed on the assumed framing pattern the QuadFALC will stay in the asynchronous state, searching for a possible available framing pattern. This procedure will be repeated until the framer has locked on the right pattern. This automatic synchronization mode has been added in order to reduce the microprocessor load.

Remote Alarm (yellow alarm) Generation / Detection

Remote alarm (yellow alarm) is indicated by the periodical pattern ‘1111 1111 0000 0000 …’ in the DL bits. Remote alarm will be declared even in the presence of BER 1/1000. The alarm will be reset when the ‘yellow alarm pattern’ no longer is detected .

Depending on bit RC1.SJR the QuadFALC will generate and detect the Remote Alarm according to JT G. 704. In the DL-bit position 16 continous „1“ are transmitted if FMR0.SRAF=0 and FMR4.XRA=1.

CRC6 Generation and Checking

Generation and checking of CRC6 bits transmitted/received in the e1-e6 bit positions is done according to ITU-T G.706. The CRC6 checking algorithm is enabled via bit FMR1.CRC. If not enabled, all check bits in the transmit direction are set to ‘1’. In the synchronous state received CRC6 errors are accumulated in a 16 bit error counter and are additionally indicated by an interrupt status.

– CRC6 Inversion

If enabled by bit RC0.CRCI, all CRC bits of one outgoing extended multiframe are automatically inverted in case a CRC error is flagged for the previous received multiframe. Setting the bit RC0.XCRCI will invert the CRC bits before transmitted to the distant end. This function is logically ored with RC0.CRCI.

– CRC6 Generation / Checking According to JT G. 706

Setting of RC1.SJR the QuadFALC will generate and check the CRC6 bits according to JT G. 706. The CRC6 checksum is calculated including the FS/DL bits. In synchronous state CRC6 errors will increment an error counter.

7.7.4 72-Frame Multiframe (SLC96)

The 72-multiframe is an alternate use of the FS-bit pattern and is used for carrying data link information. This is done by stealing some of redundant multiframing bits after the transmission of the 12-bit framing header (refer to **table 25**). The position of A and B signaling channels (robbed bit signaling) is defined by zero-to-one and one-to-zero transitions of the FS bits and is continued when the FS bits are replaced by the data link bits.

Remote Alarm (Yellow Alarm) is indicated by setting bit 2 to zero in each time-slot. An additional use of the D bits for alarm indication is user defined and must be done externally.

Synchronization Procedure

In the synchronous state terminal framing (FT bits) and multiframing (FS bits of the framing header) are observed independently. Further reaction on framing errors depends on the selected sync/resync procedure (via bit FMR2.SSP):

- FMR2.SSP = ‘0’: terminal frame and multiframe synchronization are combined
  Two errors within 4/5/6 framing bits (via bits FMR4.SSC1/0) of one of the above will lead to the asynchronous state for terminal framing **and** multiframing. Additionally to the bit FRS0.LFA, loss of multiframe alignment is reported via bit FRS0.LMFA.
  The resynchronization procedure starts with synchronizing upon the terminal framing. If the pulseframing has been regained, the search for multiframe alignment is initiated. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.

- FMR2.SSP = ‘1’: terminal frame and multiframe synchronization are separated
  Two errors within 4/5/6 terminal framing bits will lead to the same reaction as described above for the “combined” mode.
  Two errors within 4/5/6 multiframing bits will lead to the asynchronous state only for the multiframing. Loss of multiframe alignment is reported via bit FRS0.LMFA. The state of terminal framing is not influenced.
  Now, the resynchronization procedure includes only the search for multiframe alignment. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.

Table 25
72-Frame Multiframe Structure

Frame Number	F_T	F_S	Signaling Channel Designation
1	1	–	
2	–	0	
3	0	–	
4	–	0	
5	1	–	
6	–	1	A
7	0	–	
8	–	1	
9	1	–	
10	–	1	
11	0	–	
12	–	0	B
13	1	–	
14	–	0	
15	0	–	
16	–	0	
17	1	–	
18	–	1	A
19	0	–	
20	–	1	
21	1	–	
22	–	1	
23	0	–	
24	–	D	B
25	1	–	
26	–	D	
27	.	.	
28	.	.	
.	1	–	
66	–	D	A
67	0	–	
68	–	D	
69	1	–	
70	–	D	
71	0	–	
72	–	0	B

Table 26
Summary Frame Recover / Out of Frame Conditions

Format	Frame Recover Condition	Out of Frame Condition
F4	only one FT pattern found, optional forcing on next available FT framing candidate	2 out of 4/5/6 incorrect FT bits
F12 (D4) and F72 (SLC96)	FMR2.SSP = 0: Combined FT + FS framing search: First searching for FT pattern with optional forcing on next available fr. candidates and then for 2 consecutive correct FS pattern[1)]. FMR2.SSP = 1: Separated FT + FS pattern search: Loss of FT framing will start first searching for FT and then for 2 consecutive correct FS pattern[1)]. Loss of FS framing will start only the FS pattern[1)]. search.	FMR2.SSP=0 : 2 out of 4/5/6 incorrect FT or FS bits FMR2.SSP= 1 : 2 out of 4/5/6 incorrect FT bits will search FT and FS framing bits, 2 out of 4/5/6 incorrect FS bits will search only the FS framing.
F24 (ESF)	FMR2.MCSP/SSP = 00: only one FAS pattern found, optional forcing on next available FAS framing candidate with discarding of all remaining fr. cand. FMR2.MCSP/SSP = 01: 3 consecutive correct multiframing found independent of CRC6 errors. FMR2.MCSP/SSP = 10: choosing multiple framing pattern step by step, optional forcing on next available FAS framing pattern with discarding only of the previous assumed framing candidate. FMR2.MCSP/SSP = 11: FAS framing correctly found and CRC6 check error free.	2 out of 4/5 incorrect FAS bits or 2 out of 6 incorrect FAS bits per multiframe or 4 consecutive incorrect multiframing pattern or more than 320 CRC6 errors per second interval

[1)] In F12 (D4) format bit 1 in frame 12 is excluded fromthe synchronization process.

7.7.5 Additional Functions

Error performance monitoring and alarm handling

- Alarm detection and generation

Alarm Indication Signal: Detection and recovery is flagged by bit FRS0.AIS and ISR2.AIS. Transmission is enabled via bit FMR1.XAIS.

Loss of Signal: Detection and recovery is flagged by bit FRS0.LOS and ISR2.LOS.

Remote Alarm Indication: Detection and release is flagged by bit FRS0.RRA and ISR2.RA/RAR. Transmission is enabled via bit FMR4.XRA.

Excessive Zeros: Detection is flagged by bit FRS1.EXZD.

Pulse Density Violation: Detection is flagged by bit FRS1.PDEN and ISR0.PDEN.

Transmit Line Shorted: Detection and release is flagged by bit FRS1.XLS and ISR1.XLSC.

Transmit Ones Density: Detection and release is flagged by bit FRS1.XLO and ISR1.XLSC.

Table 27
Summary of Alarm Detection and Release

Alarm	Detection Condition	Clear Condition
Red Alarm or Loss of Signal (LOS)	no transitions (logical zeros) in a programmable time interval of 16 - 4096 consecutive pulse periods. Programmable receive input signal threshold	programmable number of ones (1-256) in a programmble time interval of 16 - 4096 consecutive pulse periods. A one is a signal with a level above the programmed threshold. or the pulse density is fulfilled and no more than 15 contiguous zeros during the recovery interval are detected.
Blue Alarm or Alarm Indication Signal (AIS)	FMR4.AIS3 = 0: less than 3 zeros in 12 frames or 24 frames (ESF), FMR4.AIS3 = 1: less than 4 zeros in 12 frames or less than 6 zeros in 24 frames (ESF)	active for at least one multiframe. FMR4.AIS3 = 0: more than 2 zeros in 12 or 24 frames (ESF), FMR4.AIS3 = 1: more than 3 zeros in 12 frames or more than 5 zeros in 24 frames (ESF)

Alarm	Detection Condition	Clear Condition
Yellow Alarm or Remote Alarm (RRA)	RC1.RRAM = 0: bit 2 = 0 in 255 consecutive time-slots or FS bit = 1 of frame12 in F12 (D4) format or 8x1,8x0 in the DL channel (ESF) RC1.RRAM = 1: bit 2 = 0 in every time-slot per frame or FS bit = 1 of frame12 in F12 (D4) format or 8x1,8x0 in the DL channel (ESF)	RC1.RRAM = 0: set conditions no longer detected. RC1.RRAM = 1: bit 2 = 0 not detected in 3 consecutive frames or FS bit not detected in 3 consecutive mulitframes or 8x1,8x0 not detected for 3 times in a row (ESF).
Excessive Zeros (EXZD)	more than 7 (B8ZS code) or more than 15 (AMI code) contiguous zeros	Latched Status: cleared on read
Pulse Density Violation (PDEN)	less than 23 ones received in a floating time window of 192 bits or more than 14 consecutive zeros	Latched Status: cleared on read
Transmit Line Short (XLS)	more than 32 pulse periods with highly increased transmit line current on XL1/2	no transmit line current limiter active
Transmit Ones Density (XLO)	32 consecutive zeros in the transmit data stream on XL1/2	Cleared with each transmitted pulse

RRA detection operates in the presence of 10exp(-3) bit error rate.

– **Auto modes**

- Automatic remote alarm (Yellow Alarm) access

If the receiver has lost its synchronization (FRS0.LFA) a remote alarm (yellow alarm) could be sent automatically, if enabled by bit FMR2.AXRA to the distant end. In synchronous state the remote alarm bit will be removed.

- Automatic AIS to system interface

In asynchronous state the synchronizer enforces automatically an AIS to the receive system interface. However, received data may be transparently switched through if bit FMR2.DAIS is set.

- Automatic clock source switching

In Slave mode (LIM0.MAS = 0) the DCO-R will synchronize to the recovered route

clock. In case of Loss of Signal LOS the DCO-R switches automatically to Master mode. If bit CMR1.DCS is set automatic switching from RCLK to SYNC can be disabled.

- Automatic freeze signaling:

Updating of the received signaling information is controlled by the freeze signaling status. The freeze signaling status is automatically activated if a Loss of Signal, or a Loss of Multiframe Alignment or a receive slip occures. The internal signaling buffer RS1-12 is froozen. Optionally automatic freeze signaling may be disabled by setting bit SIC3.DAF.

- **Error counter**

  The QuadFALC offers six error counters each of them has a length of 16 bit. They record code violations, framing bit errors, CRC6 bit errors, errored blocks and the number of received multiframes in the asynchronous state or the changes of frame alignment (COFA). Counting of the multiframes in the asyn. state and the COFA parameter is done in a 6 / 2 bit counter. Each of the error counter is buffered. Updating the buffer is done in two modes:

  - one second accumulation
  - on demand via handshake with writing to the DEC register

  In the one second mode an internal/external one second timer will update these buffers and reset the counter to accumulate the error events in the next one second period. The error counter can not overflow. Error events occuring during reset will not lost.

- **Status : errored second**

  The QuadFALC supports the error performance monitoring by detecting the following alarms or error events in the received data:
  framing errors , CRC errors , code violations , loss of frame alignment , loss of signal, alarm indication signal , receive and transmit slips.
  With a programmable interrupt mask register ESM all these alarms or error events could generate an Errored Second interrupt (ISR3.ES) if enabled.

- **Second timer**

  Additionally per channel a one second timer interrupt could be internally generated to indicate that the enabled alarm status bits or the error counters have to be checked. Enabled by GPC1.FSS2-0 the one second timer of the selected channel may be output on port SEC/FSC (GPC1.CSFP1/0). Optionally if all four channels of the QuadFALC should synchronized to an external second timer an appropriate clock has to be provided to pin SEC/FSC. Selecting the external second timer is done with GCR.SES. Refer also to register GPC1.

Clear Channel Capability

For support of common T1 applications, clear channels can be specified via the 3-byte register bank CCB1 … CCB3. In this mode the contents of selected transmit time-slots

will not be overwritten by internal or external sourced bit robbing and Zero Code Suppression (B7 stuffing) information.

In-Band Loop Generation and Detection

The QuadFALC generates and detects a framed or unframed in-band loop up/actuate (00001) - and down/deactuate (001) pattern according to ANSI T1. 403 with bit error rates as high as 1/100. Framed or unframed in-band loop code is selected by LCR1.FLLB . Replacing the in-band loop codes with transmit data is done by FMR5.XLD / XLU.
The QuadFALC also offers the ability generating and detecting of a flexible in-band loop up - and down pattern (LCR1.LLBP = 1). The loop up and loop down pattern is individual programmable from 2 to 8 bit in length (LCR1.LAC1/0 and LCR1.LDC1/0). Programming of loop codes is done in registers LCR2 and LCR3.
Status and interrupt-status bits will inform the user whether loop up - or loop down code was detected.

Transparent Mode

The transparent modes are useful for loopbacks or for routing data unchanged through the QuadFALC.

In receive direction, transparency for ternary or dual / single rail unipolar data is always achieved if the receiver is in the synchronous state. All bits in F-bit position of the incoming multiframe are forwarded to RDO and inserted in the FS/DL time-slot or in the F-bit position. In asynchronous state the received data may be transparently switched through if bit FMR2.DAIS is set. Setting of bit FMR2.RTM disconnects control of the elastic buffer from the receiver. The elastic buffer is now in a “free running” mode without any possibility to actualize the time slot assignment to a new frame position in case of re-synchronization of the receiver. Together with FMR2.DAIS this function may be used to realize undisturbed transparent reception.

Setting bit FMR4.TM switches the QuadFALC in transmit transparent mode:

In transmit direction bit 8 of the FS/DL time-slot from the system highway (XDI) is inserted in the F-bit position of the outgoing frame. For complete transparency the internal signaling controller, IDLE code generation, AIS alarm generation, single channel and payload loop back has to be disabled and “Clear Channels” have to be defined via registers CCB1…3.

Pulse Density Detection

The QuadFALC examines the receive data stream on the pulse density requirement which is defined by ANSI T1. 403. More than 14 consecutive zeros or less than N ones in each and every time window of 8(N+1) data bits where N=23 will be detected.

Violations of these rules are indicated by setting the status bit FRS1.PDEN and the interrupt status bit ISR0.PDEN. Generation of the interrupt status may be programmed either with the detection or with any change of state of the pulse density alarm (GCR.SCI).

Pseudo-Random Bit Sequence Generation and Monitor

The QuadFALC has the added ability to generate and monitor a 2^{15}-1 and 2^{20}-1 pseudo-random bit sequences (PRBS). The generated PRBS pattern will be transmitted optionally inverted or not to the remote end via pins XL1/2 resp. XDOP/N. Generating and monitoring of PRBS pattern is done according to ITU-T O. 151 and TR62411 with maximum 14 consecutive zero restriction.
The PRBS monitor senses the PRBS pattern in the incoming data stream. Synchronization is done on the inverted and non inverted PRBS pattern. The current synchronization status is reported in status and interrupt status registers. Enabled by bit LCR1.EPRM each PRBS bit error will increment an error counter (BEC).
Synchronization will be reached within 400 msec with a probability of 99.9% and a BER of 1/10 (pattern defined by ITU-T O.151).

Payload Loopback

To perform an effective circuit test a line loop is implemented.

If the payload loopback (FMR2.PLB) is activated the received 192 bits of payload data will be looped back to the transmit direction. The framing bits, CRC6 and DL bits are not looped, if FMR4.TM = 0. They are originated by the QuadFALC transmitter. If the PLB is enabled the transmitter and the data on pins XL1/XDOP and XL2/XDON are clocked with the working clock of the receive system interface (SCLKR). If FMR4.TM= 1 the received FS/DL bit is sent transparently back to the line interface. Following pins are ignored: XDI, XSIG, TCLK, SCLKX, $\overline{\text{SYPX}}$ and XMFS. All the received data is processed normally. With bit FMR2.SAIS an AIS could be sent to the system interface via pin RDO.

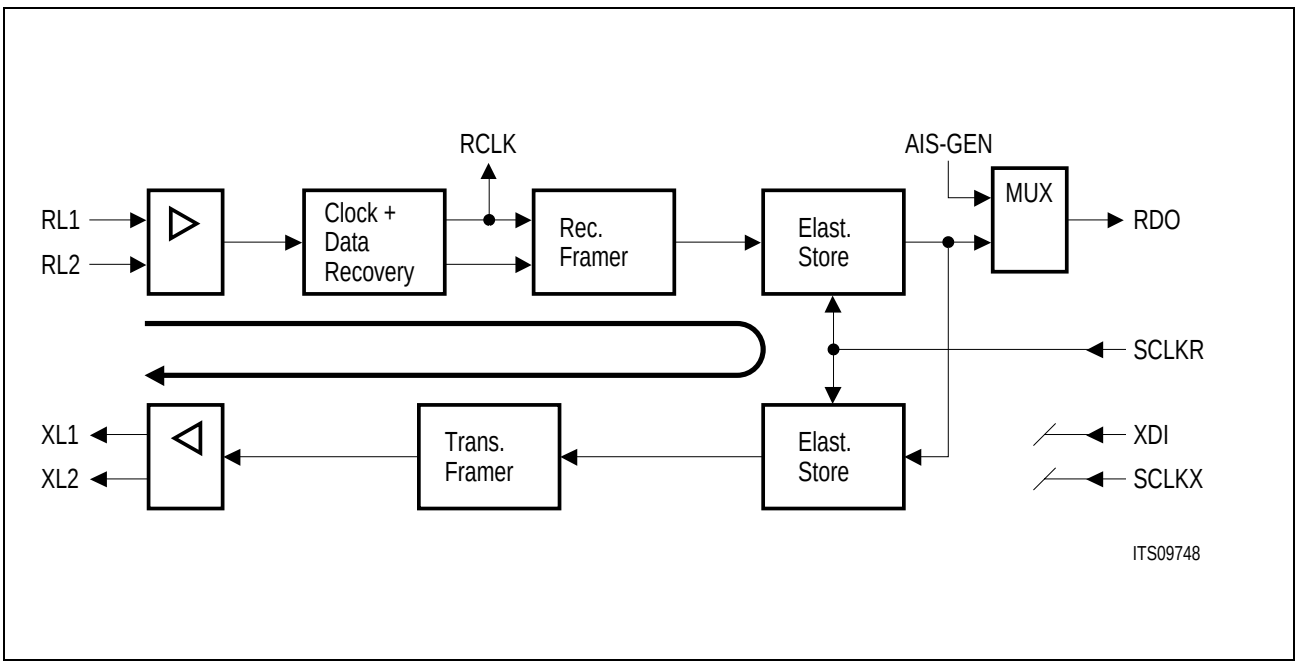


Figure 65
Payload Loop

Remote Loop

In the remote loopback mode the clock and data recovered from the line inputs RL1/2 or RDIP/RDIN are routed back to the line outputs XL1/2 or XDOP/XDON via the analog or digital transmitter. As in normal mode they are also processed by the synchronizer and then sent to the system interface.The remote loopback mode is selected by setting the respective control bits LIM1.RL+JATT. Received data may be looped with or without the transmit jitter attenuator (FIFO).

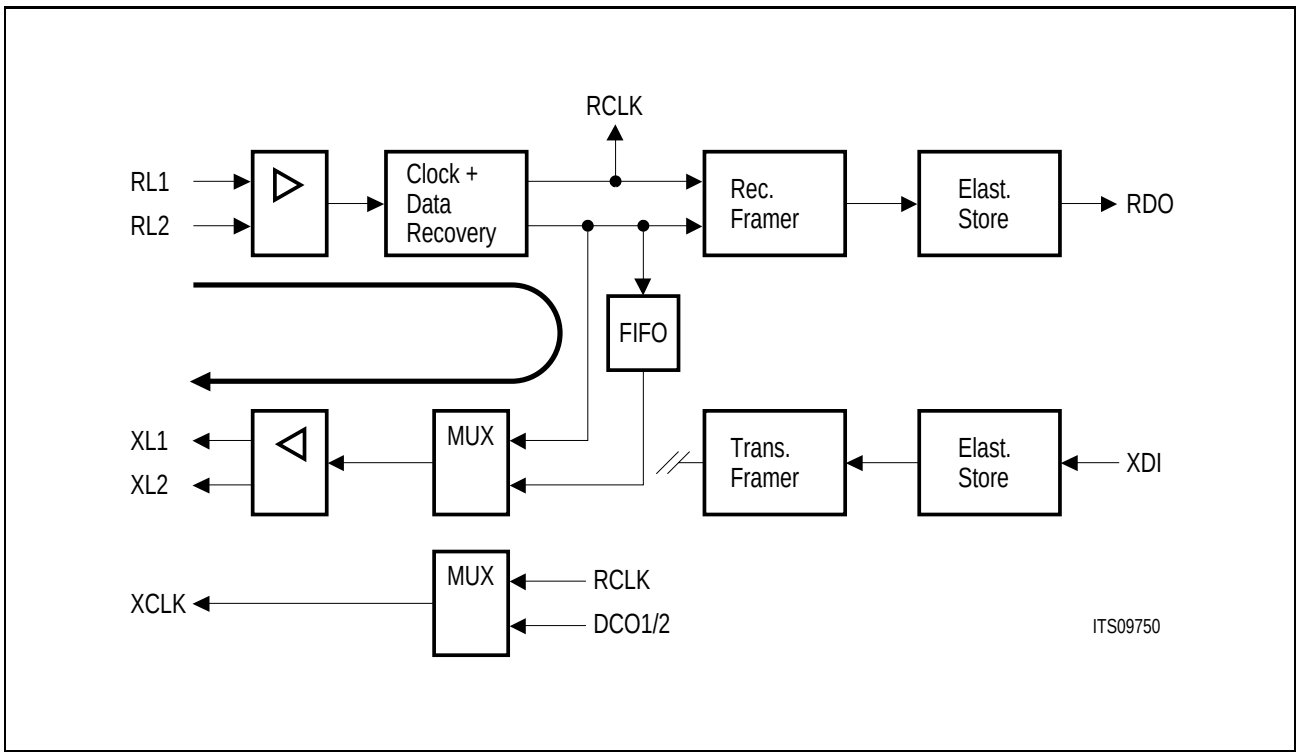


Figure 66
Remote Loop

Local Loop

The local loopback mode, selected by LIM0.LL = 1, disconnects the receive lines RL1/2 or RDIP/RDIN from the receiver. Instead of the signals coming from the line the data provided by system interface are routed through the analog receiver back to the system interface. However, the bit stream will be undisturbed transmitted on the line. However an AIS to the distant end could be enabled by setting FMR1.XAIS without influencing the data looped back to the system interface.

Note that enabling the local loop will usually invoke an out of frame error until the receiver can resync to the new framing. The serial code from the transmitter and receiver has to be programmed identically.

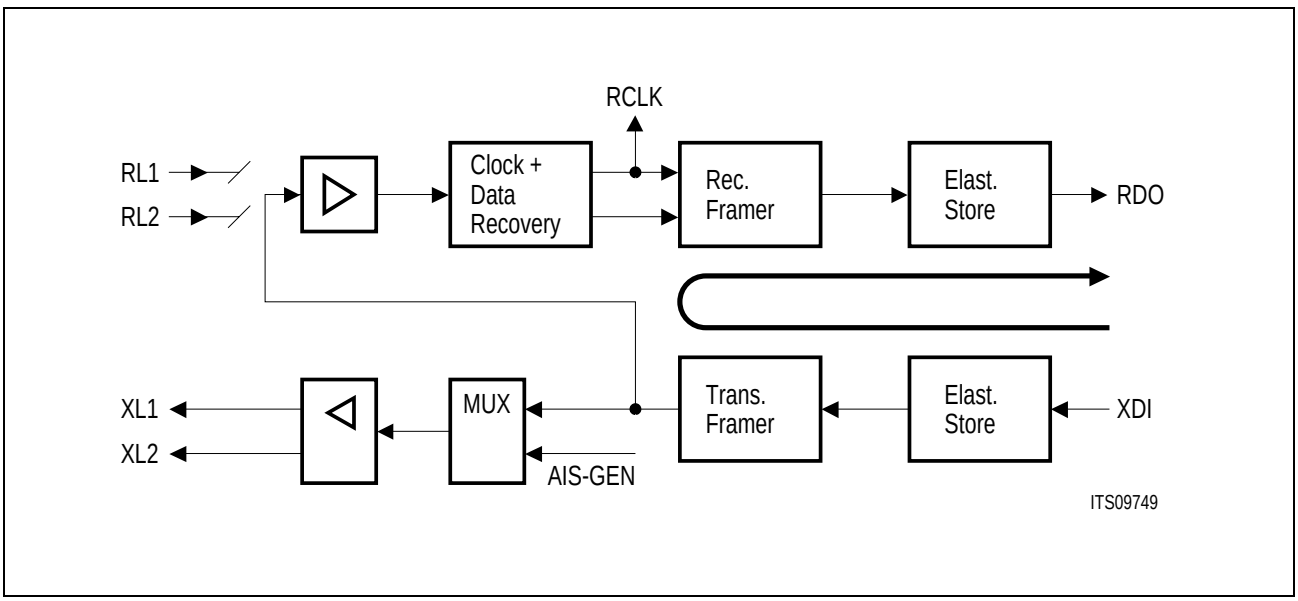


Figure 67
Local Loop

Single Channel Loop (loopback of time-slots)

The channel loopback is selected via LOOP.ECLB = 1.

Each of the 24 time-slots may be selected for loopback from the system PCM input (XDI) to the system PCM output (RDO). This loopback is programmed for one time-slot at a time selected by register LOOP. During loopback, an idle channel code programmed in register IDLE is transmitted to the remote end in the corresponding PCM route time-slot.

For the time-slot test, sending sequences of test patterns like a 1 kHz check signal should be avoided. Otherwise, an increased occurrence of slips in the tested time-slot will disturb testing. These slips do not influence the other time-slots and the function of the receive memory. The usage of a quasi-static test pattern is recommended.

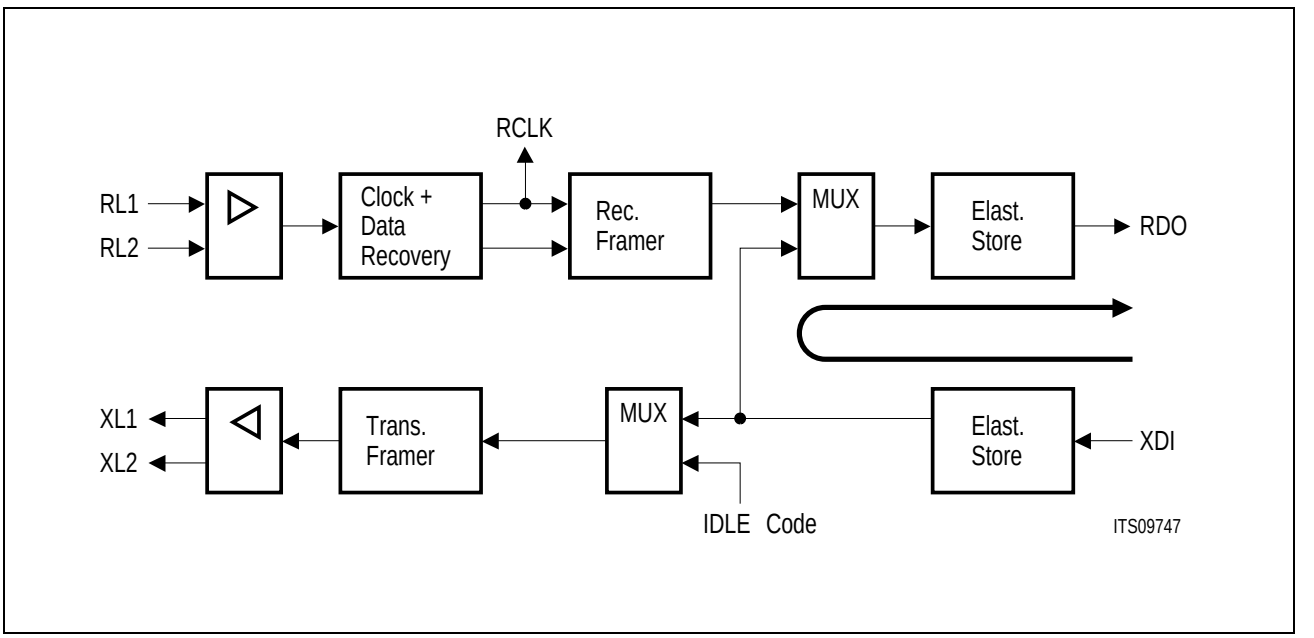


Figure 68
Channel Loopback

Alarm Simulation

Alarm simulation does not affect the normal operation of the device, i.e. all time-slots remain available for transmission. However, possible ‘real’ alarm conditions are not reported to the processor or to the remote end when the device is in the alarm simulation mode.

The alarm simulation is initiated by setting the bit FMR0.SIM. The following alarms are simulated:

- Loss of Signal (red alarm)
- Alarm Indication Signal AIS (blue alarm)
- Loss of pulse frame
- Remote alarm (yellow alarm) indication
- Receive and transmit slip indication
- Framing error counter
- Code violation counter
- CRC6 error counter

Some of the above indications are only simulated if the QuadFALC is configured in a mode where the alarm is applicable.

The alarm simulation is controlled by the value of the Alarm Simulation Counter: FRS2.ESC which is incremented by setting bit: FMR0.SIM.

Clearing of alarm indications:

– Automatically for LOS, remote (yellow) alarm, AIS, and loss of synchronization and

– User controlled for slips by reading the corresponding interrupt status register ISR3.

– Error counter have to be cleared by reading the corresponding counter registers.

is only possible at defined counter steps of FRS2.ESC. For complete simulation (FRS2.ESC = 0), eight simulation steps are necessary.

8 Operational Description T1 / J1

8.1 Signaling Controller Operating Modes

The HDLC controller can be programmed to operate in various modes, which are different in the treatment of the HDLC frame in receive direction. Thus, the receive data flow and the address recognition features can be performed in a very flexible way, to satisfy almost any practical requirements.

There are 4 different operating modes which can be set via the MODE register.

8.1.1 HDLC Mode

All frames with valid addresses are forwarded directly via the RFIFO to the system memory.

Depending on the selected address mode, the QuadFALC can perform a 1 or 2 byte address recognition (MODE.MDS0).

If a 2-byte address field is selected, the high address byte is compared with the fixed value FEH or FCH (group address) as well as with two individually programmable values in RAH1 and RAH2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address will be interpreted as COMMAND/RESPONSE bit (C/R) and will be excluded from the address comparison.

Similarly, two compare values can be programmed in special registers (RAL1, RAL2) for the low address byte. A valid address will be recognized in case the high and low byte of the address field correspond to one of the compare values. Thus, the QuadFALC can be called (addressed) with 6 different address combinations. HDLC frames with address fields that do not match any of the address combinations, are ignored by the FALC.

In case of a 1-byte address, RAL1 and RAL2 will be used as compare registers. The HDLC control field, data in the I-field and an additional status byte are temporarily stored in the RFIFO. Additional information can also be read from a special register (RSIS).

As defined by the HDLC protocol, the QuadFALC perform the zero bit insertion/deletion (bit-stuffing) in the transmit/receive data stream automatically. That means, it is guaranteed that at least after 5 consecutive “1”-s a “0” will appear.

Non-Auto-Mode (MODE.MDS2-1=01)

Characteristics: address recognition, FLAG - and CRC generation/check, bit-stuffing

All frames with valid addresses are forwarded directly via the RFIFO to the system memory.

Transparent Mode 1 (MODE.MDS2-0=101)

Characteristics: address recognition, FLAG - and CRC generation/check, bit-stuffing

Only the high byte of a 2-byte address field will be compared with registers RAH1/2. The whole frame excluding the first address byte will be stored in RFIFO.

Transparent Mode 0 (MODE.MDS2-0=100)

Characteristics: FLAG - and CRC generation/check, bit-stuffing
No address recognition is performed and each frame will be stored in the RFIFO.

Receive Data Flow

The following figure gives an overview of the management of the received HDLC frames in the different operating modes.

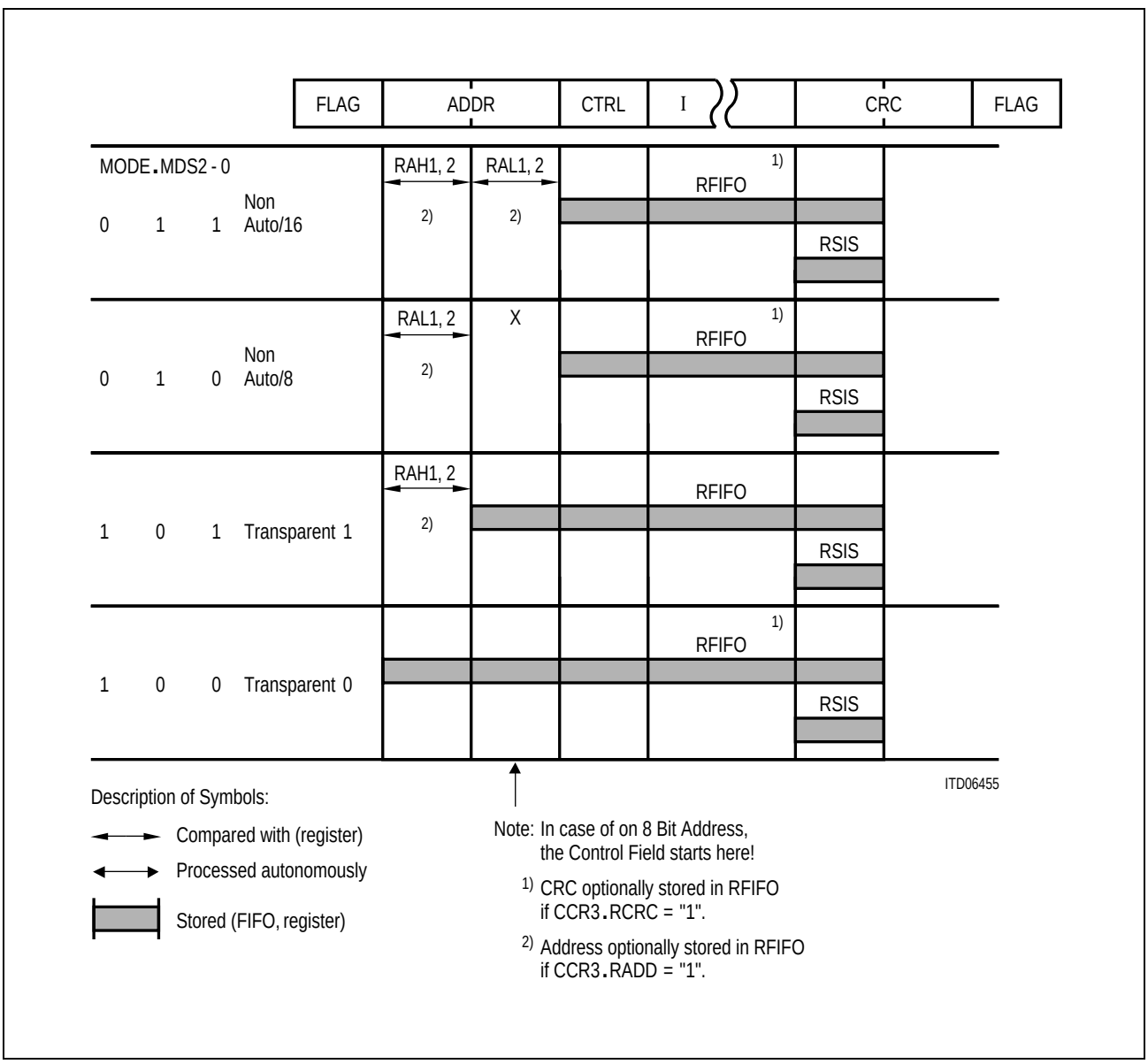


Figure 69
Receive Data Flow of QuadFALC

Transmit Data Flow

The frames can be transmitted as shown below.

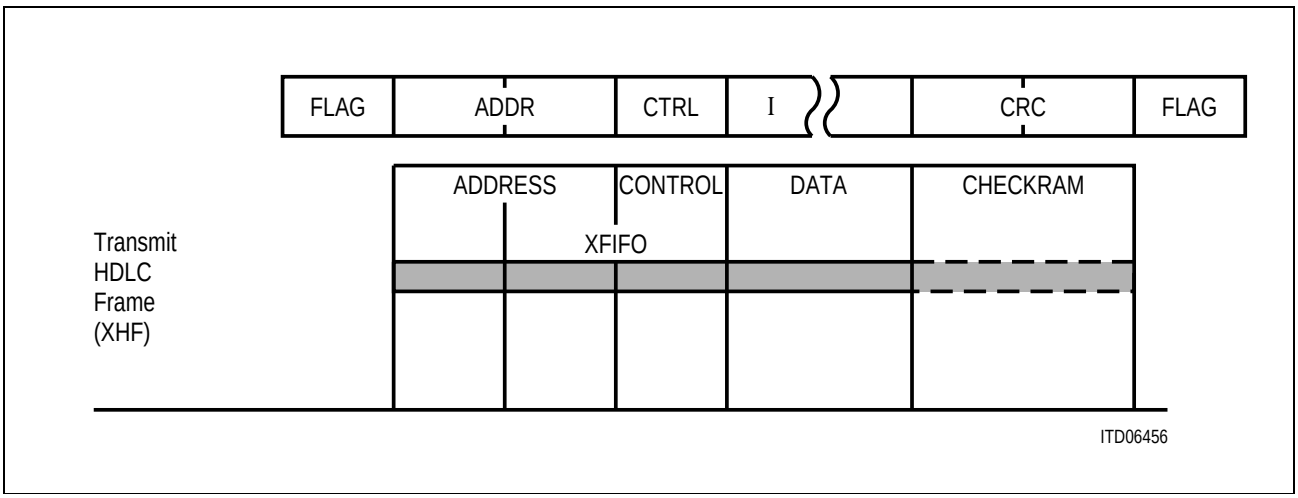


Figure 70
Transmit Data Flow of QuadFALC

Transmitting a HDLC frame via register CMDR.XTF, the address, the control fields and the data field have to be entered in the XFIFO.

If CCR3.XCRC is set, the CRC checksum will not be generated internally. The checksum has to be provided via the transmit FIFO (XFIFO) as the last two bytes. The transmitted frame will be closed automatically only with a (closing) flag.

The QuadFALC does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.

8.1.2 Extended Transparent Mode

Characteristics: fully transparent

In no HDLC mode, fully transparent data transmission/reception without HDLC framing is performed, i.e. without FLAG generation/recognition, CRC generation/check, or bit-stuffing. This feature can be profitably used e.g for:

- Specific protocol variations
- Transmission of a BOM frame
- Test purposes

Data transmission is always performed out of the XFIFO. In transparent mode, the receive data is shifted into the RFIFO.

8.1.3 Signaling Controller Functions

Shared Flags

The closing Flag of a previously transmitted frame simultaneously becomes the opening Flag of the following frame if there is one to be transmitted. The Shared Flag feature is enabled by setting bit SFLG in control register CCR1.

Transparent Transmission and Reception

When programmed in the extended transparent mode via the MODE register (MDS2-0 = 111), the QuadFALC performs fully transparent data transmission and reception without HDLC framing, i.e. without

- FLAG insertion and deletion
- CRC generation and checking
- Bit-stuffing

In order to enable fully transparent data transfer, bit MODE.HRAC has to be set.

Received data is always shifted into RFIFO.

Data transmission is always performed out of XFIFO by directly shifting the contents of XFIFO in the outgoing datastream. Transmission is initiated by setting CMDR.XTF (04_H). A synch-byte FF_H is automatically sent before the first byte of the XFIFO will be transmitted.

Cyclic Transmission (fully transparent)
If the extended transparent mode is selected, the QuadFALC supports the continuous transmission of the contents of the transmit FIFO.

After having written 1 to 32 bytes to XFIFO, the command XREP.XTF via the CMDR register (bit 7 … 0 = '00100100' = 24_H) forces the QuadFALC to transmit the data stored in XFIFO repeatedly to the remote end.

Note: The cyclic transmission continues until a reset command (CMDR: SRES) is issued or with resetting CMDR.XREP, after which continuous '1'-s are transmitted. During cyclic transmission the XREP-bit has to be set with every write operation to CMDR.

CRC ON/OFF Features

As an option in HDLC mode the internal handling of received and transmitted CRC checksum can be influenced via control bits CCR3.RCRC and CCR3.XCRC.

- Receive Direction
  The received CRC checksum is always assumed to be in the 2 (CRC-ITU) last bytes of a frame, immediately preceding a closing flag. If CCR3.RCRC is set, the received CRC checksum will be written to RFIFO where it precedes the frame status byte (contents of register RSIS). The received CRC checksum is additionally checked for

correctness. If HDLC mode is selected, the limits for ‘Valid Frame’ check are modified (refer to description of bit RSIS.VFR).

- Transmit Direction
  If CCR3.XCRC is set, the CRC checksum is not generated internally. The checksum has to be provided via the transmit FIFO (XFIFO) as the last two bytes. The transmitted frame will only be closed automatically with a (closing) flag.
  The QuadFALC does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.

8.1.3.1 HDLC Data Transmission

In transmit direction 2x32 byte FIFO buffers are provided. After checking the XFIFO status by polling the bit SIS.XFW or after an interrupt ISR1.XPR (Transmit Pool Ready), up to 32 bytes may be entered by the CPU to the XFIFO.

The transmission of a frame can be started by issuing a XTF or XHF command via the command register. If the transmit command does not include an end of message indication (CMDR.XME), the QuadFALC will repeatedly request for the next data block by means of a XPR interrupt as soon as no more than 32 bytes are stored in the XFIFO, i.e. a 32-byte pool is accessible to the CPU.

This process will be repeated until the CPU indicates the end of message per XME command, after which frame transmission is finished correctly by appending the CRC and closing flag sequence. Consecutive frames may be share a flag, or may be transmitted as back-to-back frames, if service of XFIFO is quick enough.

In case no more data is available in the XFIFO prior to the arrival of XME, the transmission of the frame is terminated with an abort sequence and the CPU is notified per interrupt ISR1.XDU. The frame may be aborted per software CMDR.SRES.

The data transmission sequence, from the CPU's point of view, is outlined in **figure 71**.

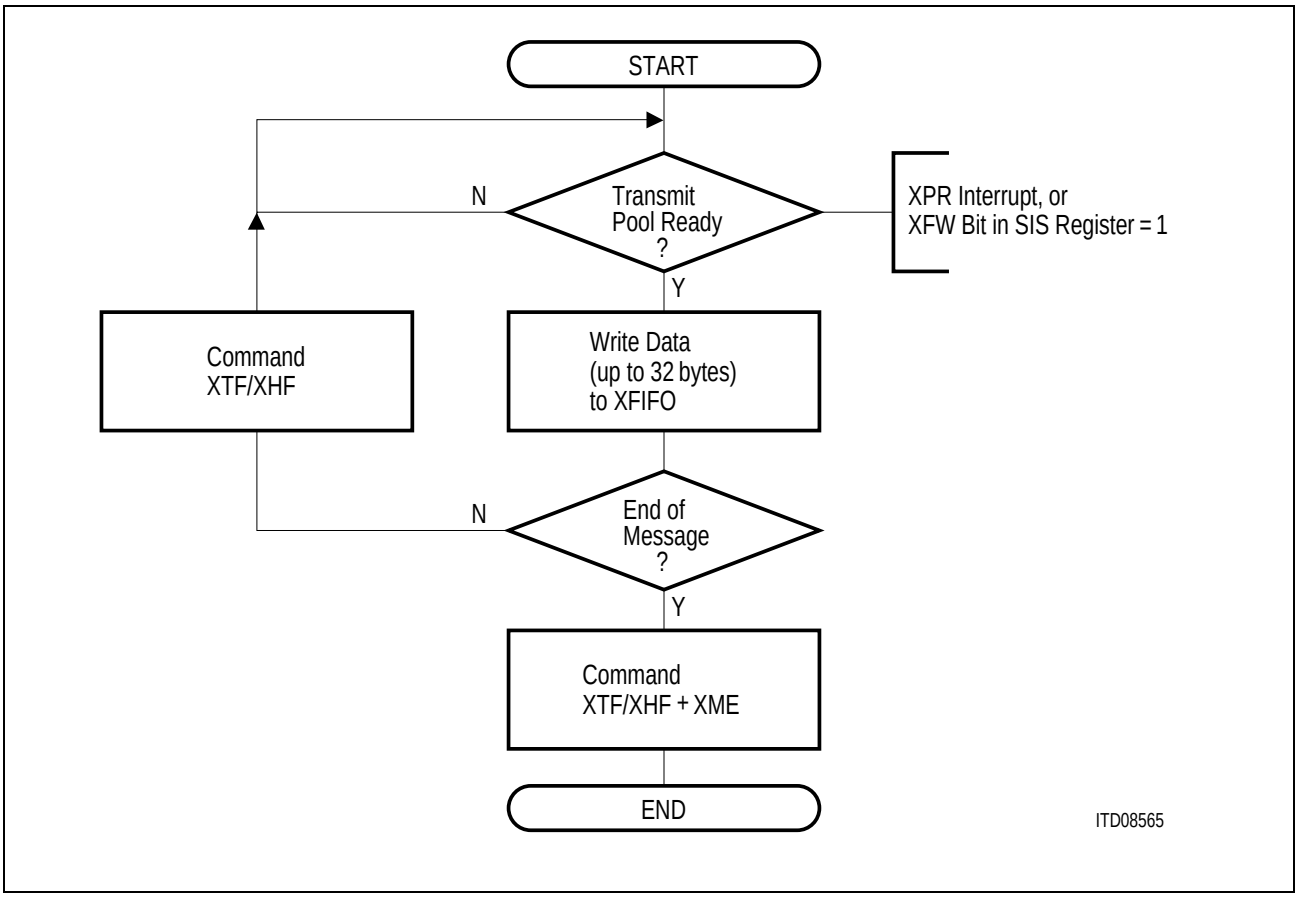


Figure 71
Interrupt Driven Data Transmission (flow diagram)

The activities at both serial and CPU interface during frame transmission (supposed frame length = 70 bytes) is shown in **figure 72**.

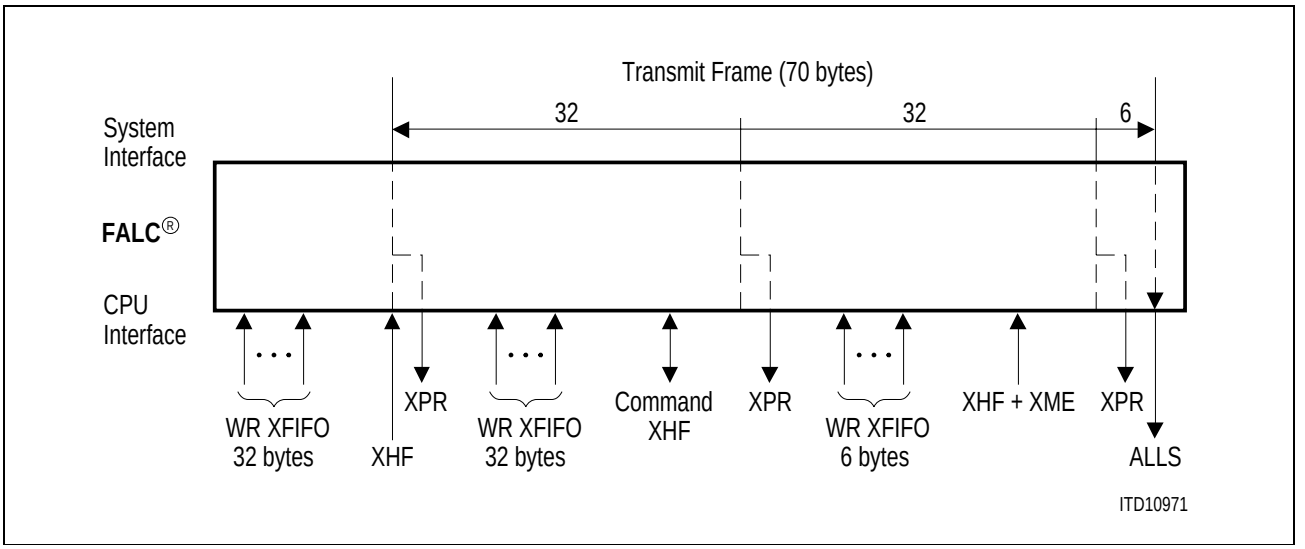


Figure 72
Interrupt Driven Transmission Example

8.1.3.2 HDLC Data Reception

Also 2×32 byte FIFO buffers are provided in receive direction. There are different interrupt indications concerned with the reception of data:

RPF (Receive Pool Full) interrupt, indicating that a 32-byte-block of data can be read from RFIFO and the received message is not yet complete.

RME (Receive Message End) interrupt, indicating that the reception of one message is completed.

The following **figure 73** gives an example of a reception sequence, assuming that a “long” frame (66 bytes) followed by two short frames (6 bytes each) are received.

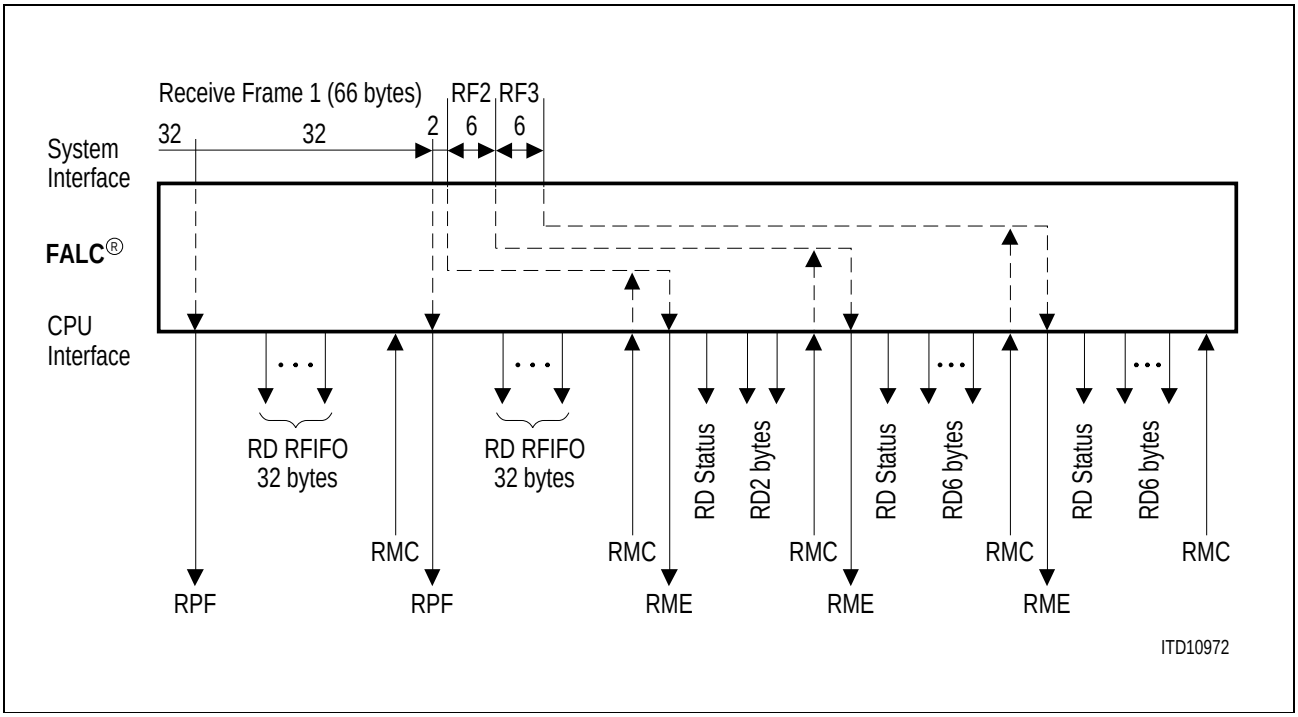


Figure 73
Interrupt Driven Reception Sequence Example

8.1.4 Bit Oriented Message Mode

The QuadFALC supports signaling and maintenance functions for T1 - Primary Rate Interfaces using the Extended Super Frame format. The device supports the DL-channel protocol for ESF format according to T1.403-1989 ANSI or to AT&T TR54016 specification. The HDLC- and Bit Oriented Message (BOM) -Receiver can be switched ON/OFF independently. If the QuadFALC is used for HDLC formats only, the BOM receiver has to be switched off. If HDLC- and BOM-receiver has been switched on

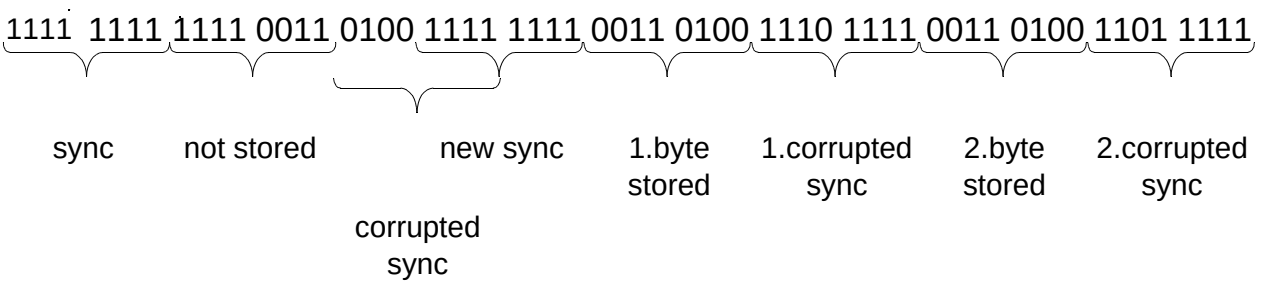
(MODE.HRAC/BRAC), an automatic switching between HDLC and BOM mode is enabled. Storing of received DL bit information in the RFIFO of the signaling controller and transmitting the XFIFO contents in the DL bit positions is enabled by CCR1.EDLX/EITS = 10. After Reset or software-reset (CMDR.RRES) the QuadFALC operates in HDLC mode. If eight or more consecutive ones are detected, the BOM mode is entered. Upon detection of a flag in the data stream, the QuadFALC switches back to HDLC-mode. Operating in BOM-mode, the QuadFALC may receive an HDLC frame immediately, i.e. without any preceding flags.

In BOM-mode, the following byte format is assumed (the left most bit is received first).
111111110xxxxxx0

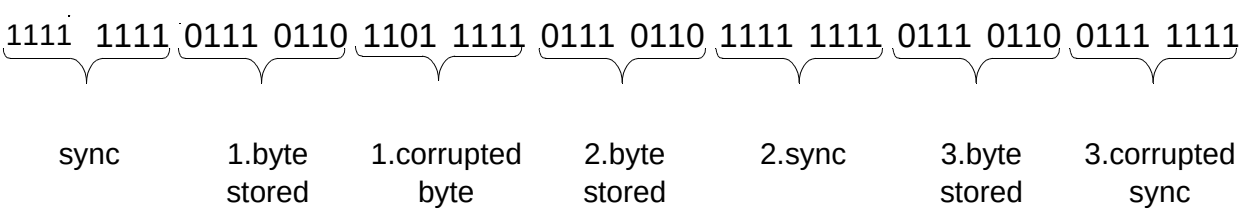
The QuadFALC uses the FF_H byte for synchronization, the next byte is stored in RFIFO (first bit received: LSB) if it starts and ends with a ‘0’. Bytes starting and ending with a ‘1’ are not stored. If there are no 8 consecutive one’s detected within 32 bits, an interrupt is generated. However, byte sampling is not stopped.

Byte sampling in BOM Mode

a)



b)



Three different BOM reception modes may be programmed (CCR1.BRM, CCR2.RBFE).

10 byte packets: CCR1.BRM = 0
After storing 10 bytes in RFIFO the receive status byte marking a BOM frame (RSIS.HFR) is added as the eleventh byte and an interrupt (ISR0.RME) is generated. The sampling of data bytes continues and interrupts are generated every 10 bytes until an HDLC flag is detected.

Continuous reception: CCR1.BRM = 1
Interrupts are generated every 32 (16, 4, 2) bytes. After detecting an HDLC flag, byte sampling is stopped, the receive status byte is stored in RFIFO and an RME interrupt is generated.

Receiption with enabled BOM filter: CCR2.RBFE = 1
The BOM-receiver will only accept BOM frames after detecting 7 out of 10 equal BOM pattern. The BOM pattern is stored in the RFIFO adding a receive status byte, marking a BOM frame (RSIS.HFR) and generating an interrupt status ISR0.RME. The current state of the BOM receiver is indicated in register SIS.IVB. When the valid BOM pattern disappears an interrupt ISR0.BIV is generated.

The user may switch between these modes at any time. Byte sampling may be stopped by deactivating the BOM receiver (MODE.BRAC). In this case the receive status byte is added, an interrupt is generated and HDLC-mode is entered. Whether the QuadFALC operates in HDLC or BOM mode may be checked by reading the Signaling Status Register (SIS.BOM).

8.1.5 4 Kbit/s Data Link Access in F72 Format

The QuadFALC supports the DL-channel protocol using the F72 (SLC96) format as follows:

- Sampling of DL bits is done on a multiframe basis and stored in the registers RDL1-3. A receive multiframe begin interrupt is provided to read the received data DL bits. The contents of registers XDL1-3 is subsequently sent out on the transmit multiframe basis if it is enabled via FMR1.EDL. A transmit multiframe begin interrupt requests for writing new information to the DL-bit registers.
- If enabled via CCR1.EDLX/EITS=10 , the DL bit information from frame 26 to 72 is stored in the Receive FIFO of the signaling controller.The DL bits stored in the XFIFO are inserted in the outgoing datastream. If CCR1.EDLX is cleared, a HDLC- or a transparent- frame could be sent or received via the RFIFO / XFIFO.

8.2 Operational Phase

The QuadFALC is programmable via a microprocessor interface which enables byte or word access to all control and status registers.

After RESET the QuadFALC has to be first initialized. General guidelines for initialization are described in section Initialization.

The status registers are read-only and are continuously updated. Normally, the processor periodically reads the status registers to analyze the alarm status and signaling data.

Reset

The QuadFALC is forced to the reset state if a high signal is input at port RES for a minimum period of 10 µs. During RESET the QuadFALC needs an active clock on pin MCLK. All output stages are tri-stated, all internal flip-flops are reset and most of the control registers are initialized with default values.

After Reset bit FMR1.PMOD has to be set high and the device needs up to 20 µsec to settle up to the internal clocking. After FMR1.PMOD has been set the configuration shown in **table 28** is initialized.

Table 28
Configuration if Initialized after RESET

Register	Initiated Value	Meaning
FMR0	00_H	NRZ Coding, No alarm simulation.
FMR1 FMR2	00_H 00_H	PCM 24 mode, 2.048 MBit/s system data rate, no AIS transmission to remote end or system interface, Payload Loop off, Channel translation mode 0
SIC1 SIC2, SIC3	00_H 00_H 00_H	2.048 MHz system clocking rate, Rec. Buffer 2 Frames, Transmit Buffer bypass, Data sampled or transmitted on the falling edge of SCLKR/X, Automatic freeze signaling, data is active in the first channel phase,
LOOP	00_H	Channel loop back are disabled.
FMR4 FMR5	00_H 00_H	Remote alarm indication towards remote end disabled. LFA condition: 2 out of 4/5/6 framing bits, Non-auto-synchronization mode, F12 multiframing, internal Bit Robbing Access disabled
XC0 XC1	00_H 00_H	The transmit clock-slot offset is cleared. The transmit time-slot Offset is cleared.

Table 28
Configuration if Initialized after RESET (cont'd)

Register	Initiated Value	Meaning
RC0 RC1	00_H 00_H	The receive clock slot offset is cleared. The receive time-slot offset is cleared.
IDLE ICB 1 … 3	00_H 00_H	Idle channel code is cleared. Normal operation (no "Idle Channels" selected).
CCB 1 … 3	00_H	Normal operation (no clear channel operation).
LIM0 LIM1 PCD PCR	00_H 00_H 00_H 00_H	Slave Mode, Local Loop off, Analog interface selected, Remote Loop off Pulse Count for LOS Detection cleared Pulse Count for LOS Recovery cleared
XPM2-0	$00,03,9c_H$	Transmit Pulse Mask
IMR1-4	FF_H	All interrupts are disabled
GCR	00_H	Internal second timer, Power on of all 4 single FALC channels,
CMR1	00_H	DCO-R reference clock: channel 1, RCLK output: DPLL clock, DCO-X enabled, DCO-X internal reference clock
CMR2	00_H	SCLKR selected, SCLKX selected, Rec. synchr. pulse sourced by $\overline{SYPR}$, Tr. synchr. pulse sourced by $\overline{SYPX}$,
GPC1	00_H	system multiplex mode disabled, SEC port input active high, FSC is sourced by channel 1, RCLK1 clock source: channel 1,
PC1-4	00_H , 00_H 00_H , 00_H	Input function of ports RP(A-D) : $\overline{SYPR}$, Input function of ports XP(A-D) : $\overline{SYPX}$
PC5	00_H	SCLKR, SCLKX, RCLK configured to inputs, XMFS active low
RTR1-4 TTR1-4	00_H	No time-slots selected
MODE	00_H	Signaling controller disabled
RAH1/2 RAL1/2	FD_H,FF_H FF_H,FF_H	Compare register for receive address cleared

Initialization

For a correct start up of the Primary Access Interface a set of parameters specific to the system and hardware environment must be programmed after RESET goes inactive. Both the basic and the operational parameters must be programmed **before** the activation procedure of the PCM line starts. Such procedures are specified in ITU-T and DMI recommendations (e.g. Fault conditions and consequent actions). Setting optional parameters primarily makes sense when basic operation via the PCM line is guaranteed. **Table 29** gives an overview of the most important parameters in terms of signals and control bits which are to be programmed in one of the above steps. The sequence is recommended but not mandatory. Accordingly, parameters for the basic and operational set up, for example, may be programmed simultaneously. The bit FMR1.PMOD should always be kept high.

Features like channel loop back, idle channel activation, clear channel activation, extensions for signaling support, alarm simulation, … may be activated later. Transmission of alarms (e.g. AIS, remote alarm) and control of synchronization in connection with consequent actions to remote end and internal system depend on the activation procedure selected.

Table 29
Initialization Parameters

Basic Set Up	**T1**
Mode Select	FMR1.PMOD = 1
Specification of Line interface and clock generation	LIM0, LIM1, XPM2-0
Line interface coding	FMR0.XC1/0, FMR0.RC1/0
Loss of Signal detection/recovery conditions	PCD, PCR, LIM1, LIM2
System clocking and data rate	SIC1.SSC1/0, SIC1.SSD1, FMR1.SSD0 CMR1.IRSP/IRSC/ IXSP/IXSC
channel translation mode	FMR1.CTM
Transmit offset counters	XC0.XCO, XC1.XTO
Receive offset counters	RC0.RCO, RC1.RTO
AIS to system interface	FMR2.DAIS/SAIS
Operational Set Up	**T1**
Select framing	FMR4.FM1/0
Framing additions	FMR1.CRC, FMR0.SRAF
Synchronization mode	FMR4.AUTO, FMR4.SSC1/0, FMR2.MCSP, FMR2.SSP
Signaling mode	FMR5.EIBR, XC0.BRM, MODE, CCR1, CCR2, RAH1/2, RAL1/2

Note: Read access to unused register addresses: value should be ignored.
Write access to unused register addresses: should be avoided, or set to '00'hex.
All control registers (except XFIFO, XS1-12, CMDR, DEC) are of type: Read/Write

8.3 Specific T1 Initialization

The following is a suggestion for a basic initialization to meet most of the T1 requirements. Depending on different applications and requirements any other initialization can be used.

LIU Initialization

FMR0.XC0/1 FMR0.RC0/1 LIM1.DRS CCB1-3	The QuadFALC supports requirements for the analog line interface as well as the digital line interface. For the analog line interface the codes AMI (with and without bit 7stuffing) and B8ZS are supported. For the digital line interface modes (dual or single rail) the QuadFALC supports AMI (with and without bit 7 stuffing) and B8ZS.
PCD = 0x0A	LOS detection after 176 consecutive "zeros" (fulfills G.775 spec, Bellcore/AT&T)
PCR = 0x15	LOS recovery after 22 "ones" in the PCD intervall. (fulfills G.775, Bellcore/AT&T)
LIM1.RIL2-0 = 0x02	LOS threshold of 0.6 V (fulfills G.775).
GCR.SCI = 1	Additional Recovery Interrupts. Help to meet alarm activation and deactivation conditions in time.
LIM2.LOS2/1 = 01	Automatic pulse densitiy check on 15 consecutive zeros for LOS recovery condition (Bellcore requirement)

Framer Initialization

FMR4.SSC1/0	Selection of framing sync conditions
FMR4.FM1/0	Select framing format

FMR2.AXRA = 1	The transmission of RAI via the line interface is done automatically by the QuadFALC in case of Loss of Frame Alignment (FRS0.LFA = 1). If framing has been reinstalled RAI is automatically reset
FMR4.AUTO = 1	Automatic synchronization in case of definite framing candidate (FRS0.FSRF). In case of multiple framing candidates and CRC6 errors different resynchronization conditions can be programmed via FMR2.MCSP/SSP.

Signaling Controller Initialization

Initialization of the HDLC controller:

MODE = 0x88	HDLC Receiver active, No address comparison
CCR1 = 0x18	Enable Signaling via time-slot 0-31, Interframe Time Fill with continous FLAGs
IMR0.RME = 0 IMR0.RPF = 0 IMR1.XPR = 0	Select interrupts for HDLC processor requests
RTR4.0 = 1 XTR4.0 = 1	Select time-slot 24 for HDLC data reception and transmission

Initialization of the CAS-BR Controller

FMR5.EIBR = 1	Enable CAS-BR Mode Send CAS-BR information stored in XS1-12
IMR1.CASE = 0 IMR0.RSC = 0	Enable interrupts which indicate the access to the XS1-12 CAS-BR registers and any data change in RS1-12

After the device initialization a software reset should be executed by setting of bits CMDR.XRES/RRES.

8.4 Control Register Description

Table 30
Control Register Address Arrangement

Address				Register	Type	Comment
00	100	200	300	XFIFO	W	Transmit FIFO
01	101	201	301	XFIFO	W	Transmit FIFO
02	102	202	302	CMDR	W	Command Register
03	103	203	303	MODE	R/W	Mode Register
04	104	204	304	RAH1	R/W	Receive Address High 1
05	105	205	305	RAH2	R/W	Receive Address High 2
06	106	206	306	RAL1	R/W	Receive Address Low 1
07	107	207	307	RAL2	R/W	Receive Address Low 2
08				IPC	R/W	Interrupt Port Configuration
09	109	209	309	CCR1	R/W	Common Configuration Register 1
0A	10A	20A	30A	CCR2	R/W	Common Configuration Register 2
0C	10C	20C	30C	RTR1	R/W	Receive Timeslot Register 1
0D	10D	20D	30D	RTR2	R/W	Receive Timeslot Register 2
0E	10E	20E	30E	RTR3	R/W	Receive Timeslot Register 3
0F	10F	20F	30F	RTR4	R/W	Receive Timeslot Register 4
10	110	210	310	TTR1	R/W	Transmit Timeslot Register 1
11	111	211	311	TTR2	R/W	Transmit Timeslot Register 2
12	112	212	312	TTR3	R/W	Transmit Timeslot Register 3
13	113	213	313	TTR4	R/W	Transmit Timeslot Register 4
14	114	214	314	IMR0	R/W	Interrupt Mask Register 0
15	115	215	315	IMR1	R/W	Interrupt Mask Register 1
16	116	216	316	IMR2	R/W	Interrupt Mask Register 2
17	117	217	317	IMR3	R/W	Interrupt Mask Register 3
18	118	218	318	IMR4	R/W	Interrupt Mask Register 4
1C	11C	21C	31C	FMR0	R/W	Framer Mode Register 0
1D	11D	21D	31D	FMR1	R/W	Framer Mode Register 1
1E	11E	21E	31E	FMR2	R/W	Framer Mode Register 2
1F	11F	21F	31F	LOOP	R/W	Channel Loop Back

Table 30
Control Register Address Arrangement

Address				Register	Type	Comment
20	120	220	320	FMR4	R/W	Framer Mode Register 4
21	121	221	321	FMR5	R/W	Framer Mode Register 5
22	122	222	322	XC0	R/W	Transmit Control 0
23	123	223	323	XC1	R/W	Transmit Control 1
24	124	224	324	RC0	R/W	Receive Control 0
25	125	225	325	RC1	R/W	Receive Control 1
26	126	226	326	XPM0	R/W	Transmit Pulse Mask 0
27	127	227	327	XPM1	R/W	Transmit Pulse Mask 1
28	128	228	328	XPM2	R/W	Transmit Pulse Mask 2
2B	12B	22B	32B	IDLE	R/W	Idle Channel Code
2C	12C	22C	32C	XDL1	R/W	Transmit DL-Bit Register 1
2D	12D	22D	32D	XDL2	R/W	Transmit DL-Bit Register 2
2E	12E	22E	32E	XDL3	R/W	Transmit DL-Bit Register 3
2F	12F	22F	32F	CCB1	R/W	Clear Channel Register 1
30	130	230	330	CCB2	R/W	Clear Channel Register 2
31	131	231	331	CCB3	R/W	Clear Channel Register 3
32	132	232	332	ICB1	R/W	Idle Channel Register 1
33	133	233	333	ICB2	R/W	Idle Channel Register 2
34	134	234	334	ICB3	R/W	Idle Channel Register 3
36	136	236	336	LIM0	R/W	Line Interface Mode 0
37	137	237	337	LIM1	R/W	Line Interface Mode 1
38	318	238	338	PCD	R/W	Pulse Count Detection
39	139	239	339	PCR	R/W	Pulse Count Recovery
3A	13A	23A	33A	LIM2	R/W	Line Interface Register 2
3B	13B	23B	33B	LCR1	R/W	Loop Code Register 1
3C	13C	23C	33C	LCR2	R/W	Loop Code Register 2
3D	13D	23D	33D	LCR3	R/W	Loop Code Register 3
3E	13E	23E	33E	SIC1	R/W	System Interface Control 1
3F	13F	23F	33F	SIC2	R/W	System Interface Control 2

Table 30
Control Register Address Arrangement

Address				Register	Type	Comment
40	140	240	340	SIC3	R/W	System Interface Control 3
44	144	244	344	CMR1	R/W	Clock Mode Register 1
45	145	245	345	CMR2	R/W	Clock Mode Register 2
46	146	246	346	GCR1	R/W	Global Configuration Register 1
47	147	247	347	ESM	R/W	Errored Second Mask
60	160	260	360	DEC	W	Disable Error Counter
70	170	270	370	XS1	W	Transmit Signaling Register 1
71	171	271	371	XS2	W	Transmit Signaling Register 2
72	172	272	372	XS3	W	Transmit Signaling Register 3
73	173	273	373	XS4	W	Transmit Signaling Register 4
74	174	274	374	XS5	W	Transmit Signaling Register 5
75	175	275	375	XS6	W	Transmit Signaling Register 6
76	176	276	376	XS7	W	Transmit Signaling Register 7
77	177	277	377	XS8	W	Transmit Signaling Register 8
78	178	278	378	XS9	W	Transmit Signaling Register 9
79	179	279	379	XS10	W	Transmit Signaling Register 10
7A	17A	27A	37A	XS11	W	Transmit Signaling Register 11
7B	17B	27B	37B	XS12	W	Transmit Signaling Register 12
80	180	280	380	PC1	R/W	Port Configuration 1
81	181	281	381	PC2	R/W	Port Configuration 2
82	182	282	382	PC3	R/W	Port Configuration 3
83	183	283	383	PC4	R/W	Port Configuration 4
84	184	284	384	PC5	R/W	Port Configuration 5
85				GPC1	R/W	Global Port Configuration 1

After ‘RESET’ all control registers except the XFIFO and XS1-12 are initialized to defined values.

Unused bits have to be set to logical ‘0’.

The status registers are only readable and are updated by the QuadFALC.

Transmit FIFO (WRITE) XFIFO

	7							0	
XFIFO	XF7							XF0	(x00/x01)

Up to 32 bytes/16 words of received data can be read from the RFIFO following an RPF or an RME interrupt.
Writing data to XFIFO can be done in 8-bit (byte) or 16-bit (word) access. The LSB is transmitted first.

Up to 32 bytes/16 words of transmit data can be written to the XFIFO following an XPR (or ALLS) interrupt.

Command Register (Write)

Value after RESET: 00_H

	7							0	
CMDR	RMC	RRES	XREP	XRES	XHF	XTF	XME	SRES	(x02)

RMC… **Receive Message Complete**

Confirmation from CPU to QuadFALC that the current frame or data block has been fetched following an RPF or RME interrupt, thus the occupied space in the RFIFO can be released.

RRES… **Receiver Reset**

The receive line interface except the clock and data recovery unit (DPLL), the receive framer, the one second timer and the receive signaling controller are reset. However the contents of the control registers will not be deleted.

XREP… **Transmission Repeat**

If XREP is set to one together with XTF (write 24H to CMDR), the QuadFALC repeatedly transmits the contents of the XFIFO (1…32 bytes) without HDLC framing fully transparently, i.e. without FLAG,CRC.

The cyclic transmission is stopped with an SRES command or by resetting XREP.

Note: During cyclic transmission the XREP- bit has to be set with every write operation to CMDR.

XRES… **Transmitter Reset**

The transmit framer and transmit line interface excluding the system clock generator and the pulse shaper will be reset. However the contents of the control registers will not be deleted.

XHF… **Transmit HDLC Frame**

After having written up to 32 bytes to the XFIFO, this command initiates the transmission of a HDLC frame.

XTF… **Transmit Transparent Frame**

Initiates the transmission of a transparent frame without HDLC framing.

XME… **Transmit Message End**

Indicates that the data block written last to the transmit FIFO completes the current frame. The QuadFALC can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data.

SRES… **Signaling Transmitter Reset**

The transmitter of the signaling controller will be reset. XFIFO is cleared of any data and an abort sequence (seven 1's) followed by interframe time fill is transmitted. In response to XRES an XPR interrupt is generated.

This command can be used by the CPU to abort a frame currently in transmission.

Note: The maximum time between writing to the CMDR register and the execution of the command takes 2.5 periods of the current system data rate. Therefore, if the CPU operates with a very high clock rate in comparison with the QuadFALC's clock, it is recommended that bit SIS.CEC should be checked before writing to the CMDR register to avoid any loss of commands.

Mode Register (Read/Write)

Value after RESET: 00_H

	7							0	
MODE	MDS2	MDS1	MDS0	BRAC	HRAC	DIV			(x03)

MDS2-0… **Mode Select**

The operating mode of the HDLC controller is selected.

000… Reserved
001… Reserved
010… 1 byte address comparison mode (RAL1, 2)
011… 2 byte address comparison mode (RAH1, 2 and RAL1, 2)
100… No address comparison
101… 1 byte address comparison mode (RAH1, 2)
110… Reserved
111… No HDLC framing mode 1

BRAC… **BOM Receiver Active**

Switches the BOM receiver to operational or inoperational state.

0… Receiver inactive

1… Receiver active

HRAC… **HDLC Receiver Active**

Switches the HDLC receiver to operational or inoperational state.

0… Receiver inactive
1… Receiver active

DIV… **Data Inversion**

Setting this bit will invert the internal generated HDLC data stream.

0… normal operation, HDLC data stream not inverted
1… HDLC data stream inverted

Receive Address Byte High Register 1 (Read/Write)
Value after RESET: FD_H

	7	…	1	0	
RAH1			0		(x04)

In operating modes that provide high byte address recognition, the high byte of the received address is compared with the individually programmable values in RAH1 and RAH2.

RAH1… **Value of the First Individual High Address Byte**

Bit 1 (C/R-bit) is excluded from address comparison.

Receive Address Byte High Register 2 (Read/Write)
Value after RESET: FF_H

	7							0	
RAH2									(x05)

RAH2… **Value of Second Individual High Address Byte**

Receive Address Byte Low Register 1 (Read/Write)
Value after RESET: FF_H

	7							0	
RAL1									(x06)

RAL1… **Value of First Individual Low Address Byte**

Receive Address Byte Low Register 2 (Read/Write)
Value after RESET: FF_H

	7							0	
RAL2									(x07)

RAL2... **Value of the second individually programmable low address byte.**

Interrupt Port Configuration (READ/WRITE)

Value after RESET: 00_H

	7							0	
IPC						SSYF	IC1	IC0	(08)

Unused bits have to be set to logical ‘0’.

SSYF… **Select SYNC Frequency**

Only appilcable in master mode (LIM0.MAS = 1) and bit CMR2.DCF is cleared.

0… Reference clock at port SYNC is 1.544 / 2.048 MHz
1… Reference clock at port SYNC is 8 KHz

IC0, IC1… Interrupt Port Configuration

These bits define the function of the interrupt output stage (pin INT):

IOC1	IOC0	Function
X	0	Open drain output
0	1	Push/pull output, active low
1	1	Push/pull output, active high

Common Configuration Register 1 (READ/WRITE)

Value after RESET: 00_H

	7							0	
CCR1		BRM	EDLX	EITS	ITF	XMFA	RFT1	RFT0	(x09)

BRM… BOM Receive Mode (significant in BOM mode only)

0… 10 byte packets

1… Continuous reception

EDLX… Enable DL Bit Access via the Transmit FIFO

A one in this bit position enables the internal DL- bit access via the receive / transmit FIFO of the signaling controller. FMR1.EDL has to be cleared switching the DL bits, stored in the XFIFO transparently through the QuadFALC.

EITS… Enable Internal Time-Slot 0-31 Signaling

0… Internal signaling in time-slots 0-31 defined via registers RTR1-4 or TTR1-4 is disabled.

1… Internal signaling in time-slots 0-31 defined via registers RTR1-4 or TTR1-4 is enabled.

ITF… Interframe Time Fill

Determines the idle (= no data to send) state of the transmit data coming from the signaling controller.

0… Continuous logical ‘1’ is output

1… Continuous FLAG sequences are output (‘01111110’ bit patterns)

XMFA … **Transmit Multiframe Aligned**

Determines the synchronization between the framer and the corresponding signaling controller.

0… Contents of the XFIFO is transmitted without multiframe alignment.

1… Contents of the XFIFO is transmitted multiframe aligned. If CCR1.EDLXis set, transmitting of DL bits is started in F72 format with frame 26.
After receiving a complete multiframe in the time-slot mode (RTR1-4) an ISR0.RME interrupt is generated, if no HDLC or BOM mode is enabled. In DL bit access (CCR1.EDLX/EITS = 10) XMFA is not valid.

Note: During the transmission of the XFIFO content, the $\overline{SYPX}$ or XMFS interval time should not be changed, otherwise the XFIFO data has to be retransmitted.

RFT1, RFT0… **RFIFO Threshold Level**

The size of the accessible part of RFIFO can be determined by programming these bits. The number of valid bytes after an RPF interrupt is given in the following table:

RFT1	RFT0	Size of Accessible Part of RFIFO
0	0	32 bytes (RESET value)
0	1	16 bytes
1	0	4 bytes
1	1	2 bytes

The value of RFT 1,0 can be changed dynamically

– If reception is not running or

– after the current data block has been read, but before the command CMDR.RMC is issued (interrupt controlled data transfer).

*Note: It is seen that changing the value of RFT1,0 is possible even during the reception of one frame. The total length of the received frame can be always read directly in RBCL, RBCH after an RPF interrupt, except when the threshold is increased during reception of that frame. The real length can then be inferred by noting which bit positions in RBCL are reset by an RMC command (see **table below**):*

RFT1	RFT0	Bit Positions in RBCL Reset by a CMDR.RMC Command
0	0	RBC4 …. 0
0	1	RBC3 … 0
1	0	RBC1,0
1	1	RBC0

Common Configuration Register 2 (READ/WRITE)

Value after RESET: 00_H

	7							0	
CCR2				RADD	RBFE	RCRC	XCRC		(x0A)

Unused bits have to be set to logical ‘0’.

RADD… **Receive Address Pushed to RFIFO**

If this bit is set to ‘1’, the received HDLC address information (1 or 2 bytes, depending on the address mode selected via MODE.MDS0) is pushed to RFIFO. This function is applicable in non-auto mode.

RBFE… **Receive BOM Filter Enable**

Setting this bit the Bit Oriented Message (BOM) -receiver will only accept BOM frames after detecting 7 out of 10 equal BOM pattern. The BOM pattern is stored in the RFIFO adding a receive status byte marking a BOM frame (RSIS.HFR) and an interrupt ISR0.RME is generated. The current state of the BOM receiver is indicated in register SIS.IVB. When the valid BOM pattern disappears an interrupt ISR0.BIV is generated.

RCRC… **Receive CRC ON/OFF**

Only applicable in non-auto mode.

If this bit is set to ‘1’, the received CRC checksum will be written to RFIFO (CRC-ITU-T: 2 bytes). The checksum, consisting of the 2 last bytes in the received frame, is followed in the RFIFO by the status information byte (contents of register RSIS). The received CRC checksum will additionally be checked for correctness. If non-auto mode is selected, the limits for “Valid Frame” check are modified (refer to **RSIS.VFR**).

XCRC… **Transmit CRC ON/OFF**

If this bit is set to '1', the CRC checksum will not be generated internally. It has to be written as the last two bytes in the transmit FIFO (XFIFO). The transmitted frame will be closed automatically with a closing flag.

Note: The QuadFALC does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.

Receive Timeslot Register 1-4 (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H

	7							0	
RTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7	(x0C)
RTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	(x0D)
RTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	(x0E)
RTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	(x0F)

TS0…TS31… **Timeslot Register**

These bits define the received time-slots on the system highway port RDO to be extracted. Additionally these registers will control the RSIGM marker which can be forced high during the respective time-slots independently of bit CCR1.EITS.
A one in the RTR1-4 bits will sample the corresponding time-slot in the RFIFO of the signaling controller, if bit CCR1.EITS is set.

Assignments:
SIC2.SSC2 = 0 : (32 time-slots / frame)
TS0 → time-slot 0, . . . TS31→ time-slot 31
SIC2.SSC2 = 1 : (24 time-slots / frame)
TS0 → time-slot 0, . . . TS23→ time-slot 23

0 … The corresponding time-slot is not extracted and stored in the RFIFO.
1… The contents of the selected time-slot will be stored in the RFIFO. Although the idle time-slots can be selected. This function will only become active, if bits CCR1.EITS is set.
The corresponding time-slot will be forced high on pin RSIGM.

Transmit Timeslot Register 1-4 (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H

	7							0	
TTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7	(x10)
TTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	(x11)
TTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	(x12)
TTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	(x13)

TS0…TS31… Transmit Timeslot Register

These bits define the transmit time-slots on the system highway to be inserted. Additionally these registers will control the XSIGM marker which can be forced high during the respective time-slots independently of bit CCR1.EITS.
A one in the TTR1-4 bits will insert the corresponding time-slot sourced by the XFIFO in the data received on pin XDI, if bit CCR1.EITS is set. If SIC3.TTRF is set and CCR1.EDLX/EITS=00, insertion of data received on port XSIG is controlled by this registers.

Assignments:
SIC2.SSC2 = 0 : (32 time-slots / frame)
TS0 → time-slot 0, . . . TS31→ time-slot 31
SIC2.SSC2 = 1 : (24 time-slots / frame)
TS0 → time-slot 0, . . . TS23→ time-slot 23

0 … The selected time-slot will not be inserted into the outgoing data stream.

1…The contents of the selected time-slot will be inserted in the outgoing data stream from XFIFO. This function will only become active, if bits CCR1.EITS is set.
The corresponding time-slot will be forced high on marker pin XSIGM.

Interrupt Mask Register 0…4

Value after RESET: FF_H, FF_H, FF_H, FF_H,FF_H

	7							0	
IMR0	RME	RFS	ISF	RMB	RSC	CRC6	PDEN	RPF	(x14)
IMR1	CASE	RDO	ALLS	XDU	XMB		XLSC	XPR	(x15)
IMR2	FAR	LFA	MFAR	LMFA	AIS	LOS	RAR	RA	(x16)
IMR3	ES	SEC			LLBSC		RSN	RSP	(x17)
IMR4	XSP	XSN							(x18)

IMR0...IMR4... **Interrupt Mask Register**

Each interrupt source can generate an interrupt signal at port INT (characteristics of the output stage are defined via register IPC). A ‘1’ in a bit position of IMR0…4 sets the mask active for the interrupt status in ISR0…4. Masked interrupt statuses neither generate a signal on INT, nor are they visible in register GIS. Moreover, they will

– not be displayed in the Interrupt Status Register if bit GCR.VIS is set to ‘0’

– be displayed in the Interrupt Status Register if bit GCR.VIS is set to ‘1’.

After RESET, all interrupts are **dis**abled.

Framer Mode Register 0 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR0	XC1	XC0	RC1	RC0	FRS	SRAF	EXLS	SIM	(x1C)

XC1…XC0… Transmit Code

Serial code transmitter is independent to the receiver.

00… NRZ (optical interface)
01… CMI (1T2B + B8ZS), (optical interface)

10… AMI coding with Zero Code Suppression (ZCS, B7 - Stuffing). Disabling of the ZCS is done by activating the clear channel mode via register CCB1-3. (ternary or digital interface)
11… B8ZS Code (ternary or digital dual rail interface)

RC1…RC0… Receive Code

Serial code receiver is independent to the transmitter.

00… NRZ (optical interface)
01… CMI (1T2B + B8ZS), (optical interface)
10… AMI coding with Zero Code Suppression (ZCS, B7 - Stuffing), (ternary or digital dual rail interface)
11… B8ZS Code (ternary or digital dual rail interface)

FRS… Force Resynchronization

A transition from low to high will force the frame aligner to execute a resynchronization of the pulse frame. In the asynchronous state, a new frame position is assumed at the next candidate if there is one. Otherwise, a new frame search with the meaning of a general reset is started. In the synchronous state this bit will have the same meaning as bit FMR0.EXLS except if FMR2.MCSP=1.

SRAF… Select Remote (Yellow) Alarm Format for F12 and ESF Format

0… F12: bit2 = 0 in every channel. ESF: pattern ‘1111 1111 0000 0000…’ in data link channel.
1… F12: FS bit of frame 12. ESF: bit2 = 0 in every channel

EXLS… External Loss Of Frame

With a low to high transition a new frame search will be started. This has the meaning of a general reset of the internal frame alignment unit. Synchronous state is reached only if there is one definite framing candidate. In the case of multiple candidates, the setting of the bit

FMR0.FRS forces the receiver to lock onto the next available framing position.

SIM… **Alarm Simulation**

Setting/resetting this bit initiates internal error simulation of: AIS (blue alarm), loss of signal (red alarm), loss of frame alignment, remote (yellow) alarm, slip, framing errors, CRC errors, code violations. The error counters FEC, CVC, CEC, EBC will be incremented.

The selection of simulated alarms is done via the error simulation counter: FRS2.ESC2-0 which will be incremented with each setting of bit FMR0.SIM. For complete checking of the alarm indications eight simulation steps are necessary (FRS2.ESC2-0 = 0 after a complete simulation).

Framer Mode Register 1 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR1	CTM		EDL	PMOD	CRC	ECM	SSD0	XAIS	(x1D)

CTM… **Channel Translation Mode**

0… Channel translation mode 0

1… Channel translation mode 1

EDL… **Enable DL-Bit Access via Register XDL1-3**

Only applicable in F4, F24 or F72 frame format.

0… Normal operation. The DL-bits will be taken from system highway or if enabled via CCR1.EDLX from the XFIFO of the signaling controller.

1… DL-bit register access. The DL-bit information will be taken from the registers XDL1-3 and will overwrite the DL-bits received at the system highway (pin XDI) or the internal XFIFO of the signaling controller. However, transmitting contents of registers XDL1-3 will be disabled if transparent mode is enabled (FMR4.TM).

PMOD… **PCM Mode**

For T1 application this bit must be set high. Switching into T1 mode the device needs up to 10 µsec to settle up to the internal clocking.

FMR1.PMOD of all 4 channels has to be set equally.

0… PCM 30 or E1 mode.

1… PCM 24 or T1 mode.

CRC… Enable CRC6

This bit is only significant when using the ESF format.

0… CRC6 check/generation disabled. For transmit direction, all CRC bit positions are set to ‘1’.

1… CRC6 check/generation enabled.

ECM… Error Counter Mode

The function of the error counters (FEC,CEC,CVC,EBC) will be determined by this bit.

0… Before reading an error counter the corresponding bit in the Disable Error Counter register (DEC) has to be set. In 8 bit access the low byte of the error counter should always be read before the high byte. The error counters will be reset with the rising edge of the corresponding bits in the DEC register.

1… Every second the error counter will be latched and then automatically be reset. The latched error counter state should be read within the next second. Reading the error counter during updating should be avoided.

SSD0… Select System Date Rate 0

SIC1.SSD1, FMR1.SSD0 and SIC2.SSC2 define the data rate on the system highway. Programming SSD1/SSD0 and corresponding data rate is shown below.

SIC2.SSC2 = 0:

00…2.048 MBit/s

01…4.096 MBit/s

10…8.192 MBit/s

11…16.384 MBit/s

SIC2.SSC2 = 1:

00…1.544 MBit/s

01…3.088 MBit/s

10…6.176 MBit/s

11…12.352 MBit/s

XAIS… **Transmit AIS Towards Remote End**

Sends AIS (blue alarm) via ports: XL1, XL2 towards the remote end.

If Local Loop Mode is enabled the transmitted data is looped back to the system internal highway without any changes.

Framer Mode Register 2 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR2		MCSP	SSP	DAIS	SAIS	PLB	AXRA	EXZE	(x1E)

MCSP… **Multiple Candidates Synchronization Procedure**

SSP… **Select Sync/Resync Procedure**

Together with bit FMR2.SSP the synchronization mode of the receive framer is defined:

MCSP/SSP:

00… F12/72 format:
Specified number of errors in both FT framing and FS framing lead to loss of sync (FRS0.LFA is set). In the case of FS bit framing errors, bit FRS0.LMFA is set additionally. A complete new synchronization procedure is initiated to regain pulseframe alignment and then multiframe alignment.

F24:
normal operation: synchronization is achieved only on verification the framing pattern.

01… F12/72:
Specified number of errors in FT framing has the same effect as above. Specified number of errors in FS framing only initiates a new search for multiframe alignment without influencing pulseframe synchronous state (FRS0.LMFA is set).

F24:
Synchronous state is reached when three consecutive multiframe pattern are correctly found independent of the occurence of CRC6 errors.

10…

A one will enable a synchronization mode which is able to choose multiple framing pattern candidates step by step. I.e. if in synchronous state the CRC error counter indicates that the

synchronization might have been based on an alias framing pattern, setting of FMR0.FRS will lead to synchronization on the next candidate available. However, only the previously assumed candidate will be discarded in the internal framing pattern memory. The latter procedure can be repeated until the framer has locked on the right pattern (no extensive CRC errors). Therefor bit FMR1.CRC must be set.

11… F24:
Synchronization is achieved on verification the framing pattern **and** the CRC6 bits. Synchronous state is reached when framing pattern and CRC6 checksum are correctly found. For correct operation the CRC check must be enabled by setting bit FMR1.CRC6.

DAIS… Disable AIS to System Interface

0… AIS is automatically inserted into the data stream to RDO if QuadFALC is in asynchronous state.

1… Automatic AIS insertion is disabled. Furthermore, AIS insertion can be initiated by programming bit FMR2.SAIS.

SAIS… Send AIS Towards System Interface

Sends AIS (blue alarm) via output RDO towards system interface. This function is not influenced by bit FMR2.DAIS.

PLB… Payload Loop Back

0 … Normal operation. Payload loop is disabled.

1… The payload loopback will loop the data stream from the receiver section back to transmitter section. Looped data is output on pin RDO. Data received at port XDI, XSIG, $\overline{\text{SYPX}}$ and XMFS will be ignored. With FMR4.TM=1 all 193 bits per frame will be looped back. If FMR4.TM=0 the DL- or FS- or CRC- bits will be generated internally. AIS is sent immediately on port RDO by setting the FMR2.SAIS bit. During payload loop is active the receive time-slot offset (registers RC1/0) should not be changed. A write access to register XC1 will set the read/write pointer of the transmit elastic buffer into its optimal position to ensure a maximum wander compensation.

AXRA… Automatic Transmit Remote Alarm

0 … Normal operation

1… The Remote Alarm (yellow alarm) bit will be automatically set in the outgoing data stream if the receiver is in asynchronous

state (FRS0.LFA bit is set). In synchronous state the remote alarm bit will be reset.

EXZE… Excessive Zeros Detection Enable

Selects error detection mode in the bipolar receive bit stream.

0… Only bipolar violations are detected.

1… Bipolar violations and zero strings of 8 or more contiguous zeros in B8ZS code or more than 15 contiguous zeros in AMI code are detected additionally and counted in the code violation counter CVC.

LOOP (Read/Write)

Value after RESET: 00_H

	7				0	
LOOP		RTM	ECLB	CLA4	CLA0	(x1F)

RTM… Receive Transparent Mode

Setting this bit disconnects control of the internal elastic store from the receiver. The elastic store is now in a “free running” mode without any possibility to actualize the time slot assignment to a new frame position in case of re-synchronization of the receiver. This function can be used in conjunction with the “disable AIS to system interface” feature (FMR2.DAIS) to realize undisturbed transparent reception.
This bit should be enabled in case of unframed data reception mode.

ECLB… Enable Channel Loop Back

0… Disables the channel loop back.

1… Enables the channel loop back selected by this register.

CLA4…CLA0… Channel Address For Loop Back

CLA = 1…24 selects the channel.

During loop back, the contents of the associated outgoing channel at ports XL1/XDOP/XOID and XL2/XDON is equal to the idle channel code programmed in register IDLE.

Framer Mode Register 4 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR4	AIS3	TM	XRA	SSC1	SSC0	AUTO	FM1	FM0	(x20)

AIS3… **Select AIS Condition**

0… AIS (blue alarm) is indicated (FRS0.AIS) when two or less zeros in the received bit stream are detected in a time interval of 12 frames (F4, F12, F72) or 24 frames (ESF).

1… AIS (blue alarm) detection is only enabled when QuadFALC is in asynchronous state. The alarm is indicated (FRS0.AIS) when

– three or less zeros within a time interval of 12 frames (F4, F12, F72), or

– five or less zeros within a time interval of 24 frames (ESF) are detected in the received bit stream.

TM… **Transparent Mode**

Setting this bit enables the transparent mode:

In transmit direction bit 8 of every FS/DL time-slot from the system internal highway (XDI) is inserted in the F-bit position of the outgoing frame. Internal framing generation, insertion of CRC and DL data is disabled.

XRA… **Transmit Remote Alarm (Yellow Alarm)**

If high, remote alarm is sent via PCM route. Clearing the bit will remove the remote alarm pattern. Remote alarm indication depends on the multiframe structure as follows:

F4: bit2 = 0 in every speech channel
F12: – FMR0.SRAF = 0: bit2 = 0 in every speech channel
– FMR0.SRAF = 1: FS-bit of frame 12 is forced to ‘1’
ESF: – FMR0.SRAF = 0: pattern ‘1111111100000000 11111111000…’ in data link channel
– FMR0.SRAF = 1: bit2 = 0 in every speech channel
F72: bit2 = 0 in every speech channel

SSC1/0… **Select Sync Conditions**

Loss of Frame Alignment (FRS0.LFA or opt. FRS0.LMFA) is declared if
00 = 2 out of 4 framing bits

01 = 2 out of 5 framing bits
10 = 2 out of 6 framing bits in F4/12/72 format
10 = 2 out of 6 framing bits per multiframe period in ESF format
11 = 4 consecutive multiframe pattern in ESF format
are incorrect.
are incorrect. It depends on the selected multiframe format and optionally on bit FMR2.SSP which framing bits are observed:

F4: FT bits → FRS0.LFA
F12, F72: SSP = 0: FT bits → FRS0.LFA: FS bits → FRS0.LFA
and FRS0.LMFA SSP = 1:FT → FRS0.LFA
FS → FRS0.LMFA
ESF: ESF framing bits → FRS0.LFA

AUTO… Enable Auto Resynchronization

0… The receiver will not resynchronize automatically. Starting a new synchronization procedure is possible via the bits: FMR0.EXLS or FMR0.FRS.

1… Auto-resynchronization is enabled.

FM1…FM0… Select Frame Mode

FM = 0: 12-frame multiframe format (F12, D3/4)
FM = 1: 4-frame multiframe format (F4)
FM = 2: 24-frame multiframe format (ESF)
FM = 3: 72-frame multiframe format (F72, remote switch mode)

Framer Mode Register 5 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR5		EIBR	XLD	XLU		XTM	SSC2		(x21)

EIBR… Enable Internal Bit Robbing Access

0… Normal operation.

1… A one in this bit position will cause the transmitter to send the bit robbing signaling information stored in the XS1-12 (ESF, F12, 72) registers in the corresponding time slots.

XLD… Transmit Line Loopback (LLB) Down Code

0… Normal operation.

1… A one in this bit position will cause the transmitter to replace normal transmit data with the LLB Down (Deactuate) Code

continuously until this bit is reset. The LLB Down Code will be optionally overwritten by the framing/DL/CRC bits.

XLU… Transmit LLB UP Code

0… Normal operation.

1… A one in this bit position will cause the transmitter to replace normal transmit data with the LLB UP (actuate) Code continuously until this bit is reset. The LLB UP Code will be optionally overwritten by the framing/DL/CRC bits. For proper operation bit FMR5.XLD must be cleared.

XTM… Transmit Transparent Mode

0…Ports $\overline{\text{SYPX}}$ / XMFS define the frame / multiframe begin on the transmit system highway. The transmitter is usually synchronized on this externally sourced frame boundary and generates the FS/DL bits according to this framing. Any change of the transmit time-slot assignment will subsequently produce a change of the FS/DL bit positions.

1… Disconnects the control of the transmit system interface from the transmitter. The transmitter is now in a free running mode without any possibility to actualize the multiframe position. The framing (FS/DL bits) generated by the transmitter will not be „disturbed“ (in case of changing the transmit time-slot assignment) by the transmit system highway unless register XC1 is written. This bit should be set if loop-timed application is selected. For proper operation the transmit elastic buffer (2 frames, SIC1.XBS1/0= 10) has to be enabled.

SSC2… Select Sync Conditions

Only valid in ESF framing format.
Loss of Frame Alignment FRS0.LFA is declared if more than 320 CRC6 errors per second interval are detected.

Transmit Control 0 (Read/Write)

Value after RESET: 00_H

	7							0	
XC0	BRM	MFBS			BRFO	XCO10		XCO8	(x22)

BRM… **Enable Bit Robbing Marker**

A one in this bit will mark the robbed bit positions on the system highway. RSIGM marks the receive and XSIGM marks the transmit robbed bits.

MFBS… **Enable pure Multiframe Begin Signals**

Only valid if ESF or F72 format is selected.

If set, signals RMFB and XMFB indicate only the multiframe begin. Additional pulses (every 12 frames) are disabled.

BRFO… **Bit Robbing Force One**

Setting this bit forces the robbed bits high transmitted on port RDO. The received signaling data stream for the signaling controller is not influenced by this bit.

XCO10…XCO8… **Transmit Offset**

Initial value loaded into the transmit bit counter at the trigger edge of SCLKX when the synchronous pulse at port $\overline{\text{SYPX}}$ or XMFS is active Refer to register XC1.

Transmit Control 1 (Read/Write)

Value after RESET: $9C_H$

	7			0	
XC1	XTO7			XTO0	(x23)

A write access to this address resets the transmit elastic buffer to its basic starting position. Therefore, updating the value should only be done when the QuadFALC is initialized or when the buffer should be centered. As a consequence a transmit slip may occur.

XTO7…XTO0… **Transmit Offset**

Initial value loaded into the transmit bit counter at the trigger edge of SCLKX when the synchronous pulse at port $\overline{\text{SYPX}}$ / XMFS is active (see **figure 55+56**).

Calculation of delay time T (SCLKX cycles) depends on the value X of the „Transmit Offset“ register XC1/0:

system clocking rate: modulo 2.048 MHz (SIC2.SSC2 = 0)
0 ≤ T ≤ 3 + (SC/SD) : X = 3 - T + (SC/SD)
4+ (SC/SD) ≤ T ≤ max. delay : X = 2051 - T + (SC/SD)

with max. delay = (256 * SC/SD) -1
with SC = System clock defined by SIC1.SSC1/0 + SIC2.SSC2
with SD = system data rate

or

system clocking rate: modulo 1.544 MHz (SIC2.SSC2 = 1)
0 ≤ T ≤ 3 + (7*SC/BF) + (SC/SD): -->
X = 3 - T + (7*SC/BF) + (SC/SD)
4 + (7*SC/BF) + (SC/SD) ≤ T ≤ max. delay : -->
X = 3 - T + (200 * SC/BF) + (SC/SD)

with max. delay = (200 * SC/SD) - (7*SC/SD) -1
with SC = System clock defined by SIC1.SSC1/0 + SIC2.SSC2
with SD = system data rate
with BF = Basic Frequency = 1.544 MHz

Delay time T = time between beginning of time-slot 0 (bit 0 , channel phase 0) at XDI / XSIG and the initial edge of SCLKX after $\overline{\text{SYPX}}$ / XMFS goes active.

Receive Control 0 (Read/Write)

Value after RESET: 00_H

	7							0	
RCO	SJR	RRAM	CRCI	XCRCI	RDIS	RCO10	RCO9	RCO8	(x24)

SJR… Select Japanese ITU-T Requirements

0… Alarm handling is done according ITU-T G. 704+706

1… Alarm handling is done according ITU-T JG. 704 + 706

RRAM… Receive Remote Alarm Mode

The conditions for remote (yellow) alarm (FRS0.RRA) detection can be selected via this bit to allow detection even in the presence of BER 10**-3:

RRAM = 0
Detection
F4: bit2 = 0 in every speech channel per frame.
F12: – FMR0.SRAF = 0: bit2 = 0 in every speech channel per frame.

– FMR0.SRAF = 1: S-bit of frame 12 is forced to ‘1’

ESF: – FMR0.SRAF = 0: pattern ‘1111 1111 0000 0000…’ in data link channel

– FMR0.SRAF = 1: bit2 = 0 in every speech channel

F72: bit2 = 0 in every speech channel per frame.

Release: The alarm will be reset when above conditions are no longer detected.

RRAM = 1 (BER 10**-3)

Detection

F4: bit2 = 0 in 255 consecutive speech channels.

F12: – FMR0.SRAF = 0: bit 2 = 0 in 255 consecutive speech channels.

– FMR0.SRAF = 1: S-bit of frame 12 is forced to ‘1’

ESF: – FMR0.SRAF = 0: pattern ‘1111 1111 0000 0000…’ in data link channel

– FMR0.SRAF = 1: bit 2 = 0 in 255 consecutive speech channels

F72: bit 2 = 0 in 255 consecutive speech channels.

Release

Depending on the selected multiframe format the alarm will be reset when QuadFALC does not detect

– the ‘bit 2 = 0’ condition for three consecutive pulseframes (all formats if selected),

– the ‘FS bit’ condition for three consecutive multiframes (F12),

– the ‘DL pattern’ for three times in a row (ESF).

CRCI… Automatic CRC6 Bit Inversion

If set, all CRC bits of one outgoing extended multiframe are inverted in case a CRC error is flagged for the previous received multiframe. This function is logically ORed with RC0.XCRCI.

XCRCI… Transmit CRC6 Bit Inversion

If set, the CRC bits in the outgoing data stream are inverted before transmission. This function is logically ORed with RC0.CRCI.

RDIS… Receive Data Input Sense

0… Inputs: RDIP, RDIN active low, input ROID is active high

1… Inputs: RDIP, RDIN active high, input ROID is active low

RCO10…RCO8… Receive Offset / Receive Frame Marker Offset

Depending on the RP(A-D) pin function different offsets could be programmed. The $\overline{\text{SYPR}}$ and the RFM pin function could not be selected in parallel.

Receive Offset (PC(1-4).RPC(2-0) = 000)
Initial value loaded into the receive bit counter at the trigger edge of SCLKR when the synchronous pulse at port $\overline{\text{SYPR}}$ is active (see **figure 51**).

Calculation of delay time T (SCLKR cycles) depends on the value X of the „Receive Offset“ register RC1/0. Refer to register RC1.

Receive Control 1 (Read/Write)

Value after RESET: $9C_H$

	7			0	
RC1	RTO7			RTO0	(x25)

RTO7…RTO0… Receive Offset / Receive Frame Marker Offset

Depending on the RP(A-D) pin function different offsets could be programmed. The $\overline{\text{SYPR}}$ and the RFM pin function could not be selected in parallel.

Receive Offset (PC(1-4).RPC(2-0) = 000)
Initial value loaded into the receive bit counter at the trigger edge of SCLKR when the synchronous pulse at port $\overline{\text{SYPR}}$ is active (see **figure 51**).

Calculation of delay time T (SCLKR cycles) depends on the value X of the „Receive Offset“ register RC1/0:

system clocking rate: modulo 2.048 MHz (SIC2.SSC2 = 0)
$0 \leq T \leq 4$: X= 4- T
$5 \leq T \leq$ max. delay : X= 2052 - T

with max. delay = (256*SC/SD) -1
with SC = System clock defined by SIC1.SSC1/0 + SIC2.SSC2
with SD = 2.048 MHz
or

system clocking rate: modulo 1.544 MHz (SIC2.SSC2 = 1)
$0 \leq T \leq 4$: X = 4- T + (7* SC/SD)
$5 \leq T \leq$ max. delay : X = (200 * SC/SD) + 4 - T

with max. delay = 193*SC/SD - 1
with SC = System clock defined by SIC1.SSC1/0 + SIC2.SSC2
with SD = 1.544 MHz

Delay time T = time between beginning of time-slot 0 at RDO and the initial edge of SCLKR after $\overline{SYPR}$ goes active.

Receive Frame Marker Offset (PC(1-4).RPC(2-0) = 001)

Offset programming of the receive frame marker which is output on multifunction port RFM. The receive frame marker could be activated during any bit position of the entire frame and depends on the selected system clock rate.

Calculation of the value X of the „Receive Offset“ register RC1/0 depends on the bit position BP which should be marked :

system clocking rate: modulo 2.048 MHz (SIC2.SSC2 = 0)
0 ≤ BP ≤ 2045 : X= BP + 2
2046 ≤ BP ≤2047 : X= BP - 2046)

e.g: 2.048 MBit/s: BP = 0-255; 4.096 MBit/s: BP = 0-511, 8.192 MBit/s: BP = 0-1023, 16.384 MBit/s: BP = 0-2047

system clocking rate: modulo 1.544 MHz (SIC2.SSC2 = 1)
0 ≤ BP ≤ 193*(SC/SD) -3 : X = BP + 2 + 7*SC/SD
193*(SC/SD) -2 ≤ BP ≤ max. Delay : X = BP + 2 - 186*SC/SD

with max. delay = 193*SC/SD - 1
with SC = System clock defined by SIC1.SSC1/0 + SIC2.SSC2
with SD = 1.544 MHz

Transmit Pulse-Mask 2…0 (Read/Write)

Value after RESET: $7B_H$, 03_H, 00_H

	7							0	
XPM0	XP12	XP11	XP10	XP04	XP03	XP02	XP01	XP00	(x26)
XPM1	XP30	XP24	XP23	XP22	XP21	XP20	XP14	XP13	(x27)
XPM2	XLLP	XLT	DAXLT		XP34	XP33	XP32	XP31	(x28)

The transmit pulse shape which is defined in ANSI T1. 102 will be output on pins XL1 and XL2. The level of the pulse shape can be programmed via registers XPM2-0 to create a custom waveform. In order to get an optimized pulse shape for the external transformers each pulse shape will be internally devided into four sub pulse shapes. In each sub pulse shape a programmed 5 bit value will define the level of the analog voltage on pins XL1/2. Together four 5 bit values have to be programmed to form one complete transmit pulse shape.The four 5 bit values will be sent in the following sequence:

XP04-00: First pulse shape level
XP14-10: Second pulse shape level

XP24-20: Third pulse shape level
XP34-30: Fourth pulse shape level

Changing the LSB of each subpulse in registers XPM2-0 will change the amplitude of the differential voltage on XL1/2 by approximately 80 mV.
The XPM- values in the following table are based on simulations. They are valid for the following external circuitry: transformer ratio: 1:2.4; cable: PULB 22AWG (100 Ω); serial resistors: 2 Ω. Adjustment of these coefficients may be necessary for other external conditions.

DS1: The XPMxx register values shown in the table below are in decimal format.

Range in m	XP04-XP00	XP14-XP10	XP24-XP20	XP34-XP30
0 - 35	27	24	02	01
25 - 65	27	24	02	01
55 - 95	29	25	02	01
85 - 125	29	25	03	01
115 - 155	29	25	04	01
145 - 185	29	26	04	02
175 - 210	29	27	05	02

XLT… **Transmit Line Tri-state**

0 … Normal operation

1 … Transmit line XL1/XL2 or XDOP/XDON are switched into high impedance state. If this bit is set the transmit line monitor status information will be frozen.

DAXLT... **Disable Automatic Tristating of XL1/2**

0... Normal operation. If a short is detected on pins XL1/2 the transmit line monitor will set the XL1/2 outputs into a high impedance state.

1... If a short is detected on pins XL1/2 an automatic setting these pins into a high impedance state (by the XL-monitor) will be disabled.

XLLP… **Reserved**

0… Normal operation

1… Reserved (not to be used)

Idle Channel Code Register (Read/Write)

Value after RESET: 00_H

	7							0	
IDLE	IDL7							IDL0	(x2B)

IDL7…IDL0… Idle Channel Code

If channel loop back is enabled by programming the register LOOP.ECLB = 1, the contents of the assigned outgoing channel at ports XL1/XL2 respective XDOP/XDON is set equal to the idle channel code selected by this register.

Additionally, the specified pattern overwrites the contents of all channels of the outgoing PCM frame selected via the idle channel registers ICB1…ICB3. IDL7 will be transmitted first.

Transmit DL-Bit Register 1-3 (Read/Write)

Value after RESET: 00_H, 00_H, 00_H

	7							0	
XDL1	XDL17	XDL16	XDL15	XDL14	XDL13	XDL12	XDL11	XDL10	(x2C)
XDL2	XDL27	XDL26	XDL25	XDL24	XDL23	XDL22	XDL21	XDL20	(x2D)
XDL3	XDL37	XDL36	XDL35	XDL34	XDL33	XDL32	XDL31	XDL30	(x2E)

XDL1…XDL3… Transmit FS/DL-Bit Data

The DL-bit register access is enabled by setting bits FMR1.EDL = 1. With the transmit multiframe begin an interrupt ISR1.XMB is generated and the contents of these registers XDL1-3 will be copied into a shadow register. The contents will subsequently sent out in the data stream of the next outgoing multiframe if no transparent mode is enabled. XDL10 will be sent out first.

In F4 frame format only XDL10+XDL11 will be transmitted. In F24 frame format XDL10-XDL23 will be shifted out. In F72 frame format XDL10-XDL37 will be transmitted.

The transmit multiframe begin interrupt (XMB) requests that these registers should be serviced. If requests for new information will be ignored, current contents will be repeated.

Clear Channel Register (Read/Write)

Value after RESET: 00_H, 00_H, 00_H

	7							0	
CCB1	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8	(x2F)
CCB2	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	(x30)
CCB3	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	(x31)

CH1…CH24… Channel Selection Bits

0… Normal operation. Bit robbing information and Zero Code Suppression (ZCS, B7 stuffing) may change contents of the selected speech/data channel if assigned modes are enabled via bits FMR5.EIBR and FMR0.XC1/0.

1… Clear channel mode. Contents of selected speech/data channel will not be overwritten by internal or external bit robbing and ZCS information. Transmission of channel assigned signaling and control of pulse density is applied by the user.

Idle Channel Register (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H

	7							0	
ICB1	IC1	IC2	IC3	IC4	IC5	IC6	IC7	IC8	(x32)
ICB2	IC9	IC10	IC11	IC12	IC13	IC14	IC15	IC16	(x33)
ICB3	IC17	IC18	IC19	IC20	IC21	IC22	IC23	IC24	(x34)

IC1…IC24… Idle Channel Selection Bits

These bits define the channels (time-slots) of the outgoing PCM frame to be altered.

0… Normal operation.

1… Idle channel mode. The contents of the selected channel is overwritten by the idle channel code defined via register IDLE.

Line Interface Mode 0 (Read/Write)

Value after RESET: 00_H

	7						0		
LIM0	XFB	XDOS			EQON		LL	MAS	(x36)

XFB… **Transmit Full Bauded Mode**

Only applicable for dual rail mode (bit LIM1.DRS = 1).

0…Output signals XDOP/XDON are half bauded (normal operation).

1…Output signals XDOP/XDON are full bauded.

Note: If CMI coding is selected (FMR0.XC1/0=01) this bit has to be cleared.

XDOS… **Transmit Data Out Sense**

0… Output signals XDOP/XDON are active low. Output XOID is active high (normal operation).

1… Output signals XDOP/XDON are active high. Output XOID is active low.

Note: If CMI coding is selected (FMR0.XC1/0=01) this bit has to be cleared.
The transmit frame marker XFM is independent of this bit.

EQON… **Receive Equalizer On**

0… -10 dB Receiver: short haul mode

1… -36 dB Receiver: long haul mode

LL… **Local Loop**

0 … Normal operation

1 … Local loop active. The local loopback mode disconnects the receive lines RL1/RL2 respective RDIP/RDIN from the receiver. Instead of the signals coming from the line the data provided by system interface are routed through the analog receiver back to the system interface. The unipolar bit stream will be undisturbed transmitted on the line. Receiver and transmitter coding must be identical. Operates in analog and digital line interface mode. In analog line interface mode data is transfered through the complete analog receiver.

MAS… **Master Mode**

0 … Slave mode

1 … Master mode on. Setting this bit the DCO-R circuitry is frequency synchronized to the clock (1.544 or 2.048 MHz) supplied by SYNC. If this pin is connected to VSS or VDD the DCO-R circuitry is centered and no receive jitter attenuation is performed. The generated clocks are stable.

Line Interface Mode 1 (Read/Write)

Value after RESET: 00_H

	7							0	
LIM1		RIL2	RIL1	RIL0	DCOC	JATT	RL	DRS	(x37)

RIL2…RIL0… Receive Input Threshold

Only valid if analog line interface is selected (LIM1.DRS=0.

No signal will be declared if the voltage between pins RL1 and RL2 drops below the limits programmed via bits RIL2-0 and the received data stream has no transition for a period defined in the PCD register.

The threshold where no signal will be declared is programmable via the RIL2-0 bits depending of bit LIM0.EQON.

LIM0.EQON = 0 (short haul mode):

000 = 0.9 V
001 = 0.7 V
010 = 0.6 V
011 = 0.4 V
100 = 0.3 V
101 = 0.2 V
110 = 0.07 V
111 = 0.05 V

LIM0.EQON = 1 (long haul mode):

000 = 1.7 V
001 = 0.8 V
010 = 0.8 V
011 = 0.5 V
100 = 0.5 V
101 = 0.2 V
110 = 0.1 V
111 = not assigned

DCOC … **DCO-R Control**

0… 1.544 MHz reference clock for the DCO-R circuitry provided on pin SYNC.

1… 2.048 MHz reference clock for the DCO-R circuitry provided on pin SYNC.

JATT…RL... **Transmit Jitter Attenuator / Remote Loop**

00 = Normal operation. The transmit jitter attenuator is disabled. Transmit data will bypass the buffer.

01 = Remote Loop active without transmit jitter attenuator enabled. Transmit data will bypass the buffer.

10 = not assigned

11 = Remote Loop and jitter attenuator active. Received data from pins RL1/2 or RDIP/N or ROID will be sent jitter free on ports XL1/2 or XDOP/N or XOID. The dejittered clock is generated by the DCO-X circuitry.

DRS… **Dual Rail Select**

0 = The ternary interface is selected. Multifunction ports RL1/2 and XL1/2 become analog in/outputs.

1 = The digital dual rail interface is selected. Received data is latched on multifunction ports RDIP/RDIN while transmit data is output on pins XDOP/XDON.

Pulse Count Detection Register (Read/Write)

Value after RESET: 00_H

	7		0	
PCD	PCD7		PCD0	(x38)

PCD7…PCD0… Pulse Count Detection

A LOS alarm (red alarm) will be detected if the incoming data stream has no transitions for a programmable number T consecutive pulse positions. The number T is programmable via the PCD register and can be calculated as follows:
T= 16(N+1) ; with 0 =< N =< 255.

The maximum time is: $256 \times 16 \times 648$ ns = 2.65 ms. Every detected pulse will reset the internal pulse counter. The counter will be clocked with the receive clock RCLK.

Pulse Count Recovery (Read/Write)

Value after RESET: 00_H

	7							0	
PCR	PCR7							PCR0	(x39)

PCR7…PCR0… Pulse Count Recovery

A LOS alarm (red alarm) will be cleared if a pulse density is detected in the received bit stream.The number of pulses M which must occur in the predefined PCD time interval is programmable via the PCR register and can be calculated as follows:

M = N+1 ; with 0 =< N =< 255.

The time interval starts with the first detected pulse transition. With every received pulse a counter will be incremented and the actual counter is compared with the contents of PCR register. If the pulse number >= the PCR value the LOS alarm will be reset otherwise the alarm will still be active. In this case the next detected pulse transition will start a new time interval.

An additional Loss of Signal recovery condition may be selected by register LIM2.LOS1.

Line Interface Mode 2 (Read/Write)

Value after RESET: 00_H

	7							0	
LIM2	LBO2	LBO1			SCF	ELT		LOS1	(x3A)

LBO2...LBO1… Line Build-Out

In long haul applications LIM0.EQON = 1 a transmit filter can be optionally placed on the transmit path to attenuate the data on pins XL1/2. Selecting the transmitter attenuation is possible in steps of 7.5 dB @772kHz which is according to FCC 68 or ANSI T1. 403.

To meet the line build-out defined by ANSI T1.403 registers XPM2-0 should be programmed as follows:

00… 0 dB

01… -7.5 dB --> XPM2-0 = 20_H , 02_H , 51_H

10… -15 dB --> XPM2-0 = 20_H , 01_H , 51_H

11… -22.5 dB --> XPM2-0 = 20_H , 01_H , 50_H

SCF… Select Corner Frequency of DCO-R

Setting this bit will reduce the corner frequency of the DCO-R circuit by the factor of ten to 0.6 Hz.

Note: Reducing the corner frequency of the DCO-R circuitry will increase the synchronization time before the frequencies are synchronized.

ELT… Enable Loop-Timed

0… normal operation

1… Transmit clock is generated from the clock supplied by MCLK which is synchronized to the extracted receive route clock. In this configuration the transmit elastic buffer has to be enabled. Refer to register FMR5.XTM. For correct operation of loop timed the remote loop (bit LIM1.RL = 0) must be inactive and bit CMR1.DXSS must be cleared.

LOS1… Loss of Signal Recovery condition

0… The LOS alarm will be cleared if the predefined pulse density (register PCR) is detected during the time interval which is defined by register PCD.

1… Additionally to the recovery condition described above a LOS alarm will only be cleared if the pulse density is fulfilled and no more than 15 contigious zeros are detected during the recovery interval. (according to TR-NWT 499).

Loop Code Register 1 (Read/Write)

Vaue after RESET: 00_H

	7							0	
LCR1	EPRM	XPRBS	LDC1	LDC0	LAC1	LAC0	FLLB	LLBP	(x3B)

EPRM… Enable Pseudo Random Bit Sequence Monitor

0… Pseudo random bit sequence (PRBS) monitor is disabled.

1… PRBS is enabled. Setting this bit enables incrementing the bit error counter BEC with each detected PRBS bit error. With any change of state of the PRBS internal synchronization status an interrupt ISR3.LLBSC is generated. The current status of the PRBS synchronizer is indicated by bit FRS1.LLBAD.

XPRBS… **Transmit Pseudo Random Bit Sequence**

A one in this bit position enables transmitting of a pseudo random bit sequence to the remote end. Depending on pit LLBP the PRBS is generated according to 2^{15} -1 or 2^{20}-1 (ITU-T O. 151).

LDC1…0... **Length Deactuate (Down) Code**

These bits defines the length of the LLB deactuate code which is programmable in register LCR2.

00… length: 5 bit

01… length: 6 bit, 2 bit, 3 bit

10… length : 7 bit

11… length : 8 bit, 2 bit, 4bit

LAC1…0... **Length Actuate (Up) Code**

These bits defines the length of the LLB actuate code which is programmable in register LCR3.

00… length: 5 bit

01… length: 6 bit, 2 bit, 3 bit

10… length : 7 bit

11… length : 8 bit, 2 bit, 4bit

FLLB… **Framed Line Loopback / Invert PRBS**

Depending on bit LCR1.XPRBS this bit enables different functions:

LCR1.XPRBS=0:

0… The line loopback code is transmitted including framing bits. LLB code overwrites the FS/DL bits.

1… The line loopback code is transmitted unframed. LLB code will not overwrite the FS/DL bits.

Invert PRBS

LCR1.XPRBS=1:

0… The generated PRBS is transmitted not inverted.

1… The PRBS is transmitted inverted.

LLBP… **Line Loopback Pattern**

LCR1.XPRBS=0

0… Fixed line loopback code according to ANSI T1. 403 .

1… Enable user programmable line loopback code via register LCR2/3.

LCR1.XPRBS=1 or LCR1.EPRM = 1

0… 2^{15} -1

1… 2^{20} -1

Loop Code Register 2 (Read/Write)

Value after RESET: 00_H

	7						0	
LCR2	LDC7						LDC0	(x3C)

LDC7…LDC0… Line Loopback Deactuate Code

If enabled by bit FMR5.XLD the LLB deactuate code will automatically repeat until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LDC0 is transmittted last. For correct operations bit LCR1.XPRBS has to cleared.

Loop Code Register 3 (Read/Write)

Value after RESET: 00_H

	7						0	
LCR3	LAC7						LAC0	(x3D)

LAC7…LAC0… Line Loopback Actuate Code

If enabled by bit FMR5.XLU the LLB actuate code will automatically repeat until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LAC0 is transmittted last. For correct operations bit LCR1.XPRBS has to cleared.

System Interface Control 1 (Read/Write)

Value after RESET: 00_H

	7							0	
SIC1	SSC1	SSD1	RBS1	RBS0	SSC0	BIM	XBS1	XBS0	(x3E)

SSC1...0… Select System Clock

SIC1.SSC1/0 and SIC2.SSC2 define the clocking rate on the system highway.

SIC2.SSC2 = 0:

00…2.048 MHz

01…4.096 MHz

10…8.192 MHz

11…16.384 MHz

SIC2.SSC2 = 1:

00…1.544 MHz

01…3.088 MHz

10…6.176 MHz

11…12.352 MHz

SSD1 … **Select System Data Rate 1**

SIC1.SSD1, FMR1.SSD0 and SIC2.SSC2 define the data rate on the system highway. Programming SSD1/SSD0 and corresponding data rate is shown below.

SIC2.SSC2 = 0:

00…2.048 MBit/s

01…4.096 MBit/s

10…8.192 MBit/s

11…16.384 MBit/s

SIC2.SSC2 = 1:

00…1.544 MBit/s

01…3.088 MBit/s

10…6.176 MBit/s

11…12.352 MBit/s

RBS1...0… **Receive Buffer Size**

00… buffer size : 2 frames

01… buffer size : 1 frame

10… buffer size : 96 bits

11… By-pass of receive elastic store

BIM … **Bit Interleaved Mode**

Only applicable if bit SIC2.SSC2 is cleared. If SIC2.SSC2 is set high, the bit interleaved mode is automatically performed.

0…byte interleaved mode

1…bit interleaved mode

XBS1...0… **Transmit Buffer Size**

00… By-pass of transmit elastic store

01… buffer size : 1 frame

10… buffer size : 2 frames

11… buffer size : 96 bits

System Interface Control 2 (Read/Write)

Value after RESET: 00_H

	7							0	
SIC2	FFS	SSF	CRB	SSC2	SICS2	SICS1	SICS0		(x3F)

FFS … **Force Freeze Signaling**

Setting this bit disables updating of the receive signaling buffer and current signaling information is frozen. After resetting this bit and receiving a complete superframe updating of the signaling buffer is started again. The freeze signaling status could be also automatically generated by detecting the Loss of Signal alarm or a Loss of Frame Alignment or a receive slip (only if external register access via RSIG is enabled). This automatic freeze signaling function is logically ored with this bit.
The current internal freeze signaling status is output on pin RP(A-D) / pin function FREEZ which is selected by PC(1-4).RPC(2-0) = 110. Additionally this status is also available in register SIS.SFS.

SSF … **Serial Signaling Format**

Only applicable if pin function R/XSIG is selected.

0… Bits 1-4 in all time-slots except time-slot 0 are cleared.

1… Bits 1-4 in all time-slots except time-slot 0 are set high.

CRB … **Center Receive Elastic Buffer**

Only applicable if the time-slot assigner is disabled (PC1-4.RPC2-0 = 001) , no external or internal synchronous pulse receive is generated.
A transition from low to high will force a receive slip and the read-pointer of the receive elastic buffer is centered. The delay through the buffer is set to one half of the current buffer size. It should be hold high for at least two 1.544 MHz periods before it is cleared.

SSC2 … **Select System Clock**

Setting this bit together with SIC1.SSC1/0 enables the system interface running with a clock of 1.544 , 3.088, 6.176 or 12.352 MHz. Refer also to register SIC1.SSC1/0.

SICS2 …0 **System Interface Channel Select**

Only applicable if the system clock rate is greater than 1.544 / 2.048MHz .

Received data is transmitted on pin RDO / RSIG or received on XDI / XSIG with the selected system data rate. If the data rate is greater than 1.544 / 2.048 MBit/s the data is output or sampled in half , a quarter or a 1/8 of the 125 µsec. They will not be repeated. The time where the data is active during a 488 / 648 nsec time-slot is called in the following a channel phase. RDO / RSIG are cleared while XDI / XSIG are ignored for the remaining time of the 488 / 648 nsec or for the remaining channel phases. The channel phases are selectable with these bits.

000 …data active in channel phase 1, valid if system data rate is 16 / 8 / 4 or 12 / 6 / 3 MBit/s

001 …data active in channel phase 2, valid if data rate is 16 / 8 / 4 or 12 / 6 / 3 MBit/s

010 …data active in channel phase 3, valid if data rate is 16 / 8 or 12 / 6 MBit/s

011 …data active in channel phase 4, valid if data rate is 16 / 8 or 12 / 6 MBit/s

100 …data active in channel phase 5 , valid if data rate is 16 or 12 MBit/s

101 …data active in channel phase 6 , valid if data rate is 16 or 12 MBit/s

110 …data active in channel phase 7, valid if data rate is 16 or 12 MBit/s

111 …data active in channel phase 8 , valid if data rate is 16 or 12 MBit/s

System Interface Control 3(Read/Write)

Value after RESET: 00_H

	7							0	
SIC3	CMI				RESX	RESR	TTRF	DAF	(x40)

CMI… **Select CMI Precoding**

Only valid if CMI code (FMR0.XC1/0=01) is selected. This bit defines the CMI precoding and influences only the transmit data and not the receive data.

0… CMI with B8ZS precoding

1… CMI without B8ZS precoding

RESX… **Rising Edge Synchronous Pulse Transmit**

Depending on this bit all transmit system interface data and marker are clocked off or sampled with the selected active edge.

0… $\overline{\text{SYPX}}$ is latched with the first falling (active) edge of the SCLKX clock.

1… $\overline{\text{SYPX}}$ is latched with the first rising (active) edge of the SCLKX clock.

The $\overline{\text{SYPX}}$ pin function is selected by PC(1-4).XC(2-0) = 0000.

RESR… **Rising Edge Synchronous Pulse Receive**

Depending on this bit all receive system interface data and marker are clocked off with the selected active edge.

0… $\overline{\text{SYPR}}$ is latched with the first falling edge of the SCLKR clock.

1… $\overline{\text{SYPR}}$ is latched with the first rising edge of the SCLKR clock.

The $\overline{\text{SYPR}}$ pin function is selected by PC(1-4).RPC(2-0) = 000.

TTRF… **TTR Register Function**

Setting this bit the function of the TTR1-4 registers are changed. A one in each TTR register will force the XSIGM marker high for the respective time-slot and controls sampling of the time-slots provided by pin XSIG. XSIG is selected by PC(1-4).XPC(2-0).

DAF… **Disable Automatic Freeze**

0… Signaling is automaticly frozen if one of the following alarms occured: Loss of Signal (FRS0.LOS), Loss of Frame Alignment (FRS0.LFA) , or receive slips (ISR3.RSP/N).

1… Automatic freezing of signaling data is disabled. Updating of the signaling buffer is also done if one of the above described alarm conditions is active. However, updating of the signaling buffer is stopped if SIC2.FFS is set. Significant only if the serial signaling access is enabled.

Clock Mode Register 1 (Read/Write)

Value after RESET: 00_H

	7							0	
CMR1	DRSS1	DRSS0	RS1	RS0	DCS	STF	DXJA	DXSS	(x44)

DRSS1 ... 0 … **DCO-R Synchronization Clock Source**

These bits select the reference clock source for the DCO-R circuitry.

00… receive reference clock generated by the DPLL of channel 1

01… receive reference clock generated by the DPLL of channel 2

10… receive reference clock generated by the DPLL of channel 3

11… receive reference clock generated by the DPLL of channel 4

Note: After Reset all DCO-R circuitries will synchronize on the clock sourced by the DPLL of channel 1 . Each channel have to be configured individually.
If LIM0.MAS is set the DCO-R circuitry will synchronize on the clock applied to port SYNC.

RS1 ... 0 … **Select RCLK Source**

These bits select the source of RCLK.

00… extracted receive clock, generated by the DPLL

01… extracted receive clock with the option in case of an active LOS alarm this pin is set high.

10… dejittered 1.544 or 2.048 MHz clock generated by the internal DCO-R circuitry. The frequency depends on SIC2.SSC2.

11… dejittered 6.176 or 8.192 MHz clock generated by the internal DCO-R circuitry. The frequency depends on SIC2.SSC2.

DCS … **Disable Clock Switching**

In Slave mode (LIM0.MAS = 0) the DCO-R is synchronized on the recovered route clock. In case of loss of signal LOS the DCO-R

switches automatically to the clock sourced by port SYNC. Setting this bit automatic switching from RCLK to SYNC is disabled.

STF … **Select TCLK Frequency**

Only applicable if the pin function TCLK port XP(A-D) is selected by PC(1-4).XPC(2-0) = 011. Data on XL1/2 , XDOP/N, XOID are clocked off with TCLK.

0… 1.544 MHz

1… 6.176 MHz

DXJA… **Disable Internal Transmit Jitter Attenuation**

Setting this bit disables the transmit jitter attenuation. Reading the data out of the transmit elastic buffer and transmitting on XL1/2 (XDOP/N / XOID) is done with the clock provided on pin TCLK. In transmit elastic buffer bypass mode the transmit clock is taken from SCLKX, independent of this bit.

DXSS … **DCO-X Synchronization Clock Source**

0… The DCO-X circuitry of each channel will synchronize to the internal reference clock which is sourced by SCLKX/R or RCLK. Since there are many reference clock opportunities the following internal priorization in descenting order from left to right is realized: LIM1.RL > CMR2.DXSS > LIM2.ELT > current working clock of transmit system interface.
If one of these bits is set the corresponding reference clock is taken.

1… DCO-X synchronizes to an external reference clock provided by pin XP(A-D) pin function TCLK, if no remote loop is active. TCLK is selected by PC(1-4).XPC(2-0) = 011.

Clock Mode Register 2 (Read/Write)

Value after RESET: 00_H

	7							0	
CMR2				DCF	IRSP	IRSC	IXSP	IXSC	(x45)

DCF … **DCO-R Center- Frequency Disabled**

0… The DCO-R circuitry may be frequency centered
- in master mode if no reference clock on pin SYNC is provided or
- in slave mode if a loss of signal occurs in combination with no

clock on pin SYNC or
- a gapped clock is provided at pin RCLKI and this clock is inactive or stopped.

1… The center function of the DCO-R circuitry is disabled. The generated clock (DCO-R) is frequency frozen in that moment when no clock is available at pin SYNC or pin RCLKI. The DCO-R circuitry will starts synchronization as soon as a clock at pins SYNC or RCLKI appears.

IRSP … Internal Receive System Frame Sync Pulse

0… The frame sync pulse for the receive system interface is sourced by $\overline{\text{SYPR}}$.

1… The frame sync pulse for the receive system interface is internally sourced by the DCO-R circuitry of each channel. This internally generated frame sync could be output active low on pin RP(A-D). RPC(2-0) = 001. Programming the receive time-slot offset is also done in the same way as it is done for the external $\overline{\text{SYPR}}$. For correct operation bit IRSC must be set. $\overline{\text{SYPR}}$ is ignored.

IRSC … Internal Receive System Clock

Only applicable if bit GPC1.SMM is cleared. If GPC1.SMM is set SCLKR1 of channel 1 provides the working clock for all four channels.

0… The working clock for the receive system interface is sourced by SCLKR of each channel or in receive elastic buffer bypass mode from the corresponding extracted receive clock RCLK.

1… The working clock for the receive system interface is sourced internally by DCO-R or in bypass mode by the extracted receive clock of each channel. SCLKR is ignored.

IXSP … Internal Transmit System Frame Sync Pulse

0… The frame sync pulse for the transmit system interface is sourced by $\overline{\text{SYPX}}$.

1… The frame sync pulse for the transmit system interface is internally sourced by the DCO-R circuitry of each channel. Additionally, the external XMFS signal defines the transmit multiframe begin. XMFS is enabled or disabled via the multifunction ports. For correct operation bits CMR2.IXSC / IRSC must be set. $\overline{\text{SYPX}}$ is ignored.

IXSC … Internal Transmit System Clock

Only applicable if bit GPC1.SMM is cleared. If GPC1.SMM is set SCLKX1 of channel 1 provides the working clock for all four channels.

0… The working clock for the transmit system interface is sourced by SCLKX of each channel.

1… The working clock for the transmit system interface is sourced internally by the working clock of the receive system interface. SCLKX is ignored.

Global Configuration Register (Read/Write)

Value after RESET: 00_H

	7							0	
GCR	VIS	SCI	SES	ECMC				PD	(x46)

VIS… Masked Interrupts Visible

0… Masked interrupt status bits are not visible in registers ISR0-4.

1… Masked interrupt status bits are visible in ISR0-4, but they are not visible in registers GIS and CIS.

SCI… Status Change Interrupt

0… Interrupts will be generated either on coming or going of the internal interrupt source.

1… The following interrupts will be activated if enabled with detecting and recovering of the internal interrupt source: ISR2.LOS , ISR2.AIS and ISR0.PDEN

SES… Select External Second Timer

0… internal second timer selected

1… external second timer selected

ECMC… Error Counter Mode COFA

0… not defined; reserved for future applications.

1… A Change of Frame or Multiframe Alignment COFA is detected since the last re-synchronization. The events are accumulated in the COFA event counter COEC.1-0.
Multiframe periods received in the asynchronous state are accumulated in the COFA event counter COEC.7-2.
An overflow of each counter is disabled.

PD… **Power Down**

Switches the appropriate single FALC(1-4) between power up and power down mode.

0… Power Up

1… Power Down
All outputs are driven inactive, except the multifunction ports, which are driven high.

Errored Second Mask (Read/Write)

Value after RESET: FF_H

	7							0	
ESM	LFA	FER	CER	AIS	LOS	CVE	SLIP		(x47)

ESM **Errored Second Mask**

This register functions as an additional mask register for the interrupt status bit Errored Second (ISR3.ES). A ‘1’ in a bit position of ESM sets the mask active for the interrupt status.

Disable Error Counter (Write)

Value after RESET: 00_H

	7							0	
DEC	DRBD		DCOEC	DBEC	DCEC	DEBC	DCVC	DFEC	(x60)

DRBD **Disable Receive Buffer Delay**

This bit has to be set before reading the register RBD. It will be automatically reset if RBD has been read.

DCOEC… **Disable COFA Event Counter**

DBEC… **Disable PRBS Bit Error Counter**

Only valid if LCR1.EPRM=1 and FMR1.ECM are reset.

DCEC… **Disable CRC Error Counter**

DEBC… **Disable Errored Block Counter**

DCVC… **Disable Code Violation Counter**

DFEC… **Disable Framing Error Counter**

These bits are only valid if FMR1.ECM is cleared. They have to be set before reading the error counters. They will be automatically reset if the corresponding error counter high byte has been read. With the rising edge of these bits the error counters are latched and then cleared.

Transmit Signaling Register (Write)

Value after RESET: not defined

	7							0	
XS1	A1	B1	C1/A2	D1/B2	A2/A3	B2/B3	C2/A4	D2/B4	(x70)
XS2	A3/A5	B3/B5	C3/A6	D3/B6	A4/A7	B4/B7	C4/A8	D4/B8	(x71)
XS3	A5/A9	B5/B9	C5/A10	D5/B10	A6/A11	B6/B11	C6/A12	D6/B12	(x72)
XS4	A7/A13	B7/B13	C7/A14	D7/B14	A8/A15	B8/B15	C8/A16	D8/B16	(x73)
XS5	A9/A17	B9/B17	C9/A18	D9/B18	A10/A19	B10/B19	C10/A20	D10/B20	(x74)
XS6	A11/A21	B11/B21	C11/A22	D11/B22	A12/A23	B12/B23	C12/A24	D12/B24	(x75)
XS7	A13/A1	B13/B1	C13/A2	D13/B2	A14/A3	B14/B3	C14/A4	D14/B4	(x76)
XS8	A15/A5	B15/B5	C15/A6	D15/B6	A16/A7	B16/B7	C16/A8	D16/B8	(x77)
XS9	A17/A9	B17/B9	C17/A10	D17/B10	A18/A11	B18/B11	C18/A12	D18/B12	(x78)
XS10	A19/A13	B19/B13	C19/A14	D19/B14	A20/A15	B20/B15	C20/A16	D20/B16	(x79)
XS11	A21/A17	B21/B17	C21/A18	D21/B18	A22/A19	B22/B19	C22/A20	D22/B20	(x7A)
XS12	A23/A21	B23/B21	C23/A22	D23/B22	A24/A23	B24/B23	C24/A24	D24/B24	(x7B)

Transmit Signaling Register 1-12

The transmit signaling register access is enabled by setting bit FMR5.EIBR = 1. Each register contains the bit robbing information for 8 DS0 channels. With the transmit CAS empty interrupt ISR1.CASE the contents of these registers will be copied into a shadow register. The contents will subsequently sent out in the corresponding bit positions of the next outgoing multiframe. XS1.7 will be sent out first in channel 1 frame 1 and XS12.0 will be sent out last. The transmit CAS empty interrupt ISR1.CASE requests that these registers should be serviced within the next 3 ms. If requests for new information are ignored, current contents will be repeated.
If access to XS1-12 registers is done without control of the interrupt ISR1.CASE and the write access to these registers is done exact in that moment when this interrupt is generated, data may be lost.

Note: A software reset (CMDR.XRES) will reset these registers.

Port Configuration 1-4 (Read/Write)

Value after RESET: 00_H

	7							0	
PC1		RPC2	RPC1	RPC0		XPC2	XPC1	XPC0	(x80)
PC2		RPC2	RPC1	RPC0		XPC2	XPC1	XPC0	(x81)
PC3		RPC2	RPC1	RPC0		XPC2	XPC1	XPC0	(x82)
PC4		RPC2	RPC1	RPC0		XPC2	XPC1	XPC0	(x83)

RPC2 ...0… Receive multifunction port configuration

The multifunction ports RP(A-D) are bidirectional. After Reset these ports are configured as inputs. With the selection of the pin function the In/Output configuration is also achieved. The input function $\overline{\text{SYPR}}$ may only be selected once, it should not be selected twice or more. Register PC1 configures port RPA,while PC2 --> port RPB,
PC3 --> port RPC and PC4 --> port RPD.

000…$\overline{\text{SYPR}}$: Synchronous Pulse Receive (Input)
Together with register RC1/0 $\overline{\text{SYPR}}$ defines the frame begin on the receive system interface. Because of the offset programming the $\overline{\text{SYPR}}$ and the RFM pin function could not be selected in parallel.

001…RFM : Receive Frame Sync (Output)
CMR2.IRSP = 0: This receive frame marker could be active high for a 1.544 MHz or 2.048 MHz period during any bit position of the current frame. Programming is done with registers RC1/0. The internal time-slot assigner is disabled.
CMR2.IRSP = 1: Internal generated frame synchronization pulse generated by the DCO-R circuitry. Together with registers RC1/0 the frame begin on the receive system interface is defined. This frame synchronization pulse is active low 1.544 MHz or 2.048 MHz period.

010…RMFB : Receive Multiframe Begin (Output)
Marks the beginning of every received multiframe or optionally every 12 frames (active high).

011…RSIGM : Receive Signaling Marker (Output)
Marks the time-slots which are defined by register RTR1-4 of every frame at port RDO. Optionally in CAS-BR applications the robbed bits are marked every six frames.

100…RSIG : Receive Signaling Data (Output)
The received CAS multiframe is transmitted on this pin. Time-slots on RSIG correlates directly to the time-slot assignment on RDO. In system interface multiplex mode all four received signaling data streams are merged into a single rail data stream byte or bit interleaved on RSIG1.

101…DLR : Data Link Bit Receive (Output)
Marks the DL-bit position within the data stream on RDO.

110…FREEZ : Freeze Signaling (Output)
The freeze signaling status is active high by detecting a Loss of Signal alarm, or a Loss of Frame Alignment or a receive slip (pos. or neg.). It will hold high for at least one complete multiframe after the alarm disappears. Setting SIC2.FFS enforces a high on pin FREEZ.

111…$\overline{\text{RFSP}}$: Receive Frame Synchronous Pulse (Output)
Marks the frame begin in the receivers synchrounous state. This marker is active low for 648 ns with a frequency of 8 kHz.

XPC2 ...0… Transmit multifunction port configuration

The multifunction ports XP(A-D) are bidirectional. After Reset these ports are configured as inputs. With the selection of the pin function the In/Output configuration is also achieved. Each of the four different input functions ($\overline{\text{SYPX}}$, XMFS, XSIG, TCLK) may only be selected once. No input function should be selected twice or more. $\overline{\text{SYPX}}$ and XMFS should not be selected in parallel. Register PC1 configures port XPA,while PC2 --> port XPB, PC3 --> port XPC and PC4 --> port XPD.

000…$\overline{\text{SYPX}}$: Synchronous Pulse Transmit (Input)
Together with register XC1/0 $\overline{\text{SYPX}}$ defines the frame begin on the transmit system interface ports XDI and XSIG.

001…XMFS : Transmit Multiframe Synchronization (Input)
Together with register XC1/0 XMFS defines the frame and multiframe begin on the transmit system interface ports XDI and XSIG. Depending on PC5.CXMFS the signal on XMFS is active high or low.

010…XSIG : Transmit Signaling Data (Input)
Input for transmit signaling data received from the signaling highway. In system interface multiplex mode latching of the data stream containing the 4 signaling multiframes is done byte or bit interleaved on port XDI1. Optionally sampling of XSIG data is controlled by the active high XSIGM marker.

011…TCLK : Transmit Clock (Input)
A 1.544 / 6.176 MHz clock has to be sourced by the system if the internal generated transmit clock (DCO-X) should not be used. Optionally this input functions as a synchronization clock for the DCO-X circuitry with a frequencyof 1.544 MHz.

100…XMFB : Transmit Multiframe Begin (Output)
Marks the beginning of every transmit multiframe or optionally every 12 frames.

101…XSIGM : Transmit Signaling Marker (Output)
Marks the time-slots which are defined by register TTR1-4 of every frame at port XDI. Optionally in CAS-BR applications the robbed bits are marked every six frames.

110…DLX : Data Link Bit Transmit (Output)
Marks the DL-bit position within the data stream on XDI.

111…XCLK : Transmit Line Clock (Output)
Frequency: 1.544 MHz

Port Configuration 5 (Read/Write)

Value after RESET: 00_H

	7							0	
PC5					CXMFS	CSXP	CSRP	CRP	(x84)

CXMFS … Configure XMFS Port

0… Port XMFS is active low.

1… Port XMFS is active high.

CSXP … Configure SCLKX Port

0… SCLKX : Input

1… SCLKX : Output

CSRP … Configure SCLKR Port

0… SCLKR : Input

1… SCLKR : Output

CRP … Configure RCLK Port

0… RCLK : Input

1… RCLK : Output

Global Port Configuration 1 (Read/Write)

Value after RESET: 00_H

	7							0	
GPC1	SMM	CSFP1	CSFP0		FSS1	FSS0	R1S1	R1S0	(85)

SMM … **System Interface Multiplex Mode**

Setting this bit enables a single rail data stream of 16.384 / 8.192 / 12.352 or 6.176 MBit/s containg all four T1 frames. The receive system interface for all four channels is running with the clock provided on SCLKR1 and the frame sync pulse provided on $\overline{\text{SYPR1}}$. The transmit system interface is running with SCLKX1 and $\overline{\text{SYPX1}}$. Data will be transmitted / accepted in a byte or bit interleaved format. Bit interleaving is valid with the 16.384 / 8.192 / 12.352 or 6.176 MHz clocking rates. However byte interleaving is only applicable with the 16.384 or 8.192 MHz clock. In the system interface multiplex mode the following pin configuration has to be fulfilled and must be identically for all for 4 channels:

- $\overline{\text{SYPR1}}$ has to be provided on pin RPA1
- $\overline{\text{SYPX1}}$ has to be provided on pin XPA1 or
- XMFS has to be provided on pin XPB1
- XSIG has to be provided on pin XPC1
- RSIG will be output on pin RPB1

Each of the four channels have to be configured equally:

- clocking rate : 16.384 / 8.192 / 12.352 MHz or 6.176 MHz SIC1.SSC1/0 and SIC2.SSC2
- data rate : 16.384 / 8.192 / 12.352MBit/s or 6.176 MBit/s, SIC1.SSD1, FMR1.SSD0
- time-slot offset programming : RC1/0 , XC1/0
- receive buffer size : SIC1.RBS1/0 = 00 (2 frames)

e.g. : system clock rate = 8.192 MHz : SIC1.SSC1/0 = 10 and system data rate = 8.192 MBit/s : SIC1.SSD1 = 1 , FMR1.SSD0 = 0
The multiplexed data stream is internal logically ored. Therefore the selection of the active channel phase have to be configured different for each single channel FALC(1-4). Programming is done with SIC2.SICS2-0.
for FALC1: SIC2.SICS2-0 = 000, selects the first channel phase
for FALC2: SIC2.SICS2-0 = 001, selects the second channel phase

for FALC3: SIC2.SICS2-0 = 010, selects the third channel phase
for FALC4: SIC2.SICS2-0 = 011, selects the fourth channel phase

byte interleaved data format: SIC1.BIM = 0

XDI/RDO: F1-TS0, F2-TS0, F3-TS0, F4-TS0, F1-TS1, ... F4-TS31

X/RSIG: F1-STS0, F2-STS0, F3-STS0, F4-STS0, F1-... F4-STS31

or : bit interleaved data format: SIC1.BIM = 1

XDI/RDO: F1-TS0-B1, F2-TS0-B1, F3-TS0-B1, F4-TS0-B1, F1-TS0-B2, ... F4-TS31-B8

X/RSIG: F1-STS0-B1, F2-STS0-B1, F3-STS0-B1, F4-STS0-B1, F1-STS0-B2, ... F4-STS31-B8

with : F = Framer, TS = Time-Slot, STS = Signaling Time-Slot, B = Bit

In system interface multiplex mode signals on RDO2-4 and RSIG2-4 are undefined, while signals on SCLKR2-4, $\overline{\text{SYPR}}$2-4, SCLKX2-4, $\overline{\text{SYPX}}$2-4, XDI2-4 and XSIG2-4 are ignored.

CSFP1 ... 0 … **Configure SEC / FSC Port**

The FSC pulse is generated if the DCO-R circuitry of the selected channel is active (CMR2.IRSC = 1 or CMR1.RS1/0 = 10 or 11).

00 … SEC : Input , active high

01 … SEC : Output, active high

10 … FSC: Output , active high

11 … FSC: Output, active low

FSS1 ... 0 … **SEC / FSC Source**

One of the four internal generated dejittered 8 kHz clocks or second timers (SEC) are output on port SEC / FSC.

GPC1.CSFP1 = 1:

00 … FSC : 8 kHz sourced by channel 1

01 … FSC : 8 kHz sourced by channel 2

10 … FSC : 8 kHz sourced by channel 3

11 … FSC : 8 kHz sourced by channel 4

GPC1.CSFP1 = 0:

00 … SEC : second timer sourced by channel 1

01 … SEC: second timer sourced by channel 2

10 … SEC: second timer sourced by channel 3

11 … SEC: second timer sourced by channel 4

R1S1 ... 0 … **RCLK1 Source**

One of the four internal generated receive route clocks are output on port RCLK1. Outputs RCLK2-4 are valid independent of these bits.

Refer to bit CMR1.RS1/0.

00 … extracted receive clock of channel 1

01 … extracted receive clock of channel 2

10… extracted receive clock of channel 3

11… extracted receive clock of channel

8.5 Status Register Description

Table 31
Status Register Address Arrangement

Address				Register	Type	Comment
00	100	200	300	RFIFO	R	Receive FIFO
49	149	249	349	RBD	R	Receive Buffer Delay
4A				VSTR	R	Version Status
4B	14B	24B	34B	RES	R	Receive Equalizer Status
4C	14C	24C	34C	FRS0	R	Framer Receive Status 0
4D	14D	24D	34D	FRS1	R	Framer Receive Status 1
4E	14E	24E	34E	FRS2	R	Framer Receive Status 2
4F	14F	24F	34F			
50	150	250	350	FECL	R	Framing Error Counter Low
51	151	251	351	FECH	R	Framing Error Counter High
52	152	252	352	CVCL	R	Code Violation Counter Low
53	153	253	353	CVCH	R	Code Violation Counter High
54	154	254	354	CECL	R	CRC Error Counter Low
55	155	255	355	CECH	R	CRC Error Counter High
56	156	256	356	EBCL	R	Errored Block Counter Low
57	157	257	357	EBCH	R	Errored Block Counter High
58	158	258	358	BECL	R	Bit Error Counter Low
59	159	259	359	BECH	R	Bit Error Counter High
5A	15A	25A	35A	COEC	R	COFA Event Counter
5B	15B	25B	35B			
5C	15C	25C	35C	RDL1	R	Receive DL-Bit Register 1
5D	15D	25D	35D	RDL2	R	Receive DL-Bit Register 2
5E	15E	25E	35E	RDL3	R	Receive DL-Bit Register 3
5F	15F	25F	35F			
60	160	260	360			
61	161	261	361			
62	162	262	362	RSP1	R	Receive Signaling Pointer 1
63	163	263	363	RSP2	R	Receive Signaling Pointer 2

8.5 Status Register Description

Table 31
Status Register Address Arrangement

Address				Register	Type	Comment
64	164	264	364	SIS	R	Signaling Status Register
65	165	265	365	RSIS	R	Receive Signaling Status Register
66	166	266	366	RBCL	R	Receive Byte Control Low
67	167	267	367	RBCH	R	Receive Byte Control High
68	168	268	368	ISR0	R	Interrupt Status Register 0
69	169	269	369	ISR1	R	Interrupt Status Register 1
6A	16A	26A	36A	ISR2	R	Interrupt Status Register 2
6B	16B	26B	36B	ISR3	R	Interrupt Status Register 3
6C	16C	26C	36C	ISR4	R	Interrupt Status Register 4
6D	16D	26D	36D			
6E	16E	26E	36E	GIS	R	Global Interrupt Status
6F				CIS	R	Channel Interrupt Status
70	170	270	370	RS1	R	Receive Signaling Register 1
71	171	271	371	RS2	R	Receive Signaling Register 2
72	172	272	372	RS3	R	Receive Signaling Register 3
73	173	273	373	RS4	R	Receive Signaling Register 4
74	174	274	374	RS5	R	Receive Signaling Register 5
75	175	275	375	RS6	R	Receive Signaling Register 6
76	176	276	376	RS7	R	Receive Signaling Register 7
77	177	277	377	RS8	R	Receive Signaling Register 8
78	178	278	378	RS9	R	Receive Signaling Register 9
79	179	279	379	RS10	R	Receive Signaling Register 10
7A	17A	27A	37A	RS11	R	Receive Signaling Register 11
7B	17B	27B	37B	RS12	R	Receive Signaling Register 12

Receive FIFO (Read) RFIFO

	7							0	
RFIFO	RF7							RF0	(x00/x01)

Reading data from RFIFO can be done in an 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. The LSB is received first from the serial interface.

The size of the accessible part of RFIFO is determined by programming the bits CCR1.RFT1…0 (RFIFO threshold level). It can be reduced from 32 bytes (RESET value) down to 2 bytes (four values: 32, 16, 4, 2 bytes).

Data Transfer

Up to 32 bytes/16 words of received data can be read from the RFIFO following a RPF or a RME interrupt.

RPF Interrupt: A fixed number of bytes/words to be read (32, 16, 4, 2 bytes). The message is not yet complete.

RME Interrupt: The message is completely received. The number of valid bytes is determined by reading the RBCL, RBCH registers.

RFIFO is released by issuing the “Receive Message Complete” command (RMC).

Receive Buffer Delay (Read)

	7							0	
RBD			RBD5	RBD4	RBD3	RBD2	RBD1	RBD0	(x49)

RBD5…RBD0... Receive Elastic Buffer Delay

These bits informs the user about the current delay (in time-slots) through the receive elastic buffer. The delay is updated every 386 or 193 bits (SIC1.RBS1/0). Before reding this register the user has to set bit DEC.DRBD in order to halt the current value of this register. After reading RBD updating of this register is enabled. Not valid if the receive buffer is bypassed.

000000 = delay < 1 time-slot

:

:

111111 = delay >63 time-slots

Version Status Register (Read)

	7							0	
VSTR	VN7							VN0	(4A)

VN7 – VN0… **Version Number of Chip**

00_H…Version 1.1

Receive Equalizer Status (Read)

	7							0	
RES	EV1	EV0		RES4	RES3	RES2	RES1	RES0	(x4B)

EV1…EV0... **Equalizer Status Valid**

These bits informs the user about the current state of the receive equalization network . Only vaild if LIM1.EQON is set.

00… equalizer status not vaild, still adapting

01… equalizer status vaild

10… equalizer status not vaild

11… equalizer status valid but high noise floor

RES4…RES0... **Receive Equalizer Status**

The current line attenuation status in steps of nearly 1.4 dB are displayed in these bits. Only valid if bits EV1/0 = 01.
Accuracy: +/- 2 digit, based on temperature influence and noise amplitude variations.

00000… attenuation: 0 dB

...

11001… max. attenuation: -36 dB

Framer Receive Status Register 0 (Read)

	7							0	
FRS0	LOS	AIS	LFA	RRA			LMFA	FSRF	(x4C)

LOS… **Loss of Signal (Red Alarm)**

Detection:
This bit is set when the incoming signal has „no transitions“ (analog interface) or logical zeros (dig. interface) in a time interval of T consecutive pulses, where T is programmable via PCD register:
Total account of consecutive pulses: 16 < T < 4096.

Analog interface: The receive signal level where “no transition” will be declared is defined by the programmed value of LIM1.RIL2-0.

Recovery:
Analog interface: The bit will be reset in short haul mode when the incoming signal has transitions with signal levels greater than the programmed receive input level (LIM1.RIL2-0) for at least M pulse periods defined by register PCR in the PCD time interval. In long haul mode addtionally bit RES.6 must be set for at least 250µsec.
Digital interface: The bit will be reset when the incoming data stream contains at least M ones defined by register PCR in the PCD time interval.

With the rising edge of this bit an interrupt status bit (ISR2.LOS) will be set. For additionally recovery conditions refer also to register LIM2.LOS1.
The bit will be set during alarm simulation and reset if FRS2.ESC = 0, 3, 4, 6,7 and no alarm condition exists.

AIS… **Alarm Indication Signal (Blue Alarm)**

This bit is set when the conditions defined by bit FMR4.AIS3 are detected. The flag stays active for at least one multiframe.

With the rising edge of this bit an interrupt status bit (ISR2.AIS) will be set. It will be reset with the beginning of the next following multiframe if no alarm condition is detected.

The bit will be set during alarm simulation and reset if FRS2.ESC = 0, 3, 4, 7 and no alarm condition exists.

LFA… **Loss of Frame Alignment**

The flag is set if pulseframe synchronization has been lost. The conditions are specified via bit FMR4.SSC1/0. Setting this bit will cause an interrupt status (ISR2.LFA).

The flag is cleared when synchronization has been regained. Additionally interrupt status ISR2.FAR is set with clearing this bit.

RRA… Receive Remote Alarm (Yellow Alarm)

The flag is set after detecting remote alarm (yellow alarm). Conditions for setting/resetting are defined by bit RC0.RRAM.

With the rising edge of this bit an interrupt status bit ISR2.RA will be set.

With the falling edge of this bit an interrupt status bit ISR2.RAR will be set.

The bit will be set during alarm simulation and reset if FRS2.ESC = 0, 3, 4,5,7 and no alarm condition exists.

LMFA… Loss Of Multiframe Alignment

Set in F12 or F72 format when 2 out of 4- (or 5 or 6) multiframe alignment patterns are incorrect.

Additionally the interrupt status bit ISR2.LMFA is set.

Cleared after multiframe synchronization has been regained. With the falling edge of this bit an interrupt status bit ISR2.MFAR is generated.

FSRF… Frame Search Restart Flag

Toggles when no framing candidate (pulseframing or multiframing) is found and a new frame search is started.

Framer Receive Status Register 1 (Read)

	7							0	
FRS1	EXZD	PDEN		LLBDD	LLBAD		XLS	XLO	(x4D)

EXZD… Excessive Zeros Detected

Significant only if excessive zeros detection is enabled (FMR2.EXZE=1).

Set after detecting of more than 7 (B8ZS code) or more than 15 (AMI code) contiguous zeros in the received bit stream. This bit is cleared when read.

PDEN… Pulse Density Violation Detected

The pulse density of the received data stream is below the requirement defined by ANSI T1. 403 or more than 14 consecutive zeros are detected. With the violation of the pulse density this bit will be set and will remain active until it is read. Reading the register will clear this bit. (Clear on Read).
Additionally an interrupt status ISR0.PDEN is generated with the rising edge of PDEN.

LLBDD… Line Loop Back Deactuation Signal Detected

This bit is set to one in case the LLB deactuate signal is detected and then received over a period of more than 33,16 msec with a bit error rate less than 1/100. The bit remains set as long as the bit error rate does not exceed 1/100.

If framing is aligned, the first bit position of any frame is not taken into account for the error rate calculation.

Any change of this bit will cause a LLBSC interrupt.

LLBAD… Line Loopback Actuation Signal Detected / PRBS Status

Depending on bit LCR1.EPRM the source of this status bit changed.

LCR1.EPRM=0: This bit is set to one in case the LLB actuate signal is detected and then received over a period of more than 33,16 msec with a bit error rate less than 1/100. The bit remains set as long as the bit error rate does not exceed 1/100.

If framing is aligned, the first bit position of any frame is not taken into account for the error rate calculation.

Any change of this bit will cause a LLBSC interrupt.

PRBS Status

LCR1.EPRM=1: The current status of the PRBS synchronizer is indicated in this bit. It is set high if the synchronous state is reached even in the presence of a BER 1/10. A data stream containing all zeros with / without framing bits is also a valid pseudo random bit sequence.

XLS… **Transmit Line Short**

Significant only if the ternary line interface is selected by LIM1.DRS=0.

0… Normal operation. No short is detected.

1… The XL1 and XL2 are shortend for at least 3 pulses. As a reaction of the short the pins XL1 and XL2 are automatically forced into a high impedance state if bit XPM2.DAXLT is reset. After 128 consecutive pulse periods the outputs XL1/2 are activated again and the internal transmit current limiter is checked. If a short between XL1/2 is still further active the outputs XL1/2 are in high impedance state again. When the short disappears pins XL1/2 are activated automatically and this bit will be reset. With any change of this bit an interrupt ISR1.XLSC will be generated. In case of XPM2.XLT is set this bit will be frozen.

XLO… **Transmit Line Open**

0… Normal operation

1… This bit will be set if at least 32 consecutive zeros were sent via pins XL1/XL2 respective XDOP/XDON. This bit is reset with the first transmitted pulse. With the rising edge of this bit an interrupt ISR1.XLSC will be set. In case of XPM2.XLT is set this bit will be frozen.

Framer Receive Status Register 2 (Read)

	7						0	
FRS2	ESC2	ESC0						(x4E)

ESC2…ESC0… Error Simulation Counter

This three-bit counter is incremented by setting bit FMR0.SIM. The state of the counter determines the function to be tested:

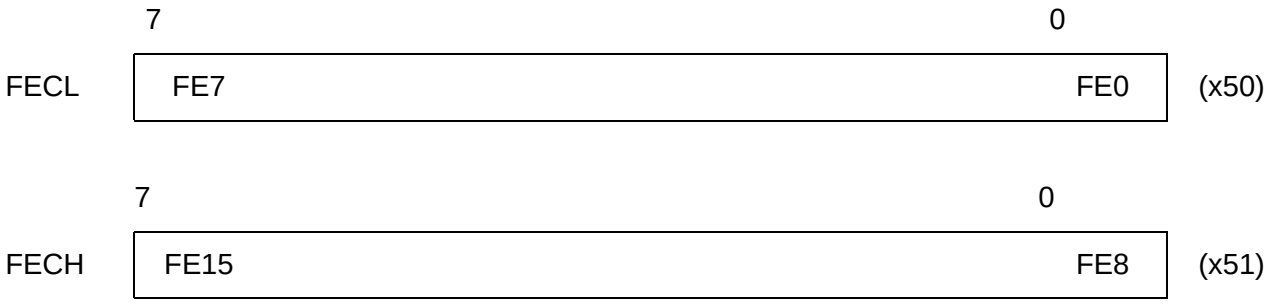
For complete checking of the alarm indications, eight simulation steps are necessary (FRS2.ESC = 0 after a complete simulation).

Tested Alarms ESC2…ESC0 =	0	1	2	3	4	5	6	7
LFA			x				x	
LMFA			x				x	
RRA (bit2 =0)		x						
RRA (S-bit fr. 12)			x					
RRA (DL-pattern)							x	
LOS		x	x			x		
EBC (F12,F72)			x				x	
EBC (only ESF)		x	x			x	x	
AIS		x	x			x	x	
FEC			x				x	
CVC		x	x			x		
CEC (only ESF)		x	x			x	x	
RSP		x						
RSN						x		
XSP		x						
XSN						x		
BEC		x	x			x		
COEC			x				x	

Some of these alarm indications are simulated only if the QuadFALC is configured in the appropriate mode. At simulation steps 0, 3, 4, and 7 pending status flags are reset automatically and clearing of the error counters and interrupt status registers ISR0-3 should be done. Incrementing the simulation counter should not be done at time intervals

shorter than 1.5 ms (F4, F12, F72) or 3 ms (ESF). Otherwise, reactions of initiated simulations may occur at later steps.

Framing Error Counter (READ)



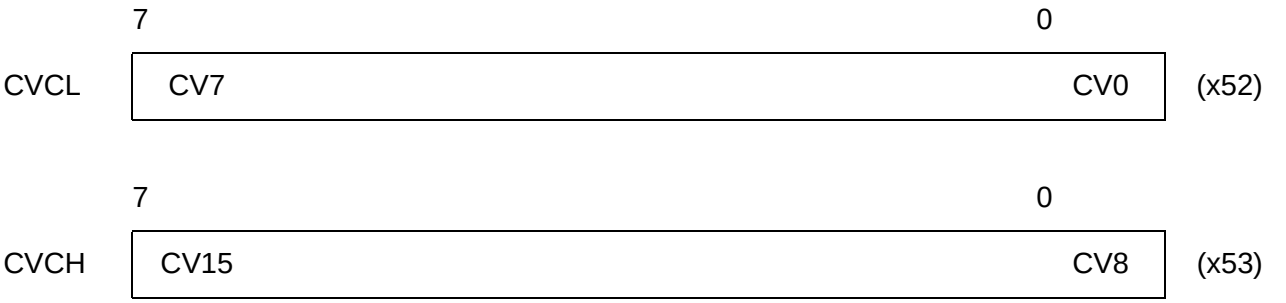
FE15…FE0… Framing Errors

This 16-bit counter will be incremented when incorrect FT and FS bits in F4, F12 and F72 format or incorrect FAS bits in ESF format are received.
Framing errors will not be counted during asynchronous state. The error counter will not roll over.
During alarm simulation, the counter will be incremented twice.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DFEC has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DFEC will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

Code Violation Counter (READ)



CV15…CV0… **Code Violations**

No function if NRZ Code has been enabled.

If the B8ZS code (bit FMR0.RC1/0 = 11) is selected, the 16-bit counter will be incremented by detecting violations which are not due to zero substitution. If FMR2.EXZE is set, additionally excessive zero strings (more than 7 contiguous zeros) are detected and counted.

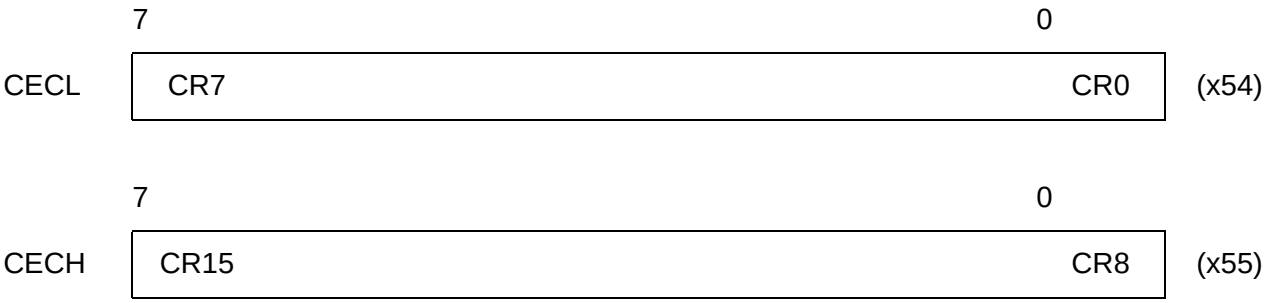
If simple AMI coding is enabled (FMR0.RC0/1 = 10) all bipolar violations are counted. If FMR2.EXZE is set, additionally excessive zero strings (more than 15 contiguous zeros) are detected and counted. The error counter will not roll over.

During alarm simulation, the counter is incremented continuously with every second received bit.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCVC has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DCVC will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

CRC Error Counter (READ)



CR15…CR0… CRC Errors

No function if CRC6 procedure or ESF format are disabled.

In ESF mode, the 16-bit counter will be incremented when a multiframe has been received with a CRC error. CRC errors will not be counted during asynchronous state. The error counter will not roll over.
During alarm simulation, the counter is incremented once per multiframe.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DCEC will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

Errored Block Counter (READ)

	7							0	
EBCL	EBC7							EBC0	(x56)

	7							0	
EBCH	EBC15							EBC8	(x57)

EBC15…EBC0… Errored Block Counter

In ESF format this 16-bit counter will be incremented once per multiframe if a multiframe has been received with a CRC error or an errored frame alignment has been detected. CRC and framing errors will not be counted during asynchronous state. The error counter will not roll over.

In F4/12/72 format an errored block contain 4/12 or 72 frames. Incrementing is done once per multiframe if framing errors has been detected.
During alarm simulation, the counter is incremented in ESF format once per multiframe and in F4/12/72 format only one time.

Clearing and updating the counter is done according to bit FMR1.ECM.

If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DEBC has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DEBC will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

Bit Error Counter (READ)

	7		0	
BECL	BEC7		BEC0	(x58)

	7		0	
BECH	BEC15		BEC8	(x59)

BEC15…BEC0… Bit Error Counter

If the PRBS monitor is enabled by LCR1.EPRM= 1 this 16-bit counter will be incremented with every received PRBS bit error in the PRBS synchronous state FRS1.LLBAD=1. The error counter will not roll over.

During alarm simulation, the counter will be incremented continuously with every second received bit.

Clearing and updating the counter is done according to bit FMR1.ECM.

If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the PRBS bit error counter bit DEC.DBEC has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DBEC will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

COFA Event Counter (READ)

	7			0	
COEC	COE7	COE2	COE1	COE0	(x5A)

COE7…COE2… Multiframe Counter

If GCR.ECMC = 1 this 6 bit counter increments with each multiframe period in the asynchronous state FRS0.LFA/LMFA =1. The error counter will not roll over.

COE1…COE0… Change of Frame Alignment Counter

If GCR.ECMC = 1 this 2 bit counter increments with each detected change of frame / multiframe alignment. The error counter will not roll over.
During alarm simulation, the counter is incremented once per multiframe.

Clearing and updating the counter is done according to bit FMR1.ECM.

If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the event counter bit DEC.DCOEC has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DCOEC will automatically be reset with reading the error counter high byte on address $5B_H$. Data read on $5B_H$ is not defined.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

Receive DL-Bit Register 1 (Read)

	7							0	
RDL1	RDL17	RDL16	RDL15	RDL14	RDL13	RDL12	RDL11	RDL10	(x5C)

RDL17…RDL10…Receive DL-Bit

Only valid if F12, F24 or F72 format is enabled.
The received FS/DL-Bits are shifted into this register. RDL10 is received in frame 1 and RDL17 in frame 15, if F24 format is enabled. RDL10 is received in frame 26 and RDL17 in frame 40, if F72 format is enabled.
In F12 format the FS-Bits of a complete multiframe is stored in this register. RDL10 is received in frame 2 and RDL15 in frame 12.
This register will be updated with every receive multiframe begin interrupt ISR0.RMB.

Receive DL-Bit Register 2 (Read)

	7							0	
RDL2	RDL27	RDL26	RDL25	RDL24	RDL23	RDL22	RDL21	RDL20	(x5D)

RDL27…RDL20…Receive DL-Bit

Only valid if F24 or F72 format is enabled.
The received DL-Bits are shifted into this register. RDL20 is received in frame 17 and RDL23 in frame 23, if F24 format is enabled. RDL20 is received in frame 42 and RDL27 in frame 56, if F72 format is enabled.
This register will be updated with every receive multiframe begin interrupt ISR0.RMB.

Receive DL-Bit Register 3 (Read)

	7							0	
RDL3	RDL37							RDL30	(x5E)

RDL37…RDL30…Receive DL-Bit

Only valid if F72 format is enabled.
The received DL-Bits are shifted into this register. RDL30 is received in frame 58 and RDL37 in frame 72, if F72 format is enabled.
This register will be updated with every receive multiframe begin interrupt ISR0.RMB.

Receive Signaling Pointer 1 (Read)

Value after RESET: 00_H

	7							0	
RSP1	RS8C	RS7C	RS6C	RS5C	RS4C	RS3C	RS2C	RS1C	(x62)

RS8C…RS1C Receive Signaling Register RS1-8 Changed

A one in each bit position indicates that the received signaling data in the corresponding RS1-8 registers are updated. Bit RS1C is the pointer for register RS1,... while RS8C points to RS8.

Receive Signaling Pointer 2 (Read)

Value after RESET: 00_H

	7							0	
RSP2					RS12C	RS11C	RS10C	RS9C	(x63)

RS12C…RS9C Receive Signaling Register RS9-12 Changed

A one in each bit position indicates that the received signaling data in the corresponding RS9-12 registers are updated. Bit RS9C is the pointer for register RS9,... while RS12C points to RS12

Signaling Status Register (Read)

	7							0	
SIS	XDOV	XFW	XREP	IVB	RLI	CEC	SFS	BOM	(x64)

XDOV… **Transmit Data Overflow**

More than 32 bytes have been written to the XFIFO.
This bit is reset by:

– a transmitter reset command XRES or

– when all bytes in the accessible half of the XFIFO have been moved in the inaccessible half.

XFW… **Transmit FIFO Write Enable**

Data can be written to the XFIFO.

XREP… **Transmission Repeat**

Status indication of CMDR.XREP.

IVB… **Invalid BOM Frame Received**

0… valid BOM frame (11111111, 0xxxxxx0) received.

1… invalid BOM frame received.

RLI… **Receive Line Inactive**

Neither FLAGs as Interframe Time Fill nor frames are received via the signaling timeslot.

CEC… **Command Executing**

0… No command is currently executed, the CMDR register can be written to.

1… A command (written previously to CMDR) is currently executed, no further command can be temporarily written in CMDR register.

Note: CEC will be active at most 2.5 periods of the current system data rate.

SFS… **Status Freeze Signaling**

0… freeze signaling status inactive.

1… freeze signaling status active.

BOM… **Bit Oriented Message**

Significant only in ESF frame format and auto switching mode is enabled.

0… HDLC mode

1… BOM mode

Receive Signaling Status Register (Read)

	7							0	
RSIS	VFR	RDO	CRC16	RAB	HA1	HA0	HFR	LA	(x65)

RSIS relates to the last received HDLC or BOM frame; it is copied into RFIFO when end-of-frame is recognized (last byte of each stored frame).

VFR… **Valid Frame**

Determines whether a valid frame has been received.

1… valid

0… invalid

An invalid frame is either

– a frame which is not an integer number of 8 bits (n × 8 bits) in length (e.g. 25 bits), or

– a frame which is too short taking into account the operation mode selected via MODE (MDS2-0) and the selection of receive CRC ON/OFF (CCR2.RCRC) as follows:

- MDS2-0 = 011 (16 bit Address),
  RCRC = 0 : 4 bytes; RCRC = 1 : 3-4 bytes
- MDS2-0 = 010 (8 bit Address),
  RCRC = 0 : 3 bytes; RCRC = 1 : 2-3 bytes

Note: Shorter frames are not reported.

RDO… **Receive Data Overflow**

A data overflow has occurred during reception of the frame.

Additionally, an interrupt can be generated
(refer to ISR1.RDO/IMR1.RDO).

CRC16… **CRC16 Compare/Check**

0… CRC check failed; received frame contains errors.

1… CRC check o.k.; received frame is error-free.

RAB… **Receive Message Aborted**

The received frame was aborted from the transmitting station. According to the HDLC protocol, this frame must be discarded by the receiver station.

HA1, HA0… **High Byte Address Compare**

Significant only if 2-byte address mode has been selected.

In operating modes which provide high byte address recognition, the QuadFALC compares the high byte of a 2-byte address with the contents of two individually programmable registers (RAH1, RAH2) and the fixed values FE_H and FC_H (broadcast address).

Dependent on the result of this comparison, the following bit combinations are possible:

00… RAH2 has been recognized

01… Broadcast address has been recognized

10… RAH1 has been recognized C/R = 0(bit 1)

11… RAH1 has been recognized C/R = 1 (bit 1)

Note: If RAH1, RAH2 contain identical values, a match is indicated by ‘10’or ‘11’.

HFR … **HDLC Frame Format**

0… A BOM frame was received.

1… A HDLC frame was received.

Note: RSIS 7-2, 0 is not valid with a BOM frame.

LA … **Low Byte Address Compare**

Significant in HDLC modes only.

The low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared with two registers. (RAL1, RAL2).

0… RAL2 has been recognized
1… RAL1 has been recognized

Receive Byte Count Low (Read)

	7							0	
RBCL	RBC7							RBC0	(x66)

Together with RBCH (bits RBC11 - RBC8), indicates the length of a received frame (1…4095 bytes). Bits RBC4-0 indicate the number of valid bytes currently in RFIFO. These registers must be read by the CPU following a RME interrupt.

Received Byte Count High (Read)

Value after RESET: 000_{xxxxx}

	7							0	
RBCH				OV	RBC11			RBC8	(x67)

OV… **Counter Overflow**

More than 4095 bytes received.

RBC11 – RBC8… **Receive Byte Count (most significant bits)**

Together with RBCL (bits RBC7… RBC0) indicate the length of the received frame.

Interrupt Status Register 0 (Read)

Value after RESET: 00_H

	7							0	
ISR0	RME	RFS/BIV	ISF	RMB	RSC	CRC6	PDEN	RPF	(x68)

All bits are reset when ISR0 is read.

If bit GCR.VIS is set to ‘1’, interrupt statuses in ISR0 may be flagged although they are masked via register IMR0. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

RME… **Receive Message End**

One complete message of length less than 32 bytes, or the last part of a frame at least 32 bytes long is stored in the receive FIFO, including the status byte.

The complete message length can be determined reading the RBCH, RBCL registers, the number of bytes currently stored in RFIFO is given by RBC4-0. Additional information is available in the RSIS register.

RFS / BIV … **Receive Frame Start**

This is an early receiver interrupt activated after the start of a valid frame has been detected, i.e. after an address match (in operation modes providing address recognition), or after the opening flag (transparent mode 0) is detected, delayed by two bytes. After a RFS interrupt, the contents of RAL1and RSIS.3-1 are valid and can be read by the CPU.

BOM Frame Invalid

Only valid if CCR2.RBFE is set.

When the BOM receiver left the valid BOM status (detecting 7 out of 10 equal BOM frames) this interrupt is generated.

ISF… **Incorrect Sync Format**

The QuadFALC could not detect eight consecutive one’s within 32 bits in BOM mode. Only valid if BOM receiver has been activated.

RMB… **Receive Multiframe Begin**

This bit is set with the beginning of a received multiframe of the receive line timing.

RSC… **Received Signaling Information Changed**

This interrupt bit is set during each multiframe in which signaling information on at least one channel changes its value from the previous multiframe. This interrupt will only occur in the synchronous state. The registers RS1-12 should be read within the next 3 ms otherwise the contents may be lost.

CRC6… **Receive CRC6 Error**

0… No CRC6 error occurs.

1… The CRC6 check of the last received multiframe failed.

PDEN… **Pulse Density violation**

The pulse density violation of the received data stream defined by ANSI T1. 403 is violated. More than 14 consectuive zeros or less than N ones in each and every time window of 8(N+1) data bits (N=23) are detected. If GCR.SCI is set high this interrupt status bit will be activated with every change of state of FRS1.PDEN.

RPF… **Receive Pool Full**

32 bytes of a frame have arrived in the receive FIFO. The frame is not yet completely received.

Interrupt Status Register 1 (Read)

	7							0	
ISR1	CASE	RDO	ALLS	XDU	XMB		XLSC	XPR	(x69)

All bits are reset when ISR1 is read.

If bit GCR.VIS is set to ‘1’, interrupt statuses in ISR1 may be flagged although they are masked via register IMR1. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

CASE… **Transmit CAS Register Empty**

In ESF format this bit is set with the beginning of a transmitted multiframe related to the internal transmitter timing. In F12 + F72 format this interrupt will occur every 24 frames to inform the user that new bit robbing data has to written to XS1-12 registers. This interrupt will only be generated if the serial signaling access on the system highway is not enabled.

RDO… **Receive Data Overflow**

This interrupt status indicates that the CPU does not respond quickly enough to an RPF or RME interrupt and that data in RFIFO has been lost. Even when this interrupt status is generated, the frame continues to be received when space in the RFIFO is available again.

Note: Whereas the bit RSIS.RDO in the frame status byte indicates whether an overflow occurred when receiving the frame currently accessed in the RFIFO, the ISR1.RDO interrupt status is generated as soon as an overflow occurs and does not necessarily pertain to the frame currently accessed by the processor.

ALLS… **All Sent**

This bit is set if the last bit of the current frame is completely sent out and XFIFO is empty.

XDU… **Transmit Data Underrun**

Transmitted frame was terminated with an abort sequence because no data was available for transmission in XFIFO and no XME was issued.

Note: Transmitter and XFIFO are reset and deactivated if this condition occurs. They are re-activated not before this interrupt status register has been read. Thus, XDU should not be masked via register IMR1.

XMB… **Transmit Multiframe Begin**

This bit is set with the beginning of a transmitted multiframe related to the internal transmit line interface timing.

XLSC… **Transmit Line Status Change**

XLSC is set to one with the rising edge of the bit FRS1.XLO or with any change of bit FRS1.XLS.

The actual status of the transmit line monitor can be read from the FRS1.XLS and FRS1.XLO.

XPR… **Transmit Pool Ready**

A data block of up to 32 bytes can be written to the transmit FIFO. XPR enables the fastest access to XFIFO. It has to be used for transmission of long frames, back-to-back frames or frames with shared flags.

Interrupt Status Register 2 (Read)

	7							0	
ISR2	FAR	LFA	MFAR	LMFA	AIS	LOS	RAR	RA	(x6A)

All bits are reset when ISR2 is read.

If bit GCR.VIS is set to ‘1’, interrupt statuses in ISR2 may be flagged although they are masked via register IMR2. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

FAR… **Frame Alignment Recovery**

The framer has reached synchronization. Set with the falling edge of bit FSR0.LFA.

It is set also after alarm simulation is finished and the receiver is still synchron.

LFA… **Loss of Frame Alignment**

The framer has lost synchronization and bit FRS0.LFA is set.
It will be set during alarm simulation.

MFAR… **Multiframe Alignment Recovery**

Set when the framer has reached multiframe alignment in F12 or F72 format. With the negative transition of bit FRS0.LMFA this bit will be set. It will be set during alarm simulation.

LMFA… **Loss of Multiframe Alignment**

Set when the framer has lost the multiframe alignment in F12 or F72 format. With the positive transition of bit FRS0.LMFA this bit will be set. It will be set during alarm simulation.

AIS… **Alarm Indication Signal (Blue Alarm)**

This bit is set when an alarm indication signal is detected and bit FRS0.AIS is set. If GCR.SCI is set high this interrupt status bit will be activated with every change of state of FRS0.AIS.
It will be set during alarm simulation.

LOS… **Loss of Signal (Red Alarm)**

This bit is set when a loss of signal alarm is detected in the received data stream and FRS0.LOS is set. If GCR.SCI is set high this interrupt status bit will be activated with every change of state of FRS0.LOS.
It will be set during alarm simulation.

RAR… **Remote Alarm Recovery**

Set if a remote alarm (yellow alarm) is cleared and bit FRS0.RRA is reset. It is set also after alarm simulation is finished and no remote alarm is detected.

RA… **Remote Alarm**

A remote alarm (yellow alarm) is detected. Set with the rising edge of bit FRS0.RRA. It will be set during alarm simulation.

Interrupt Status Register 3 (Read)

	7							0	
ISR3	ES	SEC			LLBSC		RSN	RSP	(x6B)

All bits are reset when ISR3 is read.

If bit GCR.VIS is set to ‘1’, interrupt statuses in ISR3 may be flagged although they are masked via register IMR3. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

ES… **Errored Second**

This bit is set if at least one enabled interrupt source via ESM is set during the time interval of one second. Interrupt sources of ESM register:

LFA = Loss of frame alignment detected
FER = Framing error received
CER = CRC error received
AIS = Alarm indication signal (blue alarm)
LOS = Loss of signal (red alarm)
CVE = Code violation detected
SLIP= Transmit Slip or Receive Slip positive/negative detected

SEC… **Second Timer**

The internal one second timer has expired. The timer is derived from clock RCLK.

LLBSC… **Line Loop Back Status Change / PRBS Status Change**

Depending on bit LCR1.EPRM the source of this interrupt status changed:

LCR1.EPRM=0: This bit is set to one, if the LLB actuate signal or the LLB deactuate signal respective is detected over a period of 33,16 msec with a bit error rate less than 1/100.

The LLBSC bit is also set to one, if the current detection status is left, i.e., if the bit error rate exceeds 1/100.

The actual detection status can be read from the FRS1.LLBAD and FRS1.LLBDD, respective.

PRBS Status Change

LCR1.EPRM=1: With any change of state of the PRBS synchronizer this bit will be set. The current status of the PRBS synchronizer is indicated in FRS1.LLBAD.

RSN… **Receive Slip Negative**

The frequency of the receive route clock is greater than the frequency of the receive system interface working clock based on 1.544 MHz. A frame will be skipped. It will be set during alarm simulation.

RSP… **Receive Slip Positive**

The frequency of the receive route clock is less than the frequency of the receive system interface working clock based on 1.544 MHz. A frame will be repeated. It will be set during alarm simulation.

Interrupt Status Register 4(Read)

	7							0	
ISR4	XSP	XSN							(x6C)

All bits are reset when ISR4 is read.

If bit GCR.VIS is set to ‘1’, interrupt statuses in ISR4 may be flagged although they are masked via register IMR4. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

XSP… **Transmit Slip Positive**

The frequency of the transmit clock is less than the frequency of the transmit system interface working clock based on 1.544 MHz. A frame will be repeated. After a slip has performed writing of register XC1 is not necessary.

XSN… **Transmit Slip Negative**

The frequency of the transmit clock is greater than the frequency of the transmit system interface working clock based on 1.544 MHz. A frame will be skipped. After a slip has performed writing of register XC1 is not necessary.

Global Interrupt Status Register (Read)

Value after RESET: 00_H

	7							0	
GIS				ISR4	ISR3	ISR2	ISR1	ISR0	(x6E)

This status register points to pending interrupts sourced by ISR4 ... ISR0.

Channel Interrupt Status Register (Read)

Value after RESET: 00_H

	7							0	
CIS					GIS4	GIS3	GIS2	GIS1	(6F)

This status register points to pending interrupts sourced by the GIS registers of each channel.

GIS4 ... register GIS of FALC4
GIS3 ... register GIS of FALC3
GIS2 ... register GIS of FALC2
GIS1 ... register GIS of FALC1

Receive Signaling Register (Read)

Value after RESET: not defined

	7							0	
RS1	A1	B1	C1/A2	D1/B2	A2/A3	B2/B3	C2/A4	D2/B4	(x70)
RS2	A3/A5	B3/B5	C3/A6	D3/B6	A4/A7	B4/B7	C4/A8	D4/B8	(x71)
RS3	A5/A9	B5/B9	C5/A10	D5/B10	A6/A11	B6/B11	C6/A12	D6/B12	(x72)
RS4	A7/A13	B7/B13	C7/A14	D7/B14	A8/A15	B8/B15	C8/A16	D8/B16	(x73)
RS5	A9/A17	B9/B17	C9/A18	D9/B18	A10/A19	B10/B19	C10/A20	D10/B20	(x74)
RS6	A11/A21	B11/B21	C11/A22	D11/B22	A12/A23	B12/B23	C12/A24	D12/B24	(x75)
RS7	A13/A1	B13/B1	C13/A2	D13/B2	A14/A3	B14/B3	C14/A4	D14/B4	(x76)
RS8	A15/A5	B15/B5	C15/A6	D15/B6	A16/A7	B16/B7	C16/A8	D16/B8	(x77)
RS9	A17/A9	B17/B9	C17/A10	D17/B10	A18/A11	B18/B11	C18/A12	D18/B12	(x78)
RS10	A19/A13	B19/B13	C19/A14	D19/B14	A20/A15	B20/B15	C20/A16	D20/B16	(x79)
RS11	A21/A17	B21/B17	C21/A18	D21/B18	A22/A19	B22/B19	C22/A20	D22/B20	(x7A)
RS12	A23/A21	B23/B21	C23/A22	D23/B22	A24/A23	B24/B23	C24/A24	D24/B24	(x7B)

Receive Signaling Register 1-12

Each register contains the received bit robbing information for 8 DS0 channels. The received robbed bit signaling information of a complete ESF multiframe will be compared with the previously received one. In F12/72 frame format the received signaling information of every 24 frames will be compared with the previously received 24 frames. If the contents changed a Receive Signaling Changed interrupt ISR0.RSC is generated and informs the user that a new multiframe has to be read within the next 3 ms. Received data will be stored in RS1-12 registers. The RS1.7 is received in channel 1 frame 1 and RS12.0 in channel 24 frame 24 (ESF).

If requests for reading the RS1-12 registers will be ignored the received data may be lost.

Additionally a receive signaling data change pointer indicates an update of register RS1-12 . Refer also to register RSP1/2.
Access to RS1-12 registers is only valid if the serial receive signaling access on the system highway is disabled.

9 Preliminary Electrical Characteristics

9.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	– 40 to 85	°C
Storage temperature	T_{stg}	– 65 to 150	°C
IC supply voltage digital	V_{DD}	– 0.3 to 5.5	V
IC supply voltage receive	V_{DDR}	– 0.3 to 5.5	V
IC supply voltage transmit	V_{DDX}	– 0.3 to 5.5	V
Voltage on any pin with respect to ground	V_S	– 0.3 to 5.5	V
ESD robustness[1)] HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	1000	V

1) According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Ambient temperature	T_A	- 40	85	°C	
Supply voltage digital	V_{DD}	3.135	3.465	V	
Supply voltage receive	V_{DDR}	3.135	3.465	V	
Supply voltage transmit	V_{DDX}	3.135	3.465	V	
Ground digital	V_{SS}	0	0	V	
Ground receive	V_{SSR}	0	0	V	
Ground transmit	V_{SSX}	0	0	V	

Note: In the operating range, the functions given in the circuit description are fulfilled.
*V_{DD}, V_{DDR} and V_{DDX} have to be connected to the **same** voltage level;*
V_{SS}, V_{SSR} and V_{SSX} have to be connected to ground level.

9.3 DC Characteristics

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input low voltage	V_{IL}	– 0.4	0.8	V	1)
Input high voltage	V_{IH}	2.0	V_{DD}+ 0.4	V	1)
Output low voltage	V_{OL}		0.45	V	I_{OL} = + 2 mA 1)
Output high voltage	V_{OH}	2.4		V	I_{OH} = - 2 mA 1)
Avg. power supply current (Analog line interface)	I_{DDE1} I_{DDT1}		300 350	mA mA	E1 application2) T1 application3)
Avg. power supply current (Digital line interface)	I_{DD}		90	mA	SIC1.SSC1/0 = 10
Power down current	I_{PD}		10	mA	Register GCR.PD=0, all 4 single FALCs
Input leakage current	I_{IL11}		1	µA	$V_{IN} = V_{DD}$ 4)
Input leakage current	I_{IL12}		1	µA	$V_{IN} = V_{SS}$ 4)
Input leakage current	I_{IL21}		1	µA	$V_{IN} = V_{DD}$ 5)
Input leakage current	I_{IL12}		250	µA	$V_{IN} = V_{SS}$ 5)
Output leakage current	I_{OZ}		1	µA	V_{OUT} = *tristate*1) $V_{SS} < V_{meas} < V_{DD}$ measures against V_{DD} and V_{SS}
Transmitter output impedance	R_X		3	Ω	applies to XL1and XL2 6)
Transmitter output current	I_X		100	mA	XL1, XL2
Differential peak voltage of a mark (between XL1 and XL2)	V_X		2.15	V	
Receiver differential peak voltage of a mark (between RL1 and RL2)	V_R		V_{DDR}+0.3	V	RL1, RL2
Receiver input impedance	Z_R	50 (typical value)		kΩ	6)

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Receiver sensitivity	S_{RSH}	0	10	dB	RL1, RL2 LIM0.EQON=0 (short haul)
Receiver sensitivity	S_{RLH}	0	36	dB	RL1, RL2 LIM0.EQON=1 (long haul)
Receiver input threshold	V_{RTH}	55 (typical value)		%	6)
Loss of signal threshold	V_{LOS}	0.90 0.70 0.60 0.40 0.30 0.20 0.10 0.05 (typical values)		V	RIL2-0 = 000 RIL2-0 = 001 RIL2-0 = 010 RIL2-0 = 011 RIL2-0 = 100 RIL2-0 = 101 RIL2-0 = 110 RIL2-0 = 111 6) 7)

1) Applies to all pins except analog pins RLx, TLx

2) The power consumption of the device is calculated by the internal chip consumption minus the consumption of the external transmit line components.
Wiring conditions and external circuit configuration according to **figure 11**;
values of registers: SIC1.SSC1/0=00; XPM2-0 = BD_H, 03_H, 00_H

3) The power consumption of the device is calculated by the internal chip consumption minus the consumption of the external transmit line components.
Wiring conditions and external circuit configuration according to **figure 44**;
values of registers: SIC1.SSC1/0=00; XPM2-0 = $9F_H$, 27_H, 02_H

4) Applies to all pins except RCLK, SCLKR, SYNC, RPA, XPA, TDI, TMS, TCK, RL1, RL2, XL1, XL2

5) Applies to pins RCLK, SCLKR, SYNC, RPA, XPA, TDI, TMS, TCK only

6) Parameter not tested in production

7) Differential input voltage between pins RL1 and RL2; depends on programming of register LIM1.RIL2-0

9.4 AC Characteristics

9.4.1 Input/Output Waveforms for Testing

All inputs except RLx.y are driven to V_{IH} = 2.4 V for a logical “1”
and to V_{IL} = 0.4 V for a logical “0”

Timing measurements except for XLx.y are made at V_H = 2.0 V for a logical “1”
and at V_L = 0.8 V for a logical “0”

The AC testing input/output waveforms are shown below.

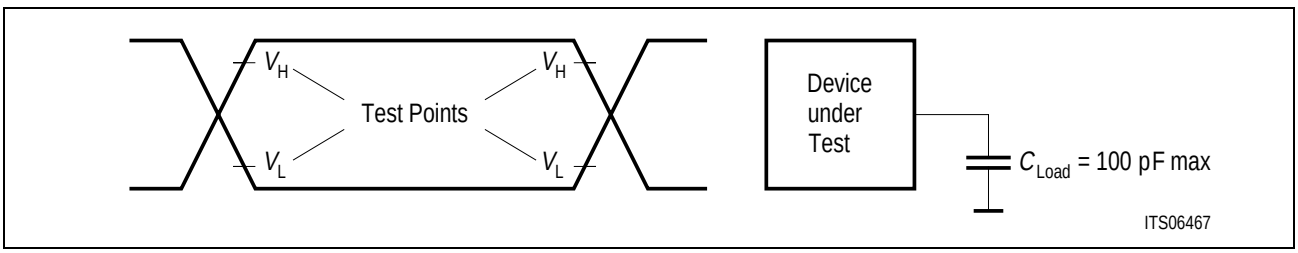


Figure 74
Input/Output Waveform for AC Testing

9.4.2 Master Clock Timing

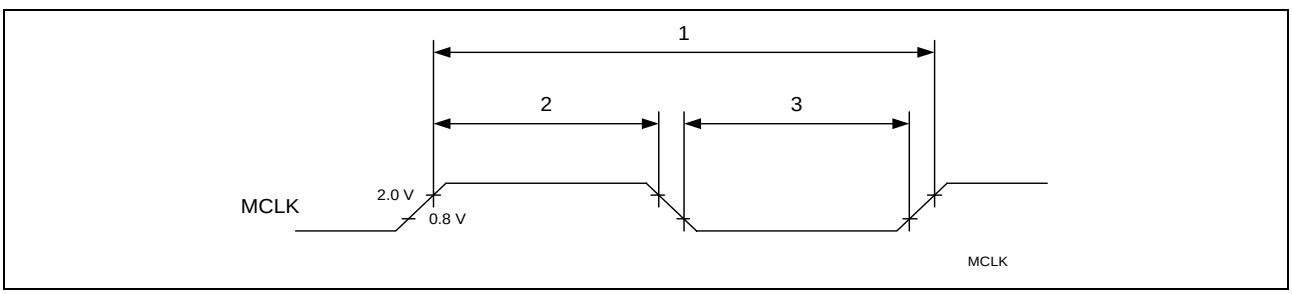


Figure 75
MCLK Timing

Table 32
MCLK Timing Parameter Values

No.	Parameter	Limit Values			Unit	Condition
		min.	typ.	max.		
1	Clock period of MCLK		488		ns	E1
			648		ns	T1
2	High phase of MCLK	40			%	
3	Low phase of MCLK	40			%	
	Clock accuracy			50	ppm	

9.4.3 JTAG Boundary Scan Interface

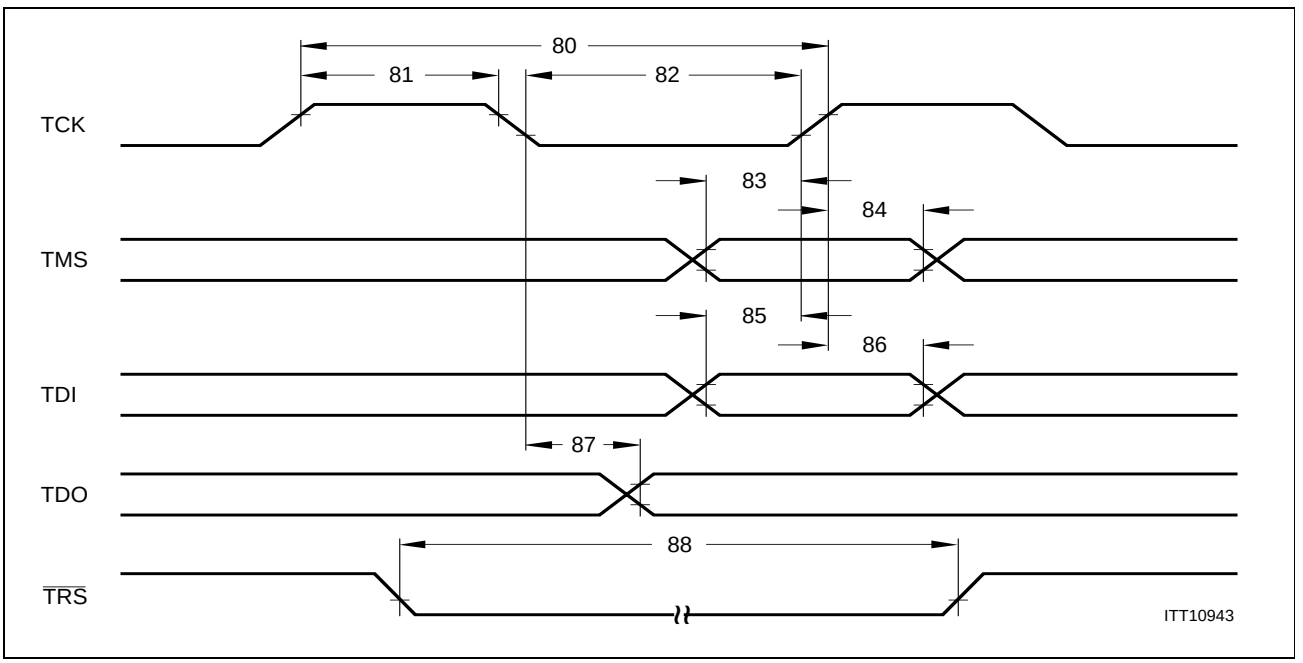


Figure 76
JTAG Boundary Scan Timing

Table 33
JTAG Boundary Scan Timing Parameter Values

No.	Parameter	Limit Values		Unit
		min.	max.	
80	TCK period	250		ns
81	TCK high time	80		ns
82	TCK low time	80		ns
83	TMS setup time	40		ns
84	TMS hold time	40		ns
85	TDI setup time	40		ns
86	TDI hold time	40		ns
87	TDO valid delay		100	ns
88	$\overline{TRS}$ active low	200		ns

Identification Register : 32 bit; Version: $1_{H;}$ Part Number: $4D_H$, Manufacturer: 083_H

9.4.4 Reset

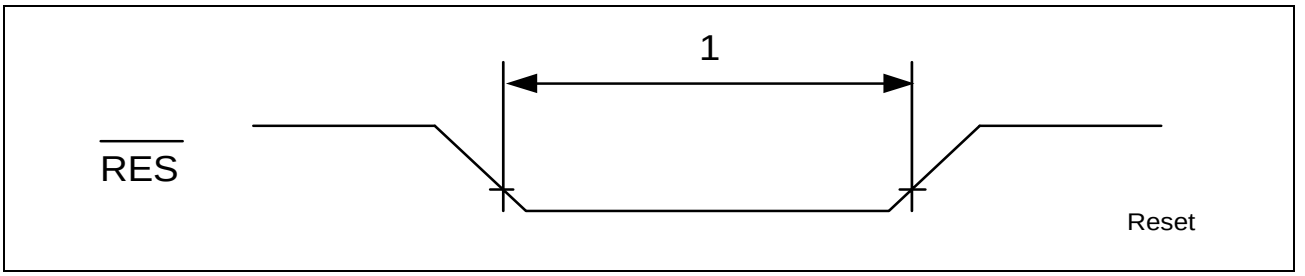


Figure 77
Reset Timing

Table 34
Reset Timing Parameter Values

No.	Parameter	Limit Values		Unit
		min.	max.	
1	$\overline{RES}$ pulse width low	10000[1)]		ns

1) while MCLK is running

9.4.5 Microprocessor Interface

9.4.5.1 Siemens/Intel Bus Interface Mode

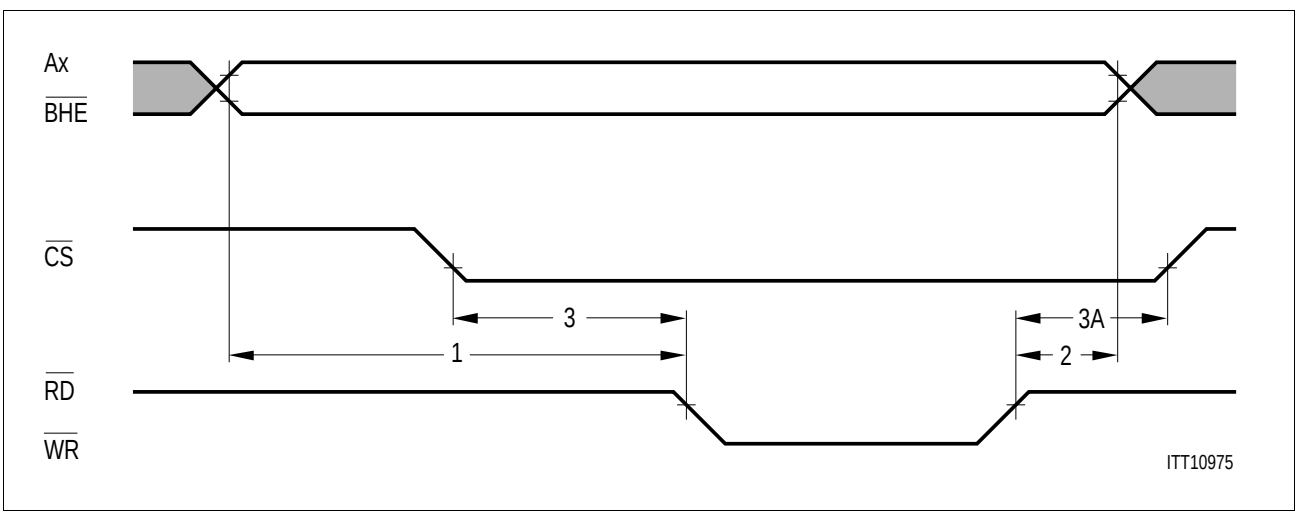


Figure 78
Siemens/Intel Non-Multiplexed Address Timing

Note: Ax = Address pins A0 - A9

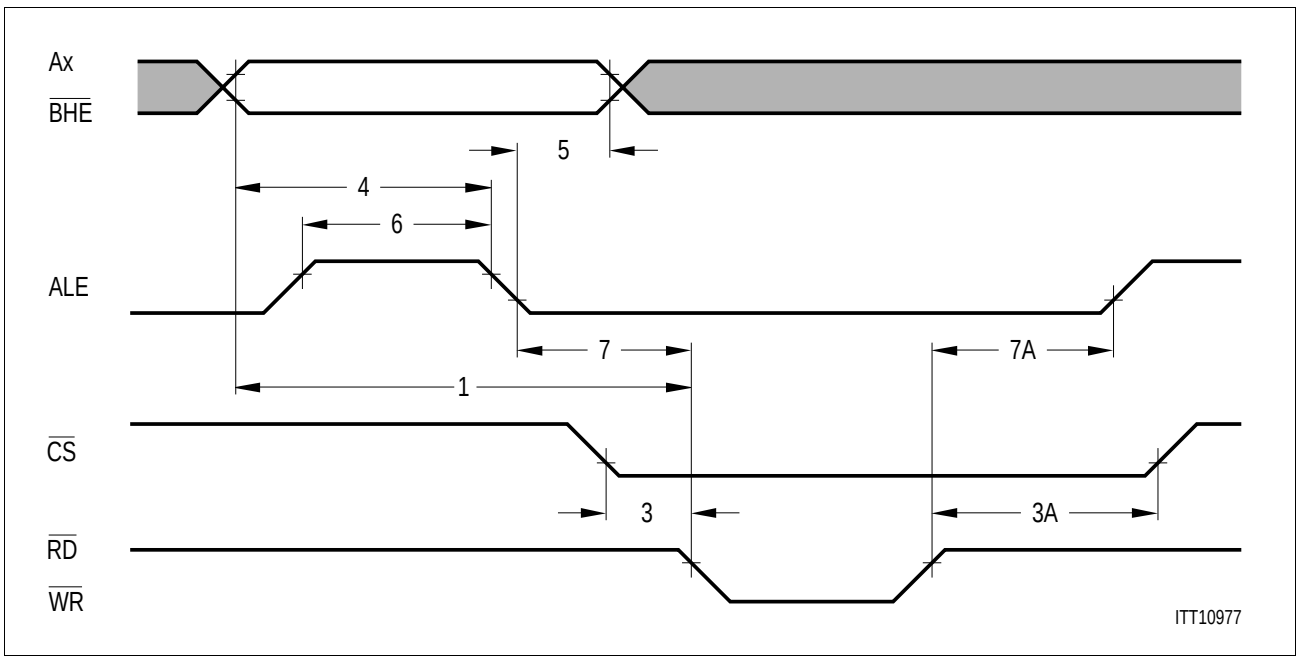


Figure 79
Siemens/Intel Multiplexed Address Timing

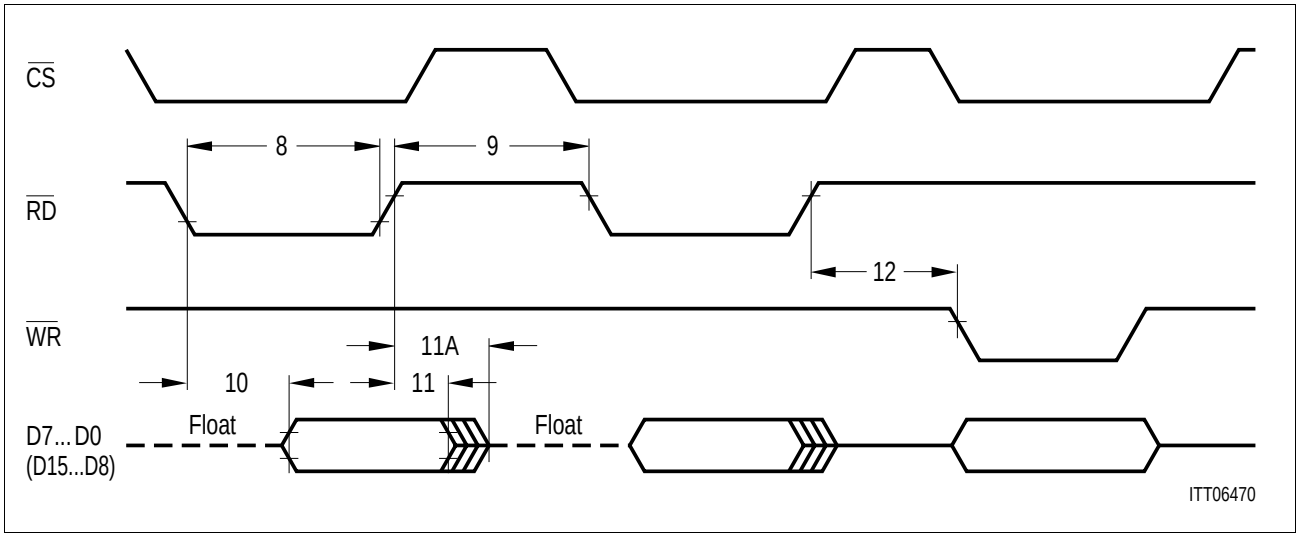


Figure 80
Siemens/Intel Read Cycle Timing

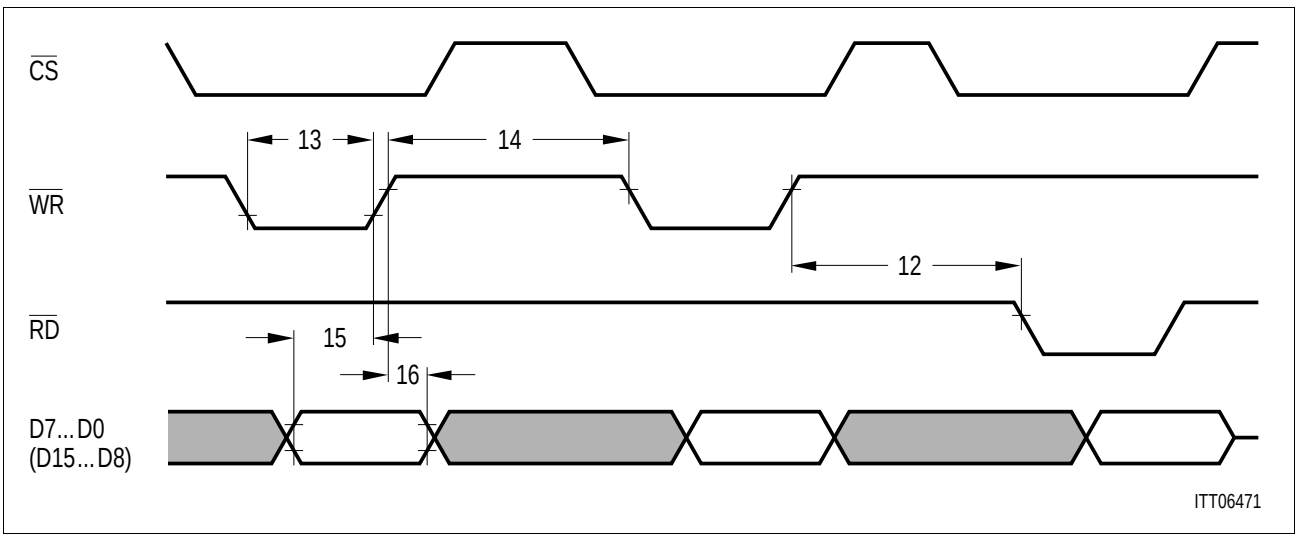


Figure 81
Siemens/Intel Write Cycle Timing

Table 35
Siemens/Intel Bus Interface Timing Parameter Values

No.	Parameter	Limit Values		Unit
		min.	max.	
1	Address, $\overline{BHE}$ setup time	15		ns
2	Address, $\overline{BHE}$ hold time	0		ns
3	$\overline{CS}$ setup time	0		ns
3A	$\overline{CS}$ hold time	0		ns
4	Address, $\overline{BHE}$ stable before ALE inactive	20		ns
5	Address, $\overline{BHE}$ hold after ALE inactive	10		ns
6	ALE pulse width	30		ns
7	Address latch setup time before cmd active	0		ns
7A	ALE to command inactive delay	30		ns
8	$\overline{RD}$ pulse width	80		ns
9	$\overline{RD}$ control interval	70		ns
10	Data valid after $\overline{RD}$ active		75	ns
11	Data hold after $\overline{RD}$ inactive	10		ns
11A	$\overline{RD}$ inactive to data bus tristate[1)]		30	ns
12	$\overline{WR}$ to $\overline{RD}$ or $\overline{RD}$ to $\overline{WR}$ control interval	70		ns

No.	Parameter	Limit Values		Unit
		min.	max.	
13	$\overline{WR}$ pulse width	80		ns
14	$\overline{WR}$ control interval	70		ns
15	Data stable before $\overline{WR}$ inactive	30		ns
16	Data hold after $\overline{WR}$ inactive	10		ns

1) typical value, not tested in production

9.4.5.2 Motorola Bus Interface Mode

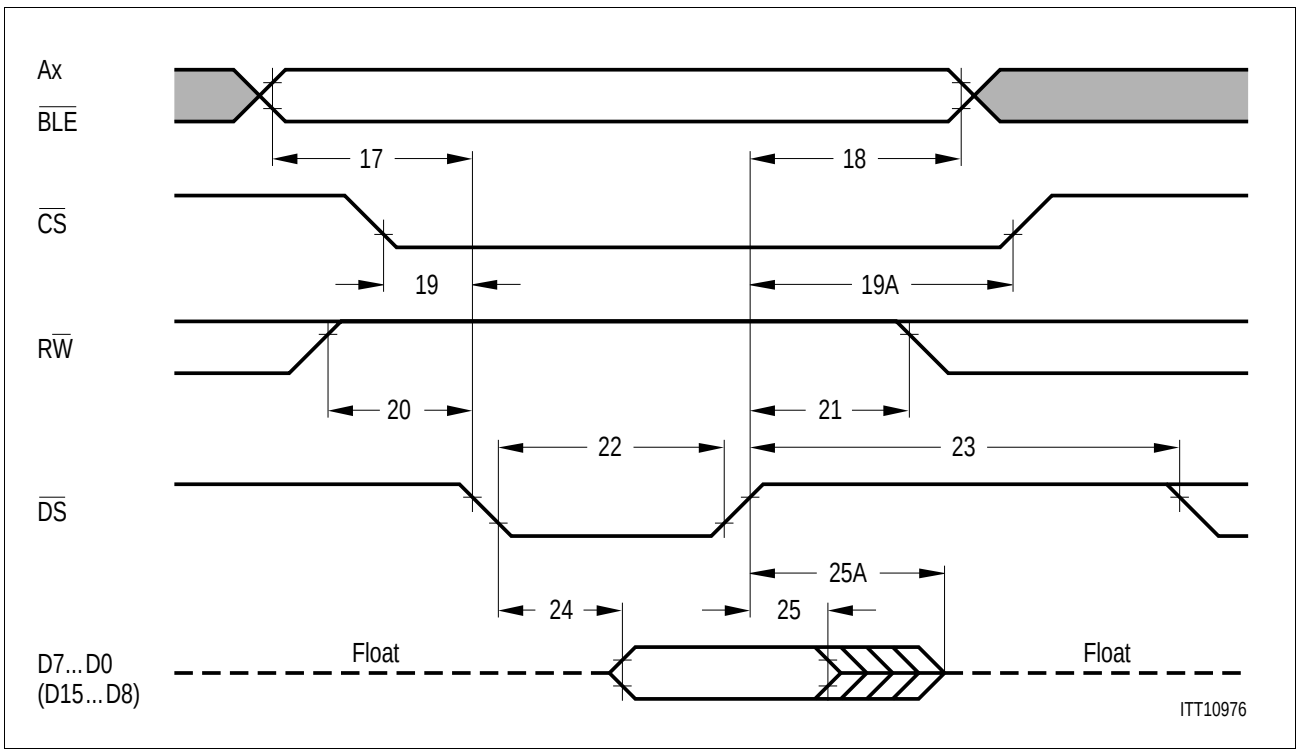


Figure 82
Motorola Read Cycle Timing

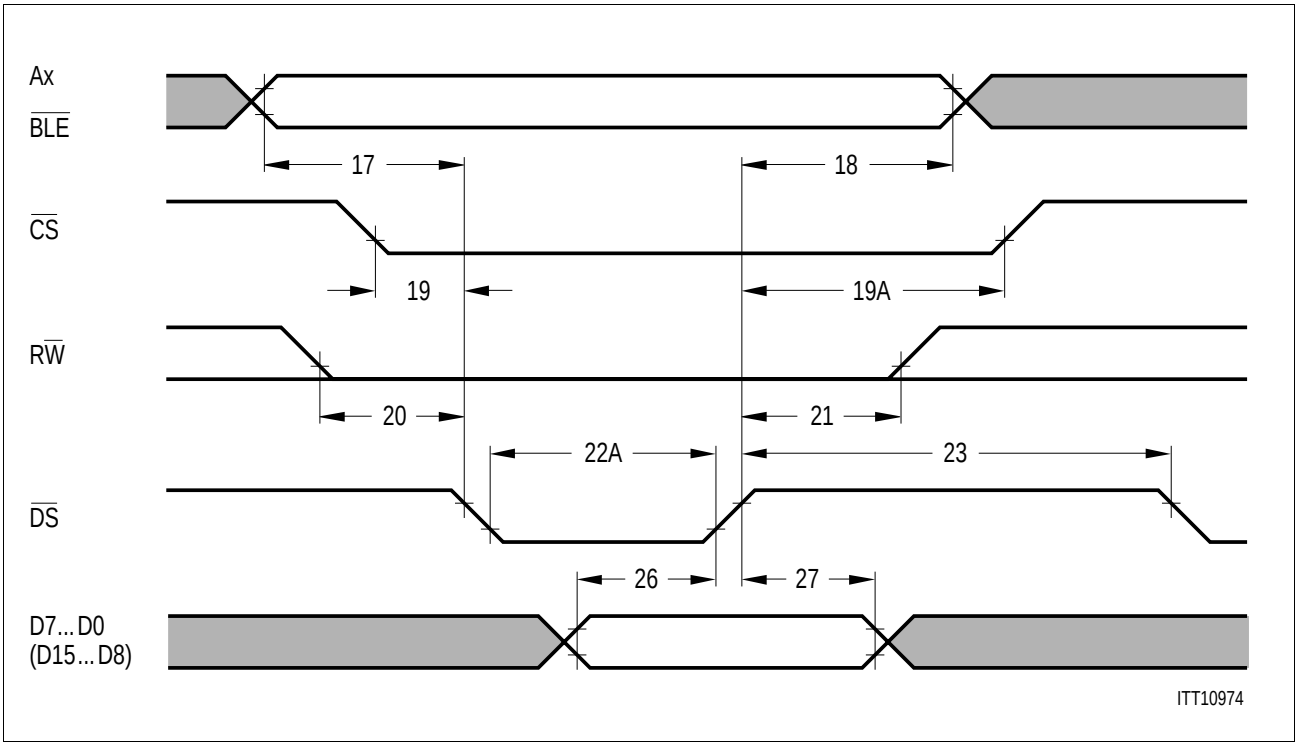


Figure 83
Motorola Write Cycle Timing

Table 36
Motorola Bus Interface Timing Parameter Values

No.	Parameter	Limit Values		Unit
		min.	max.	
17	Address, $\overline{BLE}$, setup time before $\overline{DS}$ active	15		ns
18	Address, $\overline{BLE}$, hold after $\overline{DS}$ inactive	0		ns
19	$\overline{CS}$ active before $\overline{DS}$ active	0		ns
19A	$\overline{CS}$ hold after $\overline{DS}$ inactive	0		ns
20	R$\overline{W}$ stable before $\overline{DS}$ active	10		ns
21	R$\overline{W}$ hold after $\overline{DS}$ inactive	0		ns
22	$\overline{DS}$ pulse width (read access)	80		ns
22A	$\overline{DS}$ pulse width (write access)	70		ns
23	$\overline{DS}$ control interval	70		ns
24	Data valid after $\overline{DS}$ active (read access)		75	ns
25	Data hold after $\overline{DS}$ inactive (read access)	10		ns

No.	Parameter	Limit Values		Unit
		min.	max.	
25A	$\overline{DS}$ inactive to databus tristate (read access)[1)]		30	ns
26	Data stable before $\overline{DS}$ active (write access)	30		ns
27	Data hold after $\overline{DS}$ inactive (write access)	10		ns

1) typical value, not tested in production

9.4.6 Line Interface

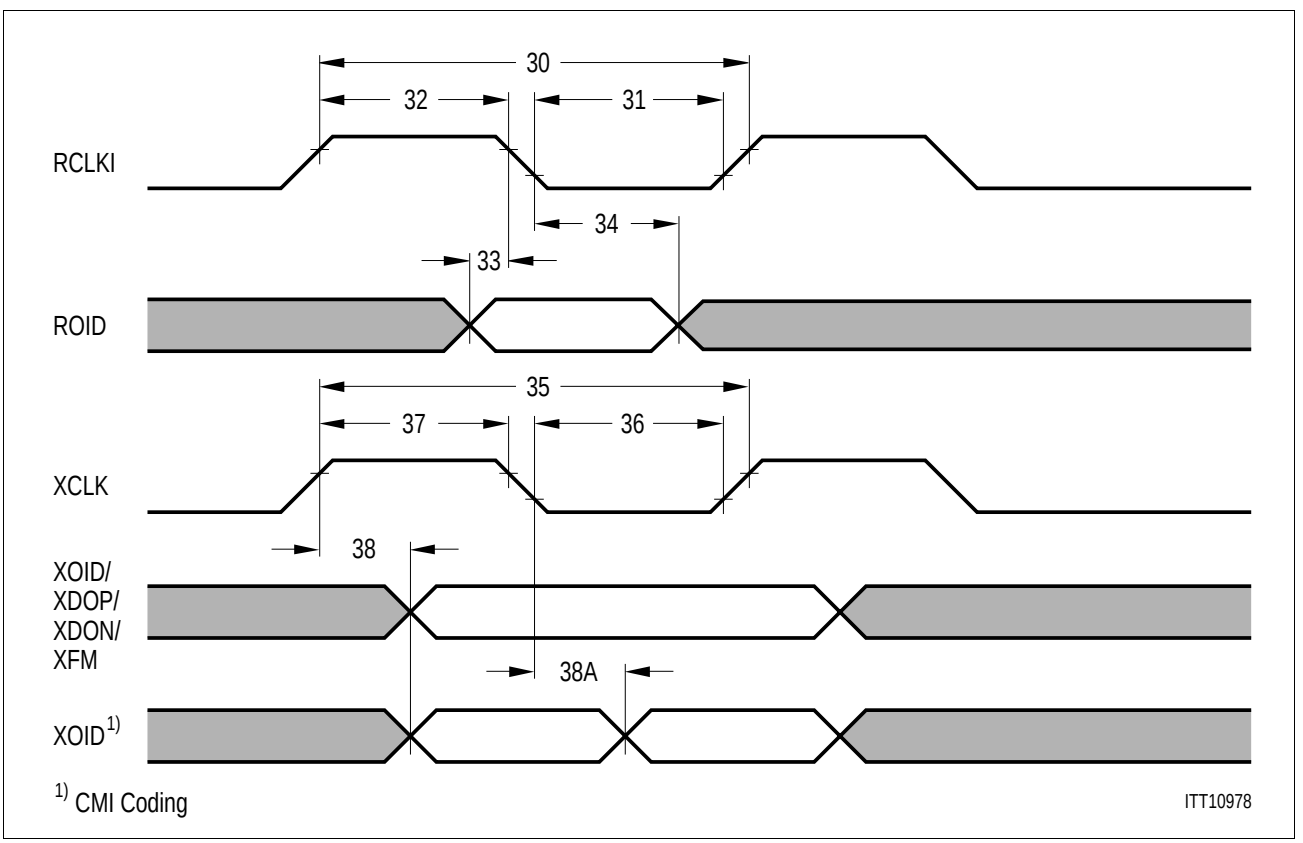


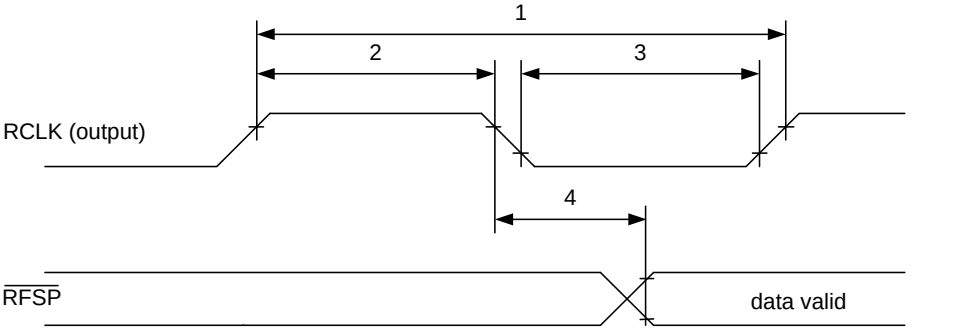
Figure 84
Timing of Dual Rail Optical Interface

Table 37
Dual Rail Optical Interface Parameter Values

No.	Parameter	Limit Values						Unit
		E1			T1			
		min.	typ.	max.	min.	typ.	max.	
30	RCLKI clock period		488			648		ns
31	RCLKI clock period low	180			240			ns
32	RCLKI clock period high	180			240			ns
33	ROID setup	50			50			ns
34	ROID hold	50			50			ns
35	XCLK clock period		488			648		ns
36	XCLK clock period low XCLK clock period low[4)]	190 150			230 200			ns
37	XCLK clock period high XCLK clock period high[4)]	190 150			230 200			ns
38	XOID delay[1)] XDOP/XDON delay[2)]			60			60	ns
38A	XOID delay[3)]			60			60	ns
	RCLK (output)		488 122			648 162		ns ns
	RCLK clock period low	40		60	40		60	%
	RCLK clock period high	40		60	40		60	%

1) NRZ coding
2) HDB3/AMI/B8ZS coding
3) CMI coding
4) depends on input RCLKI in optical interface and remote loop without transmit jitter attenuator enabled (LIM1.JATT/RL=01).

9.4.7 System Interface



1) active edge can be programmed to be positive or negative (only negative edge timing shown here)

valid only, if RCLK is derived from DPLL (not, if RCLK is jitter attenuated)

RFSP

Figure 85
RCLK, RFSP Output Timing

Table 38
RCLK, $\overline{\text{RFSP}}$ Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	RCLK period E1 (2.048 MHz)		488		ns
	RCLK period E1 (2.048 MHz x 4)		122		ns
	RCLK period T1 (1.544 MHz)		648		ns
	RCLK period T1 (1.544 MHz x 4)		162		ns
2	RCLK pulse high	40		60	%
3	RCLK pulse low	40		60	%
4	$\overline{\text{RFSP}}$ delay			80	ns

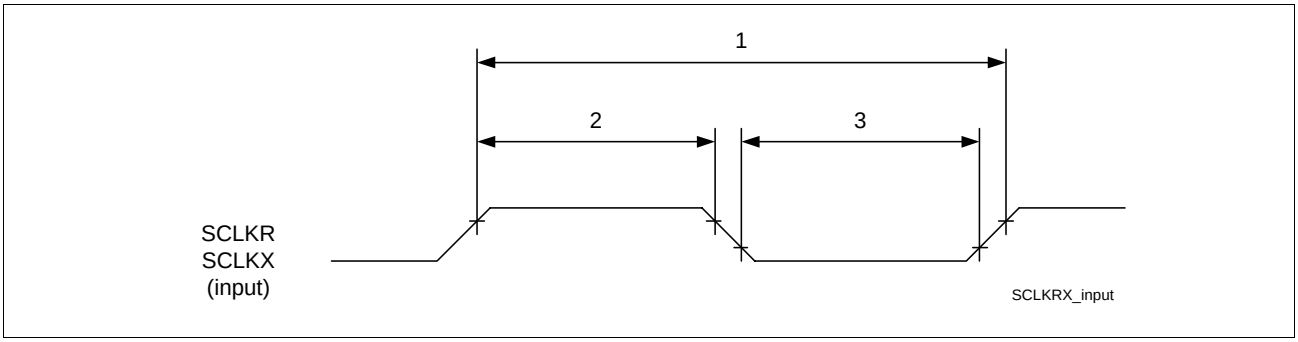


Figure 86
SCLKR/SCLKX Input Timing

Table 39
SCLKR/SCLKX Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	SXLKR/SCLKX period at 16.384 MHz		61		ns
1	SXLKR/SCLKX period at 8.192 MHz		122		ns
1	SXLKR/SCLKX period at 4.096 MHz		244		ns
1	SXLKR/SCLKX period at 2.048 MHz		488		ns
1	SXLKR/SCLKX period at 12.352 MHz		81		ns
1	SXLKR/SCLKX period at 6.176 MHz		162		ns
1	SXLKR/SCLKX period at 3.088 MHz		324		ns
1	SXLKR/SCLKX period at 1.544 MHz		648		ns
2	SCLKR/SCLKX pulse high	40			%
3	SCLKR/SCLKX pulse low	40			%

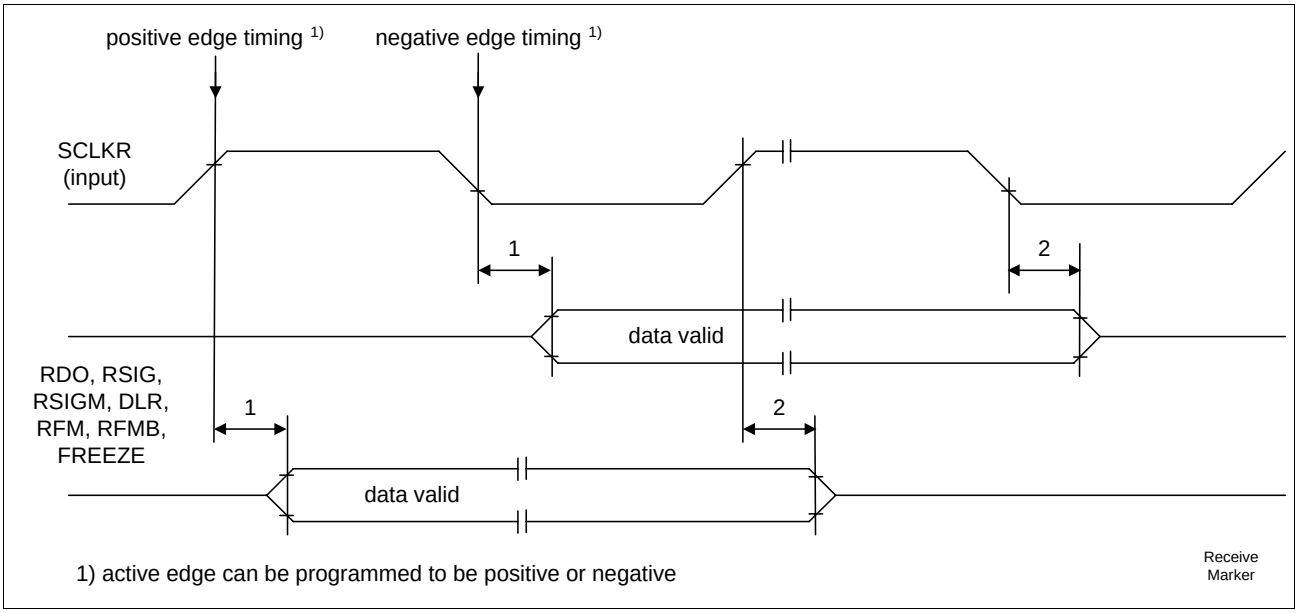


Figure 87
System Interface Marker Timing (Receive)

Table 40
System Interface Marker Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	RDO, RSIG delay			100	ns
2	RSIGM, RMFB, DLR, RFM, FREEZE marker delay			100	ns

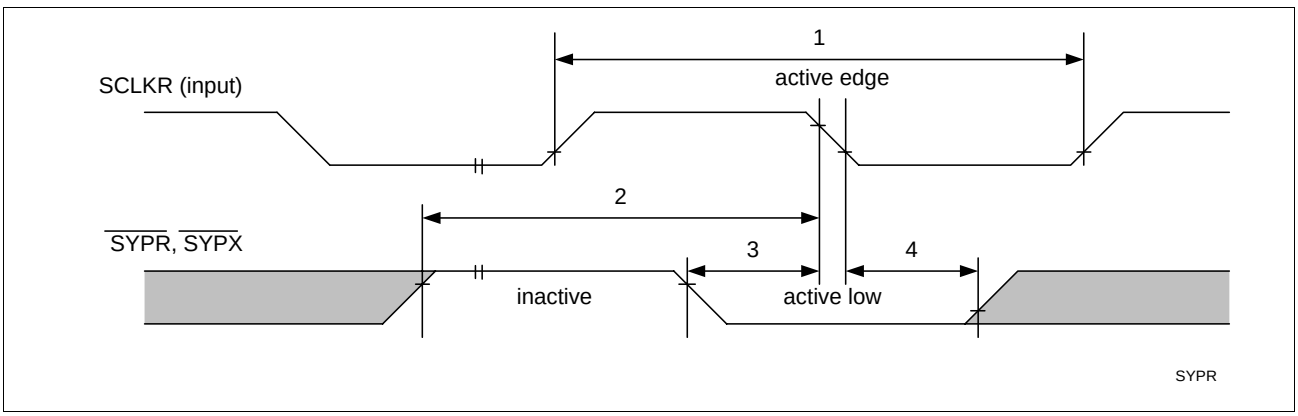


Figure 88
$\overline{\text{SYPR}}$, $\overline{\text{SYPX}}$ Timing

Table 41
$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	SCLKR period (t_1)	61		648	ns
2	$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ inactive setup time[1)]	4 x t_1			ns
3	$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ setup time	5			ns
4	$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ hold time	50			ns

1) typical value, not testd in production

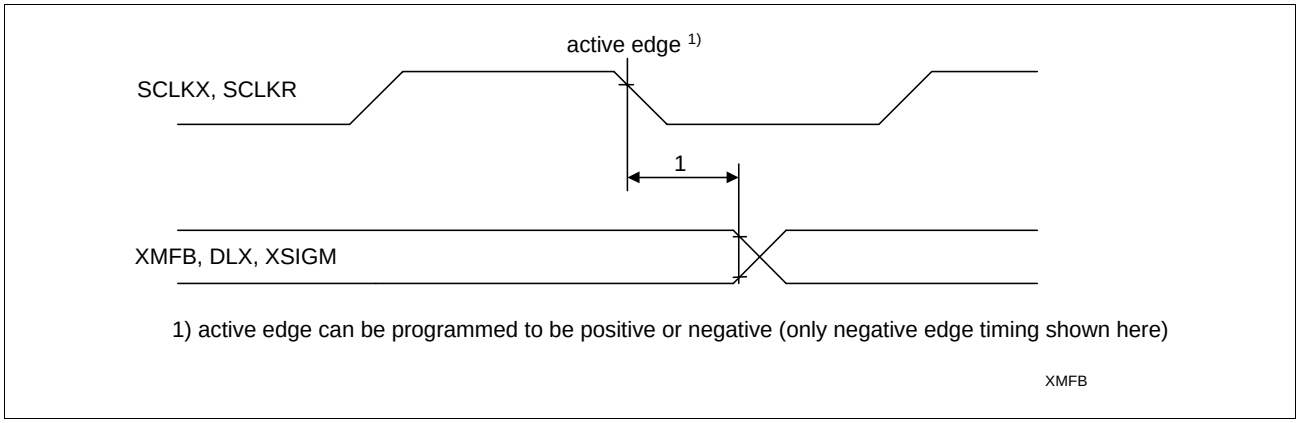


Figure 89
System Interface Marker Timing (Transmit)

Table 42
System Interface Marker Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	XMFB, DLX, XSIGM delay			100	ns

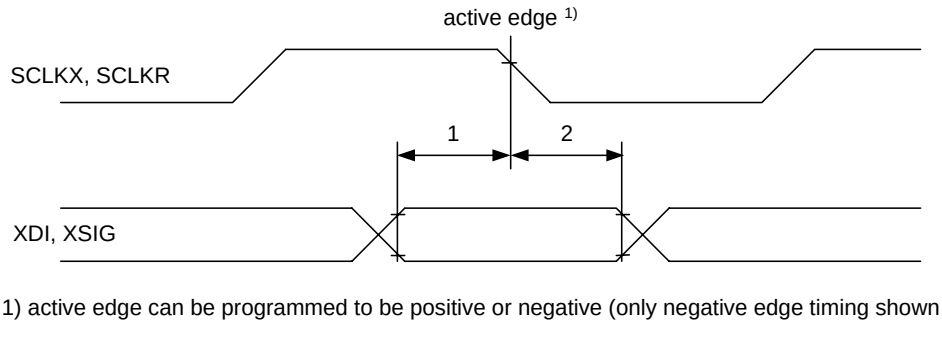


Figure 90
XDI, XSIG Timing

Table 43
XDI, XSIG Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	XSIG, XDI setup time	5			ns
2	XSIG, XDI hold time	55			ns

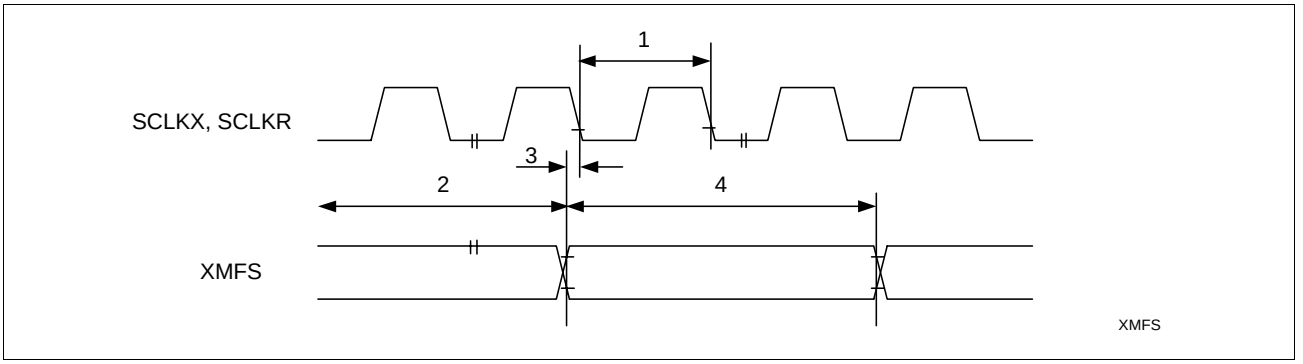


Figure 91
XMFS Timing

Table 44
XMFS Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	SCLKR/SCLKX period (t_1)		1)		ns
2	XMFS inactive Setup Time 2)	4 x t_1			ns
3	XMFS Setup Time	5			ns
4	XMFS Hold Time	50			ns

1) depending on application

2) typical value, not tested in production

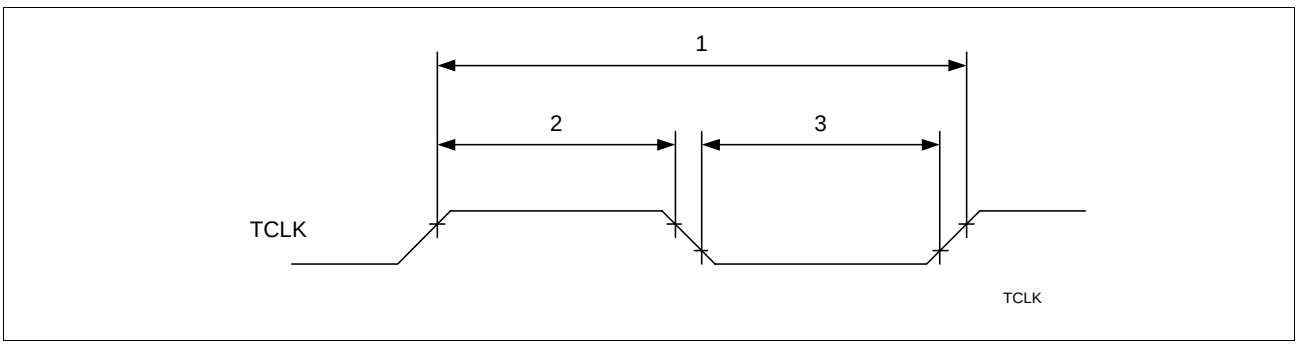


Figure 92
TCLK Input Timing

Table 45
TCLK Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	TCLK period E1 (2.048 MHz)		488		ns
	TCLK period E1 (2.048 MHz x 4)		122		ns
	TCLK period T1 (1.544 MHz)		648		ns
	TCLK period T1 (1.544 MHz x 4)		162		ns
2	TCLK high	40			%
3	TCLK low	40			%

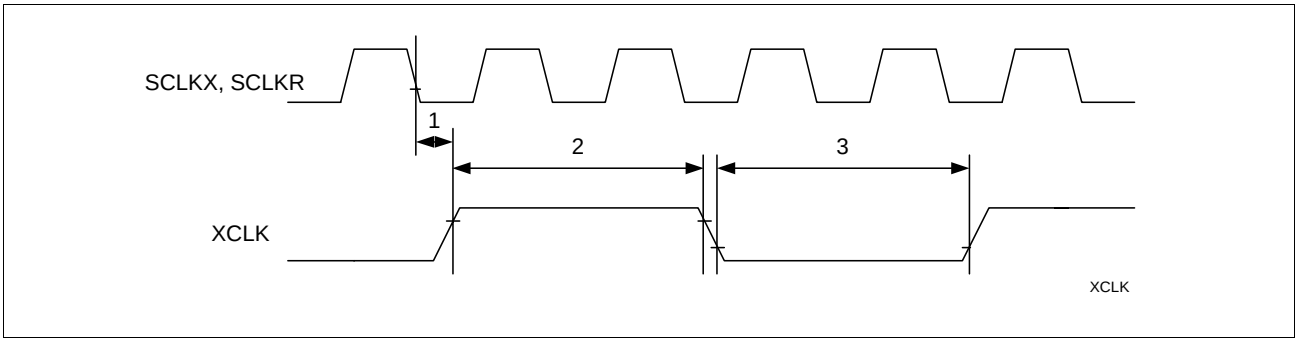


Figure 93
XCLK Timing

Table 46
XCLK Timing Parameter values

No.	Parameter	Limit Values						Unit
		E1			T1			
		min.	typ.	max.	min.	typ.	max.	
1	XCLK delay			100			100	ns
2	XCLK clock period low	190			230			ns
	XCLK clock period low[1)]	150			200			ns
3	XCLK clock period high	190			230			ns
	XCLK clock period high[1)]	150			200			ns

1) depends on input RCLKI in optical interface and remote loop without transmit jitter attenuator enabled (LIM1.JATT/RL=01)

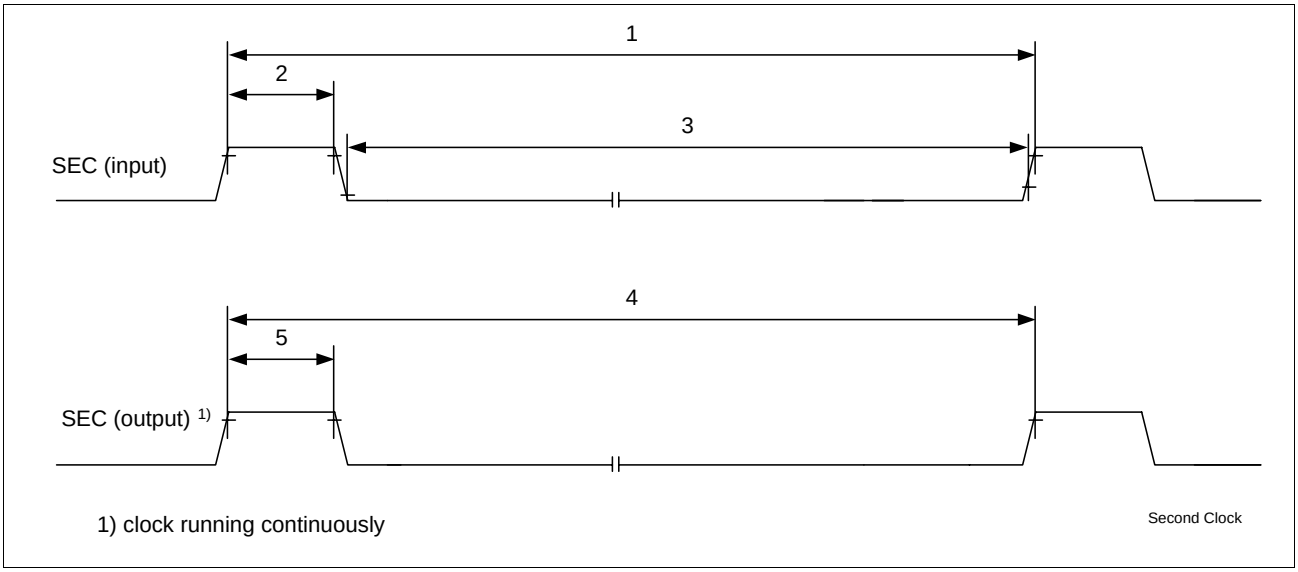


Figure 94
SEC Timing

Table 47
SEC Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	SEC input period E1		1		s
2	SEC input high E1	976			ns
	SEC input high T1	1296			ns
3	SEC input low E1	976			ns
	SEC input low T1	1296			ns
4	SEC output period		1		s
5	SEC high output E1	976			ns
	SEC high output T1	1296			ns

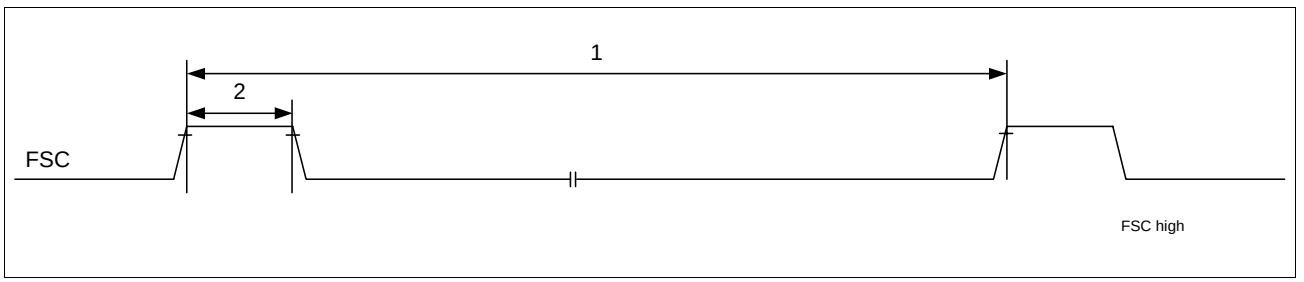


Figure 95
$\overline{\text{FSC}}$ Timing

Table 48
FSC Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	FSC period		125		µs
2	FSC low time E1		488		ns
2	FSC low time T1		648		ns

9.4.8 Pulse Templates - Transmitter

9.4.8.1 Pulse Template E1

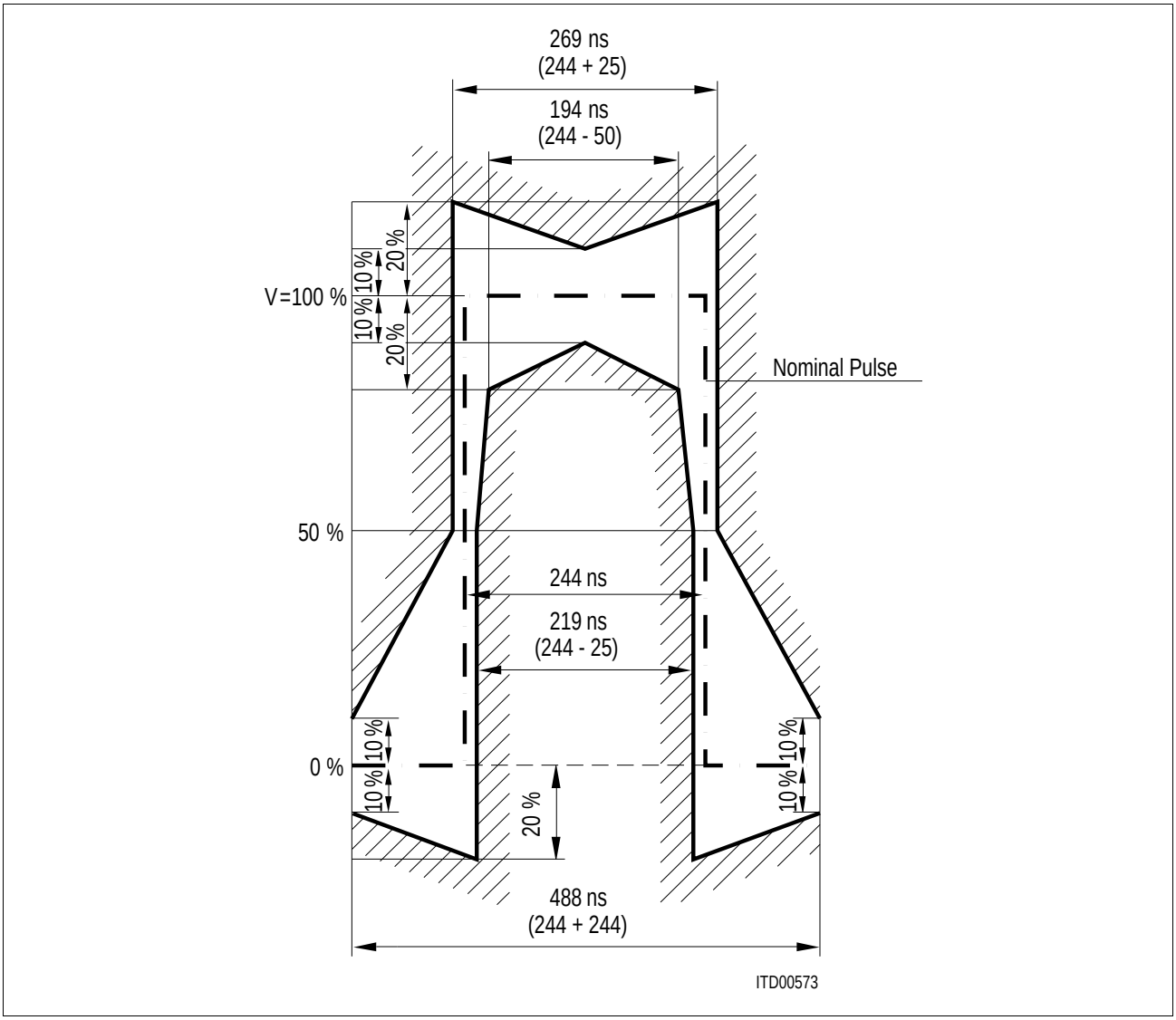


Figure 96
E1 Pulse Shape at Transmitter Output for CEPT Applications

9.4.8.2 Pulse template T1

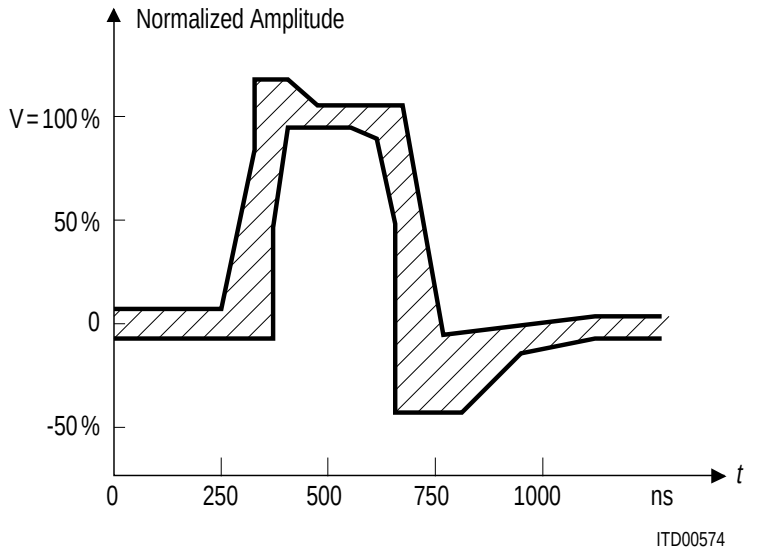


Figure 97
T1 Pulse Shape at the Cross Connect Point

Table 49
T1 Pulse Template Corner Points at the Cross Connect Point (T1.102)

Maximum Curve		Minimum Curve	
Time [ns]	**V [%]**	**Time [ns]**	**V [%]**
(0,	0.05)	(0,	-0.05)
(250,	0.05)	(350,	-0.05)
(325,	0.80)	(350,	0.5)
(325,	1.15)	(400,	0.95)
(425,	1.15)	(500,	0.95)
(500,	1.05)	(600,	0.90)
(675,	1.05)	(650,	0.50)
(725,	-0.07)	(650,	-0.45)
(1100,	0.05)	(800,	-0.45)
(1250,	0.05)	(925,	-0.2)
		(1100,	-0.05)
		(1250,	-0.05)

100 % Value must be in the range between 2.4 V and 3.6 V.

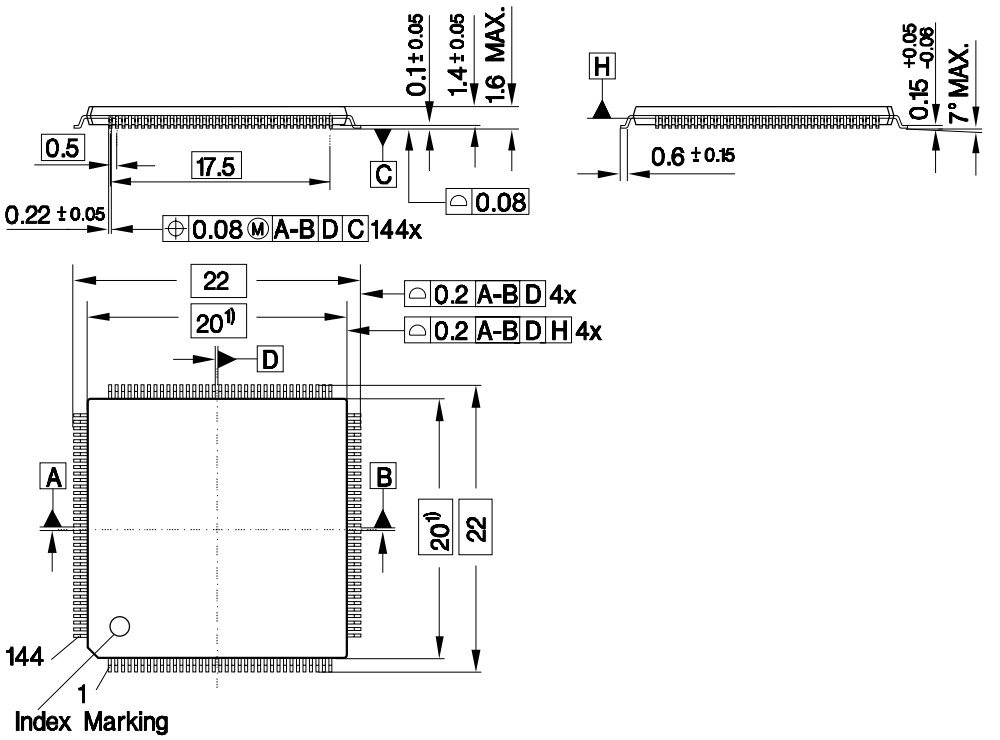
9.5 Capacitances

Parameter	Symbol	Limit Values		Unit	Pins
		typ.	max.		
Input capacitance[1)]	C_{IN}	5	10	pF	
Output capacitance[1)]	C_{OUT}	8	15	pF	all except XLx.y
Output capacitance[1)]	C_{OUT}	8	20	pF	XLx.y

1) Not tested in production.

10 Package Outlines

P-MQFP-144-8
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm

11 Glossary

ADC	Analog to digital converter
AIS	Alarm indication signal (blue alarm)
AGC	Automatic gain control
ALOS	Analog loss of signal
AMI	Alternate mark inversion
ANSI	American National Standards Institute
ATM	Asynchronous transfer mode
AUXP	Auxiliary pattern
B8ZS	Line coding to avoid too long strings of consecutive ’0’
BER	Bit error rate
BFA	Basic frame alignment
BOM	Bit orientated message
Bellcore	Bell Communications Research
BPV	Bipolar violation
CAS	Channel associated signaling
CAS-BR	Channel associated signaling - bit robbing
CAS-CC	Channel associated signaling - common channel
CCS	Common channel signaling
CRC4	Cyclic redundancy check
CSU	Channel service unit
CVC	Code violation counter
DCO	Digitally controlled oscillator
DL	Digital loop
DPLL	Digitally controlled phase locked loop

DS1	Digital signal level 1
ESD	Electrostatic discharge
ESF	Extended superframe (F24) format
EQ	Equalizer
ETSI	Eurpean Telecommunication Standards Institute
FALC®	Framing and line interface component
FAS	Frame alignment sequence
FCC	US Federal Communication Commission
FCS	Frame check sequence
FISU	Fill in signaling unit
FPS	Framing pattern sequence
HBM	Human body model for ESD classification
HDB3	High density bipolar of order 3
HDLC	High level data link control
IBL	In band loop (=LLB)
ISDN	Intergrated sevices digital network
ITU	International Telecommunications Group
JATT	Jitter attenuator
JTAG	Joined Test Action Group
LBO	Line build out
LCV	Line code violation
LIU	Line interface unit
LFA	Loss of frame alignment
LL	Local loop
LLB	Line loop back (= IBL)
LOS	Loss of signal (red alarm)

LSB	Least significant bit
LSSU	Link status signaling unit
MF	Multiframe
MSB	Most significant bit
MSU	Message signaling unit
NRZ	Non return to zero signal
PDV	Pulse density violation
PLB	Payload loop back
PLL	Phase locked loop
PMQFP	Plastic metric quad flat pack (device package)
PPR	Periodical performance report
PRBS	Pseudo ramdom binary sequence
PTQFP	Plastic thin metric quad flat pack (device package)
RAI	Remote alarm indication (yellow alarm)
RL	Remote loop
SF	Superframe
Sidactor	Overvoltage protection device for transmission lines
TAP	Test access port
UI	Unit interval

12 Appendix

12.1 Protection Circuitry

The design in figure 98 is a suggestion how to build up a generic E1/T1 platform. With the selection of the appropriate components the same circuitry is also able to handle the return loss and impedance to ground requirements of ETSI. For more details of this circuits, please refer to the appropriate application notes listed on the following page.

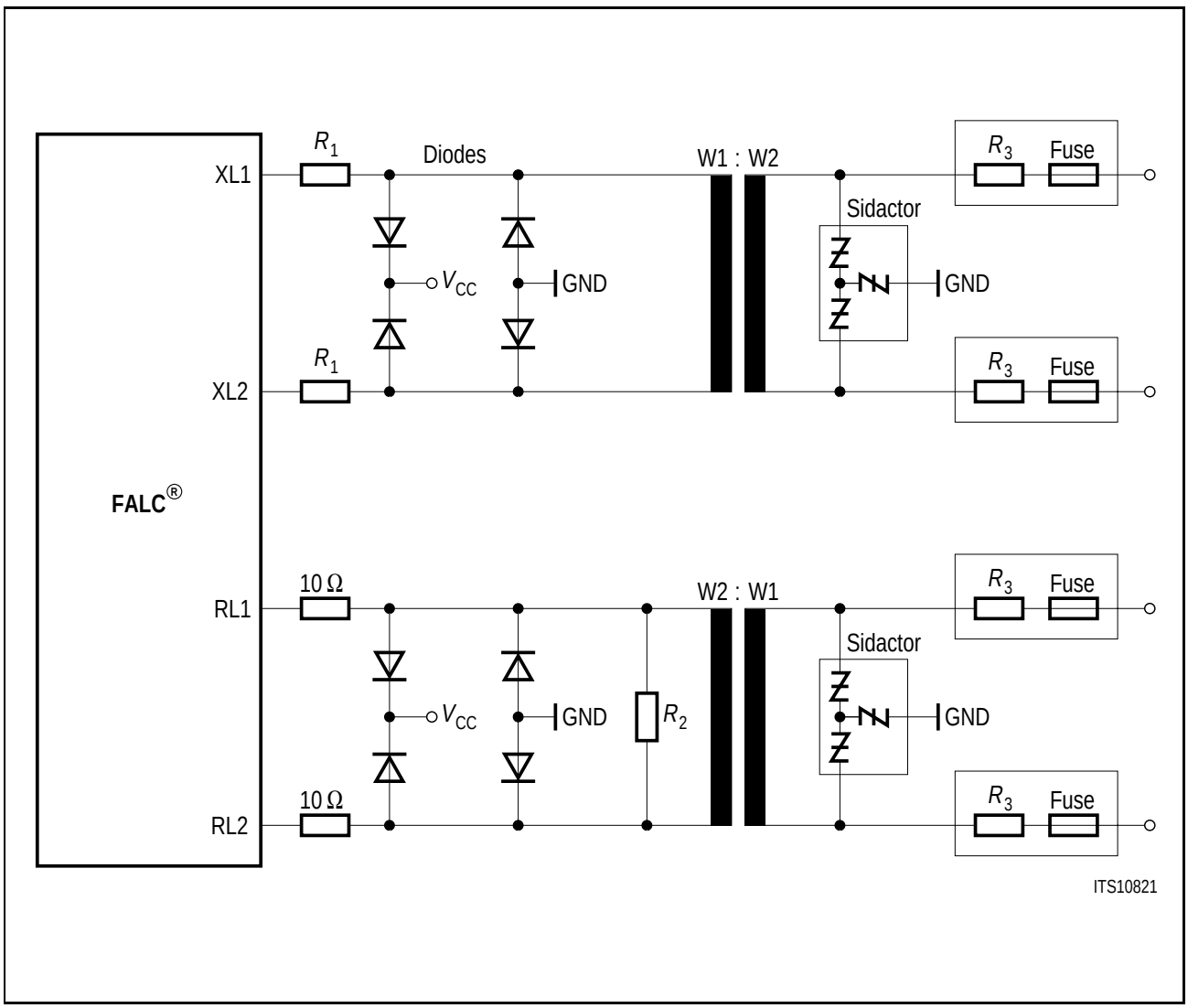


Figure 98
Protection Circuitry

12.2 Application Notes

The following application notes and technical documentation provide additional information:

- Transformer Recommendation
- Transmit Pulse Shape Programming
- Frequently Asked Questions
- Designing a Generic E1/T1 Platform for Short Haul and Long Haul Applications
- Different Hints to pass ETS300 011
- Key Features and Applications

12.3 Software Support

The following software package is provided together with the FALC Evaluation System EASY22554:

- Application Wizard
- E1 driver functions supporting different ETSI requirements including HDLC signaling
- LAPD Signaling Software
- FDL Signaling Software
- Boundary Scan File
- IBIS Model