288Mbit RDRAM®(E-die)

512K x 18bit x 32s banks

Direct RDRAM™

Version 1.4

Dec. 2003

Change History

Version 1.4(Dec. 2003)
- First Copy (Version 1.4x is named to unify the version of component and device operation datasheets) *- Based on the 256/288Mb D-die Version 1.4*

Overview

The RDRAM® device is a general purpose high-performance memory device suitable for use in a broad range of applications including computer memory, graphics, video, and any other application where high bandwidth and low latency are required.

The 288Mbit RDRAM devices are extremely high-speed CMOS DRAMs organized as 16M words by 18 bits. The use of Rambus Signaling Level (RSL) technology permits up to 1200 MHz transfer rates while using conventional system and board design technologies. RDRAM devices are capable of sustained data transfers up to 0.883ns per two bytes (6.7ns per sixteen bytes).

The architecture of RDRAM devices allows the highest sustained bandwidth for multiple, simultaneous randomly addressed memory transactions. The separate control and data buses with independent row and column control yield over 95% bus efficiency. The RDRAM device's 32 banks support up to four simultaneous transactions.

System oriented features for mobile, graphics and large memory systems include power management, byte masking, and x18 organization. The two data bits in the x18 organization are general and can be used for additional storage and bandwidth or for error correction.

Features

- Highest sustained bandwidth per DRAM device
  - 2.4GB/s sustained data transfer rate
  - Separate control and data buses for maximized efficiency
  - Separate row and column control buses for easy scheduling and highest performance
  - 32 banks: four transactions can take place simultaneously at full bandwidth data rates
- Low latency features
  - Write buffer to reduce read latency
  - 3 precharge mechanisms for controller flexibility
  - Interleaved transactions
- Advanced power management:
  - Multiple low power states allows flexibility in power consumption versus time to transition to active state
  - Power-down self-refresh
- Organization: 2kbyte pages and 32 banks, x 18
  - x18 organization allows ECC configurations or increased storage/bandwidth
- Uses Rambus Signaling Level (RSL) for up to 1200MHz operation

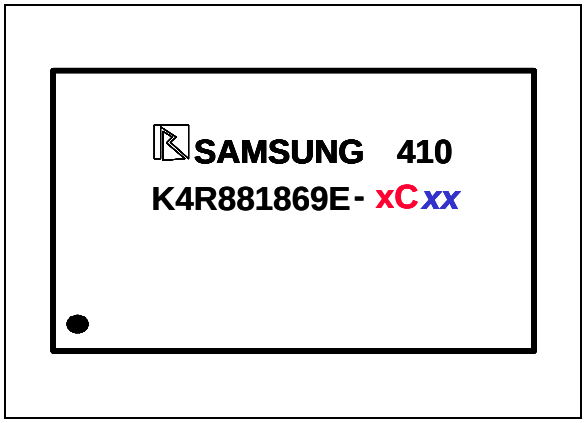


Figure 1: Direct RDRAM CSP Package

The 288Mbit RDRAM devices are offered in a CSP horizontal package suitable for desktop as well as low-profile add-in card and mobile applications.

Key Timing Parameters/Part Numbers

Organization	Speed			Part Number
	Bin	I/O Freq. MHz	t_{RAC} (Row Access Time) ns	
512Kx18x32s[a]	-CN1	1200	32	K4R881869E-G[b]C[c]N1
	-CT9	1066	32P	K4R881869E-GCT9
	-CM8	800	40	K4R881869E-GCM8
	-CK8	800	45	K4R881869E-GCK8
512Kx18x32s	-CN1	1200	32	K4R881869E-FCN1
	-CT9	1066	32P	K4R881869E-FCT9
	-CM8	800	40	K4R881869E-FCM8
	-CK8	800	45	K4R881869E-FCK8

a."32s" - 32 banks which use a "split" bank architecture.

b."G" - WBGA lead-free package , "F" - WBGA package

c."C" - RDRAM core uses normal power self refresh.

Pinouts and Definitions

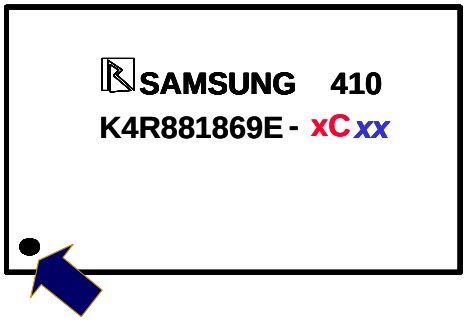
Center-Bonded Devices

These tables shows the pin assignments of the center-bonded RDRAM package. The mechanical dimensions of this package are shown in a later section. Refer to Section "Center-Bonded WBGA Package" on page 18. Note - pin #1 is at the A1 position.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	S	T	U
10		V_{DD}	GND		V_{DD}	GND	V_{DD}					V_{DD}	V_{DD}	V_{DD}		GND	V_{DD}	
9																		
8	GND	V_{DD}	CMD	V_{DD}	GND	GNDa	GNDa	V_{DD}	V_{DD}	GND	GND	V_{DD}	V_{DD}	GND	GND	V_{CMOS}	V_{DD}	GND
7	V_{DD}	DQA8	DQA7	DQA5	DQA3	DQA1	CTMN	CTM	RQ7	RQ5	RQ3	RQ1	DQB1	DQB3	DQB5	DQB7	DQB8	V_{DD}
6																		
5																		
4	GND	GND	DQA6	DQA4	DQA2	DQA0	CFM	CFMN	RQ6	RQ4	RQ2	RQ0	DQB0	DQB2	DQB4	DQB6	GND	GND
3	V_{DD}	GND	SCK	V_{CMOS}	GND	V_{DD}	GND	V_{DDa}	V_{REF}	GND	V_{DD}	GND	GND	V_{DD}	SIO0	SIO1	GND	V_{DD}
2																		
1		V_{DD}	GND		GND	V_{DD}	GND					GND	GND	GND		GND	V_{DD}	

ROW

COL



The pin #1(ROW 1, COL A) is located at the A1 position on the top side and the A1 position is marked by the marker "● ".

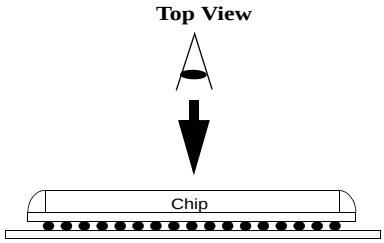


Table 1: Pin Description

Signal	I/O	Type	# Pins center	Description
SIO1,SIO0	I/O	CMOS[a]	2	Serial input/output. Pins for reading from and writing to the control registers using a serial access protocol. Also used for power management.
CMD	I	CMOS[a]	1	Command input. Pins used in conjunction with SIO0 and SIO1 for reading from and writing to the control registers. Also used for power management.
SCK	I	CMOS[a]	1	Serial clock input. Clock source used for reading from and writing to the control registers
V_{DD}			24	Supply voltage for the RDRAM core and interface logic.
V_{DDa}			1	Supply voltage for the RDRAM analog circuitry.
V_{CMOS}			2	Supply voltage for CMOS input/output pins.
GND			28	Ground reference for RDRAM core and interface.
GNDa			2	Ground reference for RDRAM analog circuitry.
DQA8..DQA0	I/O	RSL[b]	9	Data byte A. Nine pins which carry a byte of read or write data between the Channel and the RDRAM device. DQA8 is not used (no connection) by RDRAM device with a x16 organization.
CFM	I	RSL[b]	1	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
CFMN	I	RSL[b]	1	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity
V_{REF}			1	Logic threshold reference voltage for RSL signals
CTMN	I	RSL[b]	1	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
CTM	I	RSL[b]	1	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
RQ7..RQ5 or ROW2..ROW0	I	RSL[b]	3	Row access control. Three pins containing control and address information for row accesses.
RQ4..RQ0 or COL4..COL0	I	RSL[b]	5	Column access control. Five pins containing control and address information for column accesses.
DQB8.. DQB0	I/O	RSL[b]	9	Data byte B. Nine pins which carry a byte of read or write data between the Channel and the RDRAM device. DQB8 is not used (no connection) by RDRAM device with a x16 organization.
Total pin count per package			92	

a. All CMOS signals are high-true; a high voltage is a logic one and a low voltage is logic zero.
b. All RSL signals are low-true; a low voltage is a logic one and a high voltage is logic zero.

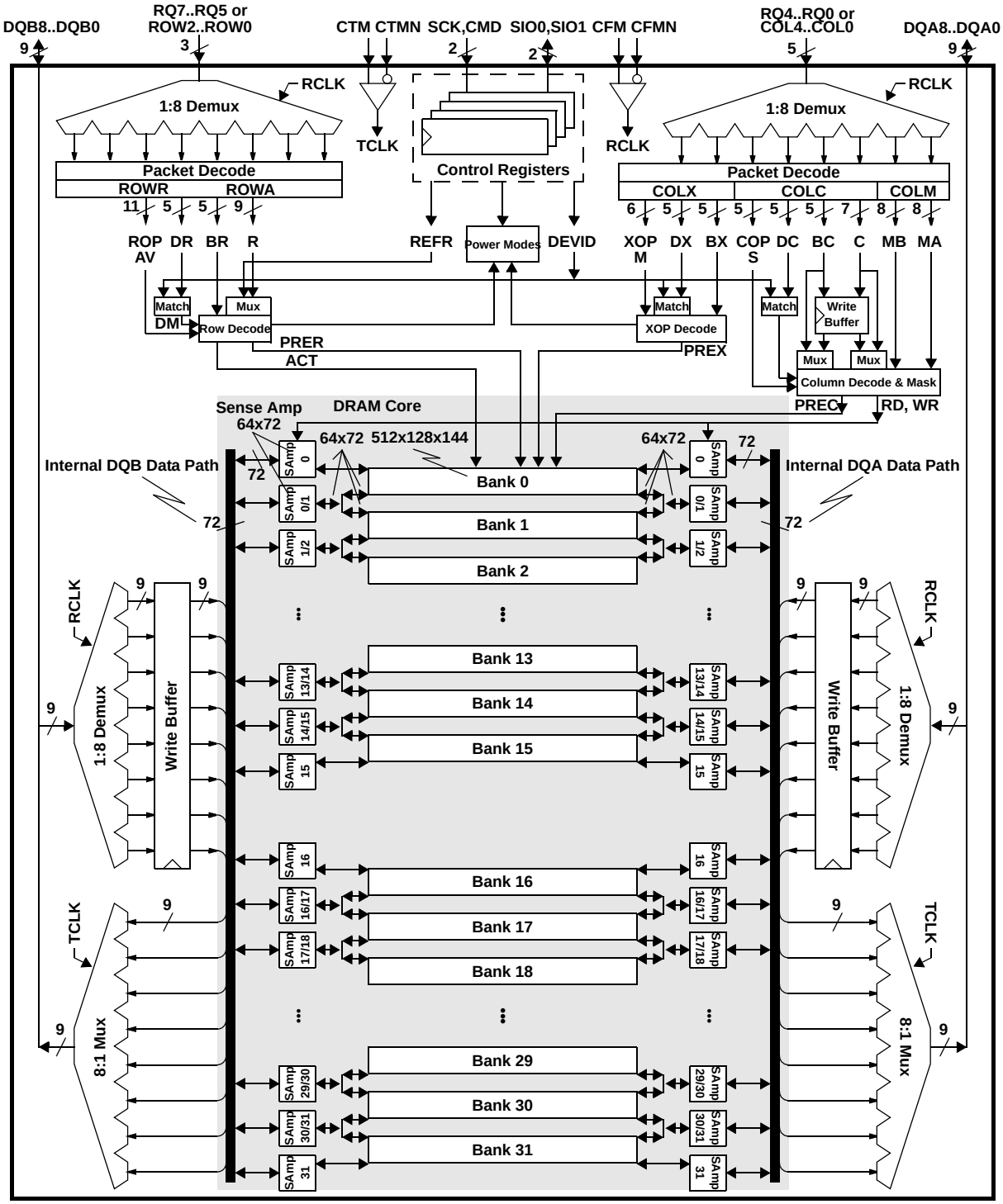


Figure 2: 288Mbit (512Kx18x32s) RDRAM Device Block Diagram

General Description

Figure 2 is a block diagram of the 288Mbit RDRAM device. It consists of two major blocks: a "core" block built from banks and sense amps similar to those found in other types of DRAM, and a Direct Rambus™ interface block which permits an external controller to access this core at up to 2.4GB/s.

Control Registers: The CMD, SCK, SIO0, and SIO1 pins appear in the upper center of Figure 2. They are used to write and read a block of control registers. These registers supply the RDRAM configuration information to a controller and they select the operating modes of the device. The REFR value is used for tracking the last refreshed row. Most importantly, the five bit DEVID specifies the device address of the RDRAM device on the Channel.

Clocking: The CTM and CTMN pins (Clock-To-Master) generate TCLK (Transmit Clock), the internal clock used to transmit read data. The CFM and CFMN pins (Clock-From-Master) generate RCLK (Receive Clock), the internal clock signal used to receive write data and to receive the ROW and COL pins.

DQA,DQB Pins: These 18 pins carry read (Q) and write (D) data across the Channel. They are multiplexed/de-multiplexed from/to two 72bit data paths (running at one-eighth the data frequency) inside the RDRAM device.

Banks: The 32Mbyte core of the RDRAM device is divided into thirty two 1Mbyte banks, each organized as 512 rows, with each row containing 128 dualocts, and each dualoct containing 18 bytes. A dualoct is the smallest unit of data that can be addressed.

Sense Amps: The RDRAM device contains 34 sense amps. Each sense amp consists of 1kbyte of fast storage (512 bytes for DQA and 512 bytes for DQB) and can hold one-half of one row of one bank of the RDRAM device. The sense amp may hold any of the 1024 half-rows of an associated bank. However, each sense amp is shared between two adjacent banks of the RDRAM device (except for sense amps 0, 15, 16, and 31). This introduces the restriction that adjacent banks may not be simultaneously accessed.

RQ Pins: These pins carry control and address information. They are broken into two groups. RQ7..RQ5 are also called ROW2..ROW0, and are used primarily for controlling row accesses. RQ4..RQ0 are also called COL4..COL0, and are used primarily for controlling column accesses.

ROW Pins: The principle use of these three pins is to manage the transfer of data between the banks and the sense amps of the RDRAM device. These pins are de-multiplexed into a 24-bit ROWA (row-activate) or ROWR (row-operation) packet.

COL Pins: The principle use of these five pins is to manage the transfer of data between the DQA/DQB pins and the sense amps of the RDRAM device. These pins are de-multiplexed into a 23-bit COLC (column-operation) packet and either a 17-bit COLM (mask) packet or a 17-bit COLX (extended-operation) packet.

ACT Command: An ACT (activate) command from an ROWA packet causes one of the 512 rows of the selected bank to be loaded to its associated sense amps (two 512 bytes sense amps for DQA and two for DQB).

PRER Command: A PRER (precharge) command from an ROWR packet causes the selected bank to release its two associated sense amps, permitting a different row in that bank to be activated, or permitting adjacent banks to be activated.

RD Command: The RD (read) command causes one of the 128 dualocts of one of the sense amps to be transmitted on the DQA/DQB pins of the Channel.

WR Command: The WR (write) command causes a dualoct received from the DQA/DQB data pins of the Channel to be loaded into the write buffer. There is also space in the write buffer for the BC bank address and C column address information. The data in the write buffer is automatically retired (written with optional bytemask) to one of the 128 dualocts of one of the sense amps during a subsequent COP command. A retire can take place during a RD, WR, or NOCOP to another device, or during a WR or NOCOP to the same device. The write buffer will not retire during a RD to the same device. The write buffer reduces the delay needed for the internal DQA/DQB data path turnaround.

PREC Precharge: The PREC, RDA and WRA commands are similar to NOCOP, RD and WR, except that a precharge operation is performed at the end of the column operation. These commands provide a second mechanism for performing precharge.

PREX Precharge: After a RD command, or after a WR command with no byte masking (M=0), a COLX packet may be used to specify an extended operation (XOP). The most important XOP command is PREX. This command provides a third mechanism for performing precharge.

Packet Format

Figure 3 shows the formats of the ROWA and ROWR packets on the ROW pins. Table 3 describes the fields which comprise these packets. DR4T and DR4F bits are encoded to contain both the DR4 device address bit and a framing bit which allows the ROWA or ROWR packet to be recognized by the RDRAM device.

The AV (ROWA/ROWR packet selection) bit distinguishes between the two packet types. Both the ROWA and ROWR packet provide a five bit device address and a five bit bank address. An ROWA packet uses the remaining bits to specify a nine bit row address, and the ROWR packet uses the remaining bits for an eleven bit opcode field. Note the use of the "RsvX" notation to reserve bits for future address field extension.

Table 3: Field Description for ROWA Packet and ROWR Packet

Field	Description
DR4T,DR4F	Bits for framing (recognizing) a ROWA or ROWR packet. Also encodes highest device address bit.
DR3..DR0	Device address for ROWA or ROWR packet.
BR4..BR0	Bank address for ROWA or ROWR packet. RsvB denotes bits ignored by the RDRAM device.
AV	Selects between ROWA packet (AV=1) and ROWR packet (AV=0).
R8..R0	Row address for ROWA packet. RsvR denotes bits ignored by the RDRAM device.
ROP10..ROP0	Opcode field for ROWR packet. Specifies precharge, refresh, and power management functions.

Figure 3 also shows the formats of the COLC, COLM, and COLX packets on the COL pins. Table 4 describes the fields which comprise these packets.

The COLC packet uses the S (Start) bit for framing. A COLM or COLX packet is aligned with this COLC packet, and is also framed by the S bit.

The 23 bit COLC packet has a five bit device address, a five bit bank address, a seven bit column address, and a four bit opcode. The COLC packet specifies a read or write command, as well as some power management commands.

The remaining 17 bits are interpreted as a COLM (M=1) or COLX (M=0) packet. A COLM packet is used for a COLC write command which needs bytemask control. The COLM packet is associated with the COLC packet from at least t_{RTR} earlier. A COLX packet may be used to specify an independent precharge command. It contains a five bit device address, a five bit bank address, and a five bit opcode. The COLX packet may also be used to specify some housekeeping and power management commands. The COLX packet is framed within a COLC packet but is not otherwise associated with any other packet.

Table 4: Field Description for COLC Packet, COLM Packet, and COLX Packet

Field	Description
S	Bit for framing (recognizing) a COLC packet, and indirectly for framing COLM and COLX packets.
DC4..DC0	Device address for COLC packet.
BC4..BC0	Bank address for COLC packet. RsvB denotes bits reserved for future extension (controller drives 0 ' s).
C6..C0	Column address for COLC packet. RsvC denotes bits ignored by the RDRAM device.
COP3..COP0	Opcode field for COLC packet. Specifies read, write, precharge, and power management functions.
M	Selects between COLM packet (M=1) and COLX packet (M=0).
MA7..MA0	Bytemask write control bits. 1=write, 0=no-write. MA0 controls the earliest byte on DQA8..0.
MB7..MB0	Bytemask write control bits. 1=write, 0=no-write. MB0 controls the earliest byte on DQB8..0.
DX4..DX0	Device address for COLX packet.
BX4..BX0	Bank address for COLX packet. RsvB denotes bits reserved for future extension (controller drives 0' s).
XOP4..XOP0	Opcode field for COLX packet. Specifies precharge, I_{OL} control, and power management functions.

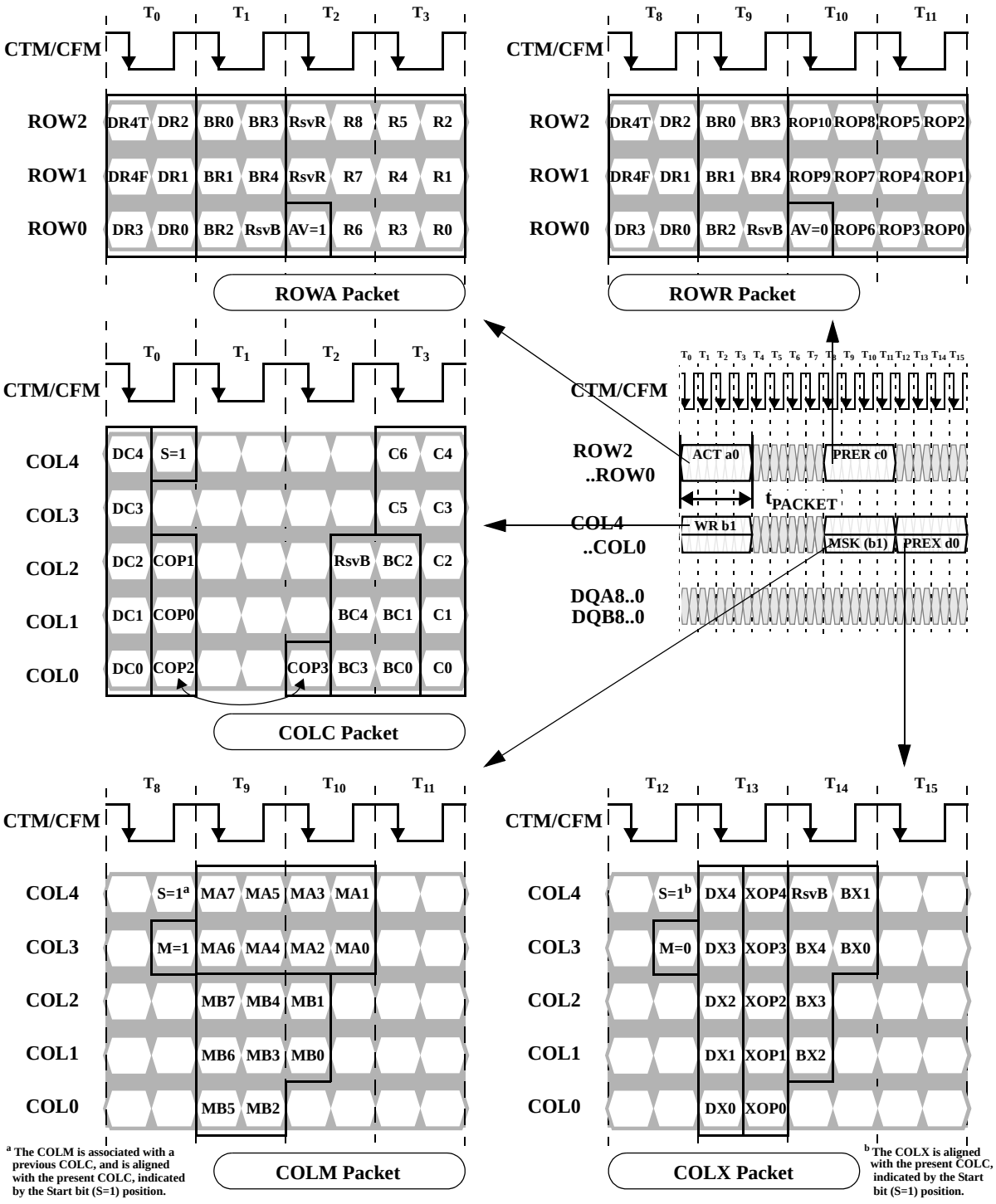


Figure 3: Packet Formats

Field Encoding Summary

Table 5 shows how the six device address bits are decoded for the ROWA and ROWR packets. The DR4T and DR4F encoding merges a fifth device bit with a framing bit. When neither bit is asserted, the device is not selected. Note that a broadcast operation is indicated when both bits are set. Broadcast operation would typically be used for refresh and power management commands. If the device is selected, the DM (DeviceMatch) signal is asserted and an ACT or ROP command is performed.

Table 5: Device Field Encodings for ROWA Packet and ROWR Packet

DR4T	DR4F	Device Selection	Device Match signal (DM)
1	1	All devices (broadcast)	DM is set to 1
0	1	One device selected	DM is set to 1 if {DEVID4..DEVID0} == {0,DR3..DR0} else DM is set to 0
1	0	One device selected	DM is set to 1 if {DEVID4..DEVID0} == {1,DR3..DR0} else DM is set to 0
0	0	No packet present	DM is set to 0

Table 6 shows the encodings of the remaining fields of the ROWA and ROWR packets. An ROWA packet is specified by asserting the AV bit. This causes the specified row of the specified bank of this device to be loaded into the associated sense amps.

An ROWR packet is specified when AV is not asserted. An 11 bit opcode field encodes a command for one of the banks of this device. The PRER command causes a bank and its two associated sense amps to precharge, so another row or an adjacent bank may be activated. The REFA (refresh-activate) command is similar to the ACT command, except the row address comes from an internal register REFR, and REFR is incremented at the largest bank address. The REFP (refresh-precharge) command is identical to a PRER command.

The NAPR, NAPRC, PDNR, ATTN, and RLXR commands are used for managing the power dissipation of the RDRAM device and are described in more detail in “Power State Management” on page 50. The TCEN and TCAL commands are used to adjust the output driver slew rate and they are described in more detail in “Current and Temperature Control” on page 56.

Table 6: ROWA Packet and ROWR Packet Field Encodings

DM[a]	AV	ROP10..ROP0 Field									Name	Command Description
		10	9	8	7	6	5	4	3	2:0		
0	-	-	-	-	-	-	-	-	-	---	-	No operation.
1	1	Row address									ACT	Activate row R8..R0 of bank BR4..BR0 of device and move device to ATTN[b].
1	0	1	1	0	0	0	x[c]	x	x	000	PRER	Precharge bank BR4..BR0 of this device.
1	0	0	0	0	1	1	0	0	x	000	REFA	Refresh (activate) row REFR8..REFR0 of bank BR4..BR0 of device. Increment REFR if BR4..BR0 = 11111 (see Figure 52).
1	0	1	0	1	0	1	0	0	x	000	REFP	Precharge bank BR4..BR0 of this device after REFA (see Figure 52).
1	0	x	x	0	0	0	0	1	x	000	PDNR	Move this device into the powerdown (PDN) power state (see Figure 49).
1	0	x	x	0	0	0	1	0	x	000	NAPR	Move this device into the nap (NAP) power state (see Figure 49).
1	0	x	x	0	0	0	1	1	x	000	NAPRC	Move this device into the nap (NAP) power state conditionally
1	0	x	x	x	x	x	x	x	0	000	ATTN[b]	Move this device into the attention (ATTN) power state (see Figure 47).
1	0	x	x	x	x	x	x	x	1	000	RLXR	Move this device into the standby (STBY) power state (see Figure 48).
1	0	0	0	0	0	0	0	0	x	001	TCAL	Temperature calibrate this device (see Figure 55).
1	0	0	0	0	0	0	0	0	x	010	TCEN	Temperature calibrate/enable this device (see Figure 55).
1	0	0	0	0	0	0	0	0	0	000	NOROP	No operation.

a. The DM (Device Match signal) value is determined by the DR4T,DR4F, DR3..DR0 field of the ROWA and ROWR packets. See Table 5.
b. The ATTN command does not cause a RLX-to-ATTN transition for a broadcast operation (DR4T/DR4F=1/1).
c. An “x” entry indicates which commands may be combined. For instance, the three commands PRER/NAPRC/RLXR may be specified in one ROP value (011000111000).

Table 7 shows the COP field encoding. The device must be in the ATTN power state in order to receive COLC packets. The COLC packet is used primarily to specify RD (read) and WR (write) commands. Retire operations (moving data from the write buffer to a sense amp) happen automatically. See Figure 18 for a more detailed description.

The COLC packet can also specify a PREC command, which precharges a bank and its associated sense amps. The RDA/WRA commands are equivalent to combining RD/WR with a PREC. RLXC (relax) performs a power mode transition. See “Power State Management” on page 50.

Table 7: COLC Packet Field Encodings

S	DC4.. DC0 (select device)[a]	COP3..0	Name	Command Description
0	----	-----	-	No operation.
1	/= (DEVID4 ..0)	-----	-	Retire write buffer of this device.
1	== (DEVID4 ..0)	x000[b]	NOCOP	Retire write buffer of this device.
1	== (DEVID4 ..0)	x001	WR	Retire write buffer of this device, then write column C6..C0 of bank BC4..BC0 to write buffer.
1	== (DEVID4 ..0)	x010	RSRV	Reserved, no operation.
1	== (DEVID4 ..0)	x011	RD	Read column C6..C0 of bank BC4..BC0 of this device.
1	== (DEVID4 ..0)	x100	PREC	Retire write buffer of this device, then precharge bank BC4..BC0 (see Figure 15).
1	== (DEVID4 ..0)	x101	WRA	Same as WR, but precharge bank BC4..BC0 after write buffer (with new data) is retired.
1	== (DEVID4 ..0)	x110	RSRV	Reserved, no operation.
1	== (DEVID4 ..0)	x111	RDA	Same as RD, but precharge bank BC4..BC0 afterward.
1	== (DEVID4 ..0)	1xxx	RLXC	Move this device into the standby (STBY) power state (see Figure 48).

a. “/=” means not equal, “==” means equal.
b. An “x” entry indicates which commands may be combined. For instance, the two commands WR/RLXC may be specified in one COP value (1001).

Table 8 shows the COLM and COLX field encodings. The M bit is asserted to specify a COLM packet with two 8 bit bytemask fields MA and MB. If the M bit is not asserted, an COLX is specified. It has device and bank address fields, and an opcode field. The primary use of the COLX packet is to permit an independent PREX (precharge) command to be specified without consuming control bandwidth on the ROW pins. It is also used for the CAL(calibrate) and SAM (sample) current control commands (see “Current and Temperature Control” on page 56), and for the RLXX power mode command (see “Power State Management” on page 50).

Table 8: COLM Packet and COLX Packet Field Encodings

M	DX4 .. DX0 (selects device)	XOP4..0	Name	Command Description
1	----	-	MSK	MB/MA bytemasks used by WR/WRA.
0	/= (DEVID4 ..0)	-	-	No operation.
0	== (DEVID4 ..0)	00000	NOXOP	No operation.
0	== (DEVID4 ..0)	1xxx0[a]	PREX	Precharge bank BX3..BX0 of this device (see Figure 15).
0	== (DEVID4 ..0)	x10x0	CAL	Calibrate (drive) I_{OL} current for this device (see Figure 54).
0	== (DEVID4 ..0)	x11x0	CAL/SAM	Calibrate (drive) and Sample (update) I_{OL} current for this device (see Figure 54).
0	== (DEVID4 ..0)	xxx10	RLXX	Move this device into the standby (STBY) power state (see Figure 48).
0	== (DEVID4 ..0)	xxxx1	RSRV	Reserved, no operation.

a. An “x” entry indicates which commands may be combined. For instance, the two commands PREX/RLXX may be specified in one XOP value (10010).

Electrical Conditions

Table 9: Electrical Conditions

Symbol	Parameter and Conditions	Min	Max	Unit
T_J	Junction temperature under bias	-	100	°C
V_{DD}, V_{DDA}	Supply voltage	2.50 - 0.13	2.50 + 0.13	V
$V_{DD,N}$, $V_{DDA,N}$	Supply voltage droop (DC) during NAP interval (t_{NLIMIT})	-	2.0	%
$v_{DD,N}$, $v_{DDA,N}$	Supply voltage ripple (AC) during NAP interval (t_{NLIMIT})	-2.0	2.0	%
V_{CMOS}[a]	Supply voltage for CMOS pins (2.5V controllers) Supply voltage for CMOS pins (1.8V controllers)	V_{DD} 1.80 - 0.1	V_{DD} 1.80 + 0.2	V V
V_{REF}	Reference voltage	1.40 - 0.2	1.40 + 0.2	V
V_{DIL}	RSL data input - low voltage @ t_{CYCLE}=1.667ns	V_{REF} - 0.5	V_{REF} - 0.15	V
	RSL data input - low voltage @ t_{CYCLE}=1.875ns	V_{REF} - 0.5	V_{REF} - 0.15	
	RSL data input - low voltage @ t_{CYCLE}=2.50ns	V_{REF} - 0.5	V_{REF} - 0.2	
V_{DIH}	RSL data input - high voltage[b] @ t_{CYCLE}=1.667ns	V_{REF} + 0.15	V_{REF} + 0.5	V
	RSL data input - high voltage[b] @ t_{CYCLE}=1.875ns	V_{REF} + 0.15	V_{REF} + 0.5	
	RSL data input - high voltage[b] @ t_{CYCLE}=2.50ns	V_{REF} + 0.2	V_{REF} + 0.5	
R_{DA}	RSL data asymmetry : R_{DA} = (V_{DIH} - V_{REF}) / (V_{REF} - V_{DIL})	0.67	1.00	-
V_{CM}	RSL clock input - common mode V_{CM} = (V_{CIH}+V_{CIL})/2	1.3	1.8	V
$V_{CIS,CTM}$	RSL clock input swing: V_{CIS} = V_{CIH} - V_{CIL} (CTM,CTMN pins).	0.35	1.00	V
$V_{CIS,CFM}$	RSL clock input swing: V_{CIS} = V_{CIH} - V_{CIL} (CFM,CFMN pins).	0.225	1.00	V
$V_{IL,CMOS}$	CMOS input low voltage	- 0.3[c]	V_{CMOS}/2 - 0.25	V
$V_{IH,CMOS}$	CMOS input high voltage	V_{CMOS}/2 + 0.25	V_{CMOS}+0.3[d]	V

a. V_{CMOS} must remain on as long as V_{DD} is applied and cannot be turned off.
b. V_{DIH} is typically equal to V_{TERM} (1.8V±0.1V) under DC conditions in a system.
c. Voltage undershoot is limited to -0.7V for a duration of less than 5ns.
d. Voltage overshoot is limited toV_{CMOS} +0.7V for a duration of less than 5ns

Electrical Characteristics

Table 10: Electrical Characteristics

Symbol	Parameter and Conditions	Min	Max	Unit
Θ_{JC}	Junction-to-Case thermal resistance	-	0.5	°C/Watt
I_{REF}	V_{REF} current @ $V_{REF,MAX}$	-10	10	µA
I_{OH}	RSL output high current @ ($0 \le V_{OUT} \le V_{DD}$)	-10	10	µA
I_{ALL}	RSL I_{OL} current @ t_{CYCLE}= 1.667ns V_{OL} = 0.9V, $V_{DD,MIN}$, $T_{J,MAX}$[a]	32.0	90.0	mA
	RSL I_{OL} current @ t_{CYCLE}= 1.875ns V_{OL} = 0.9V, $V_{DD,MIN}$, $T_{J,MAX}$[a]	32.0	90.0	
	RSL I_{OL} current @ t_{CYCLE}=2.50ns V_{OL} = 0.9V, $V_{DD,MIN}$, $T_{J,MAX}$[a]	30.0	90.0	
ΔI_{OL}	RSL I_{OL} current resolution step	-	1.5	mA
r_{OUT}	Dynamic output impedance @ V_{OL}= 0.9V	150	-	Ω
$I_{OL,NOM}$	RSL I_{OL} current @ V_{OL} = 1.0V [b,c]@ t_{CYCLE}=1.667ns	27.1	30.1	mA
	RSL I_{OL} current @ V_{OL} = 1.0V [b,c]@ t_{CYCLE}=1.875ns	27.1	30.1	
	RSL I_{OL} current @ V_{OL} = 1.0V [b,c]@ t_{CYCLE}=2.5ns	26.6	30.6	
$I_{I,CMOS}$	CMOS input leakage current @ ($0 \le V_{I,CMOS} \le V_{CMOS}$)	-10.0	10.0	µA
$V_{OL,CMOS}$	CMOS output voltage @ $I_{OL,CMOS}$= 1.0mA	-	0.3	V
$V_{OH,CMOS}$	CMOS output high voltage @ $I_{OH,CMOS}$= -0.25mA	V_{CMOS}-0.3	-	V

a. This measurement is made in manual current control mode; i.e. with all output device legs sinking current.
b. This measurement is made in automatic current control mode after at least 64 current control calibration operations to a device and after CCA and CCB are initialized to a value of 64. This value applies to all DQA and DQB pins.
c. This measurement is made in automatic current control mode in a 25Ω test system with V_{TERM}= 1.714V and V_{REF}= 1.357V and with the ASYMA and ASYMB register fields set to 0.

Timing Conditions

Table 11: Timing Conditions

Symbol	Parameter	Min	Max	Unit	Figure(s)
t_{CYCLE}	CTM and CFM cycle times (-1200)	1.667	2.5	ns	Figure 56
	CTM and CFM cycle times (-1066)	1.875	2.5		
	CTM and CFM cycle times (-800)	2.50	3.33		
t_{CR}, t_{CF}	CTM and CFM input rise and fall times. Use the minimum value of these parameters during testing. (-1200)	0.2	0.45	ns	Figure 56
	CTM and CFM input rise and fall times. Use the minimum value of these parameters during testing. (-1066,-800)	0.2	0.5		
t_{CH}, t_{CL}	CTM and CFM high and low times	40%	60%	t_{CYCLE}	Figure 56
t_{TR}	CTM-CFM differential (MSE/MS=0/0) CTM-CFM differential (MSE/MS=1/1)[a] CTM-CFM differential for 1.875ns and 1.667ns (MSE/MS=1/0)	0.0 0.9 -0.1	1.0 1.0 0.1	t_{CYCLE}	Figure 43 Figure 56
t_{DCW}	Domain crossing window	-0.1	0.1	t_{CYCLE}	Figure 62
t_{DR}, t_{DF}	DQA/DQB/ROW/COL input rise/fall times (20% to 80%). Use the minimum value of these parameters during testing.@ t_{CYCLE}=1.667ns	0.2	0.45	ns	Figure 57
	DQA/DQB/ROW/COL input rise/fall times (20% to 80%). Use the minimum value of these parameters during testing.@ t_{CYCLE}=1.875ns	0.2	0.45		
	DQA/DQB/ROW/COL input rise/fall times (20% to 80%). Use the minimum value of these parameters during testing.@ t_{CYCLE}=2.50ns	0.2	0.65		
t_S, t_H	DQA/DQB/ROW/COL-to-CFM set/hold @ t_{CYCLE}=1.667ns	0.140[b]	-	ns	Figure 57
	DQA/DQB/ROW/COL-to-CFM set/hold @ t_{CYCLE}=1.875ns	0.160[b,c]	-		
	DQA/DQB/ROW/COL-to-CFM set/hold @ t_{CYCLE}=2.50ns	0.200[b,d]	-		
t_{DR1}, t_{DF1}	SIO0, SIO1 input rise and fall times	-	5.0	ns	Figure 59
t_{DR2}, t_{DF2}	CMD, SCK input rise and fall times	-	2.0	ns	Figure 59
t_{CYCLE1}	SCK cycle time - Serial control register transactions	1000	-	ns	Figure 59
	SCK cycle time - Power transitions @ t_{CYCLE}=1.667ns	7.5	-		
	SCK cycle time - Power transitions @ t_{CYCLE}=1.875ns	7.5	-		
	SCK cycle time - Power transitions @ t_{CYCLE}=2.50ns	10	-		
t_{CH1}, t_{CL1}	SCK high and low times @ t_{CYCLE}=1.667ns	3.5	-	ns	Figure 59
	SCK high and low times @ t_{CYCLE}=1.875ns	3.5	-		
	SCK high and low times @ t_{CYCLE}=2.50ns	4.25	-		
t_{S1}	CMD setup time to SCK rising or falling edge[e]@ t_{CYCLE}=1.667ns	1.0	-	ns	Figure 59
	CMD setup time to SCK rising or falling edge[e] @ t_{CYCLE}=1.875ns	1.0	-		
	CMD setup time to SCK rising or falling edge[e] @ t_{CYCLE}=2.50ns	1.25	-		
t_{H1}	CMD hold time to SCK rising or falling edge[e]	1	-	ns	Figure 59

Table 11: Timing Conditions

Symbol	Parameter	Min	Max	Unit	Figure(s)
t_{S2}	SIO0 setup time to SCK falling edge	40	-	ns	Figure 59
t_{H2}	SIO0 hold time to SCK falling edge	40	-	ns	Figure 59
t_{S3}	PDEV setup time on DQA5..0 to SCK rising edge.	0	-	ns	Figure 50
t_{H3}	PDEV hold time on DQA5..0 to SCK rising edge.	5.5	-	ns	Figure 60
t_{S4}	ROW2..0, COL4..0 setup time for quiet window	-1	-	t_{CYCLE}	Figure 50
t_{H4}	ROW2..0, COL4..0 hold time for quiet window[f]	5	-	t_{CYCLE}	Figure 50
t_{NPQ}	Quiet on ROW/COL bits during NAP/PDN entry	4	-	t_{CYCLE}	Figure 49
$t_{READTOCC}$	Offset between read data and CC packets (same device)	12	-	t_{CYCLE}	Figure 54
$t_{CCSAMTOREAD}$	Offset between CC packet and read data (same device)	8	-	t_{CYCLE}	Figure 54
t_{CE}	CTM/CFM stable before NAP/PDN exit	2	-	t_{CYCLE}	Figure 50
t_{CD}	CTM/CFM stable after NAP/PDN entry	100	-	t_{CYCLE}	Figure 49
t_{FRM}	ROW packet to COL packet ATTN framing delay	7	-	t_{CYCLE}	Figure 48
t_{NLIMIT}	Maximum time in NAP mode		10.0	ms	Figure 47
t_{REF}	Refresh interval		32	ms	Figure 52
t_{BURST}	Interval after PDN or NAP (with self-refresh) exit in which all banks of the RDRAM device must be refreshed at least once.		200	ms	Figure 53
t_{CCTRL}	Current control interval	34 t_{CYCLE}	100ms	ms/t_{CYCLE}	Figure 54
t_{TEMP}	Temperature control interval		100	ms	Figure 55
t_{TCEN}	TCE command to TCAL command	150	-	t_{CYCLE}	Figure 55
t_{TCAL}	TCAL command to quiet window	2	2	t_{CYCLE}	Figure 55
$t_{TCQUIET}$	Quiet window (no read data)	140	-	t_{CYCLE}	Figure 55
t_{PAUSE}	RDRAM device delay (no RSL operations allowed)		200.0	ms	page 38

a. MSE/MS are fields of the SKIP register. For this combination (skip override) the tDCW parameter range is effectively 0.0 to 0.0.
b. $t_{S,MIN}$ and $t_{H,MIN}$ for other t_{CYCLE} values can be interpolated between or extrapolated from the timings at the 2 specified t_{CYCLE} values.
c. This parameter also applies to a-1200 part when operated with t_{CYCLE} = 1.875ns
d. This parameter also applies to a-1200 or -1066 part when operated with t_{CYCLE} = 2.50ns
e. With $V_{IL,CMOS}=0.5V_{CMOS}-0.4V$ and $V_{IH,CMOS}=0.5V_{CMOS}+0.4V$
f. Effective hold becomes $t_{H4}'=t_{H4}+[PDNXA•64•t_{SCYCLE}+t_{PDNXB,MAX}]-[PDNX•256•t_{SCYCLE}]$ if $[PDNX•256•t_{SCYCLE}] < [PDNXA•64•t_{SCYCLE}+t_{PDNXB,MAX}]$. See Figure 50

Timing Characteristics

Table 12: Timing Characteristics

Symbol	Parameter	Min	Max	Unit	Figure(s)
t_Q	CTM-to-DQA/DQB output time @ t_{CYCLE}=1.667ns	-0.170[a]	+0.170[a]	ns	Figure 58
	CTM-to-DQA/DQB output time @ t_{CYCLE}=1.875ns	-0.195[a,b]	+0.195[a,b]		
	CTM-to-DQA/DQB output time @ t_{CYCLE}=2.5ns	-0.260[a,c]	+0.260[a,c]		
t_{QR}, t_{QF}	DQA/DQB output rise and fall times @ t_{CYCLE}=1.667ns	0.2	0.32	ns	Figure 58
	DQA/DQB output rise and fall times @ t_{CYCLE}=1.875ns	0.2	0.32		
	DQA/DQB output rise and fall times @ t_{CYCLE}=2.5ns	0.2	0.45		
t_{Q1}	SCK(neg)-to-SIO0 delay @ $C_{LOAD,MAX}$ = 20pF (SD read data valid).	-	10	ns	Figure 61
t_{HR}	SCK(pos)-to-SIO0 delay @ $C_{LOAD,MAX}$ = 20pF (SD read data hold).	2	-	ns	Figure 61
t_{QR1}, t_{QF1}	SIO_{OUT} rise/fall @ $C_{LOAD,MAX}$ = 20pF	-	12	ns	Figure 61
t_{PROP1}	SIO0-to-SIO1 or SIO1-to-SIO0 delay @ $C_{LOAD,MAX}$ = 20pF	-	20	ns	Figure 61
t_{NAPXA}	NAP exit delay - phase A	-	50	ns	Figure 50
t_{NAPXB}	NAP exit delay - phase B	-	40	ns	Figure 50
t_{PDNXA}	PDN exit delay - phase A	-	4	µs	Figure 50
t_{PDNXB}	PDN exit delay - phase B	-	9000	t_{CYCLE}	Figure 50
t_{AS}	ATTN-to-STBY power state delay	-	1	t_{CYCLE}	Figure 48
t_{SA}	STBY-to-ATTN power state delay	-	0	t_{CYCLE}	Figure 48
t_{ASN}	ATTN/STBY-to-NAP power state delay	-	8	t_{CYCLE}	Figure 49
t_{ASP}	ATTN/STBY-to-PDN power state delay	-	8	t_{CYCLE}	Figure 49

a. $t_{Q,MIN}$ and $t_{Q,MAX}$ for other t_{CYCLE} values can be interpolated between or extrapolated from the timings at the 3 specified t_{CYCLE} values.
b. This parameter also applies to a-1200 part when operated with t_{CYCLE} = 1.875ns
c. This parameter also applies to a-1200 or -1066 part when operated with t_{CYCLE} = 2.50ns

Timing Parameters

Table 13: Timing Parameter Summary

Parameter	Description	Min -32 -1200	Min -32P -1066	Min -40 -800	Min -45 -800	Max	Units	Figure(s)
t_{RC}	Row Cycle time of RDRAM banks -the interval between ROWA packets with ACT commands to the same bank.	32	28	28	28	-	t_{CYCLE}	Figure 16 Figure 17
t_{RAS}	RAS-asserted time of RDRAM bank - the interval between ROWA packet with ACT command and next ROWR packet with PRER[a] command to the same bank.	22	20	20	20	64µs[b]	t_{CYCLE}	Figure 16 Figure 17
t_{RP}	Row Precharge time of RDRAM banks - the interval between ROWR packet with PRER[a] command and next ROWA packet with ACT command to the same bank.	10	8	8	8	-	t_{CYCLE}	Figure 16 Figure 17
t_{PP}	Precharge-to-precharge time of RDRAM device - the interval between successive ROWR packets with PRER[a] commands to any banks of the same device.	8	8	8	8	-	t_{CYCLE}	Figure 13
t_{RR}	RAS-to-RAS time of RDRAM device - the interval between successive ROWA packets with ACT commands to any banks of the same device.	8	8	8	8	-	t_{CYCLE}	Figure 14
t_{RCD}	RAS-to-CAS Delay - the interval from ROWA packet with ACT command to COLC packet with RD or WR command). Note - the RAS-to-CAS delay seen by the RDRAM core (t_{RCD-C}) is equal to $t_{RCD-C} = 1 + t_{RCD}$ because of differences in the row and column paths through the RDRAM interface.	9	9	7	9	-	t_{CYCLE}	Figure 16 Figure 17
t_{CAC}	CAS Access delay - the interval from RD command to Q read data. The equation for t_{CAC} is given in the TPARM register in Figure 40.	9	8	8	8	12	t_{CYCLE}	Figure 5 Figure 40
t_{CWD}	CAS Write Delay (interval from WR command to D write data.	6	6	6	6	6	t_{CYCLE}	Figure 5
t_{CC}	CAS-to-CAS time of RDRAM bank - the interval between successive COLC commands).	4	4	4	4	-	t_{CYCLE}	Figure 16 Figure 17
t_{PACKET}	Length of ROWA, ROWR, COLC, COLM or COLX packet.	4	4	4	4	4	t_{CYCLE}	Figure 3
t_{RTR}	Interval from COLC packet with WR command to COLC packet which causes retire, and to COLM packet with bytemask.	8	8	8	8	-	t_{CYCLE}	Figure 18
t_{OFFP}	The interval (offset) from COLC packet with RDA command, or from COLC packet with retire command (after WRA automatic precharge), or from COLC packet with PREC command, or from COLX packet with PREX command to the equivalent ROWR packet with PRER. The equation for t_{OFFP} is given in the TPARM register in Figure 40.	4	4	4	4	4	t_{CYCLE}	Figure 15 Figure 40
t_{RDP}	Interval from last COLC packet with RD command to ROWR packet with PRER.	4	4	4	4	-	t_{CYCLE}	Figure 16
t_{RTP}	Interval from last COLC packet with automatic retire command to ROWR packet with PRER.	4	4	4	4	-	t_{CYCLE}	Figure 17

a. Or equivalent PREC or PREX command. See Figure 15.
b. This is a constraint imposed by the core, and is therefore in units of µs rather than t_{CYCLE}.

Absolute Maximum Ratings

Table 14: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{I,ABS}$	Voltage applied to any RSL or CMOS pin with respect to Gnd	- 0.3	V_{DD}+0.3	V
$V_{DD,ABS}$, $V_{DDA,ABS}$	Voltage on VDD and VDDA with respect to Gnd	- 0.5	V_{DD}+1.0	V
T_{STORE}	Storage temperature	- 50	100	°C
T_{MIN}	Minimum operation temperature	0	Note*	°C

Note*) Component : refer to T_J,Θ_{JC} Module: refre to $T_{PLATE, MAX}$

I_{DD} - Supply Current Profile

Table 15: Supply Current Profile

I_{DD} value	RDRAM Power State and Steady-State Transaction Rates[a]	Min	Max (1200MHz , -32)	Max (1066MHz , -32P)	Max (800MHz , -40/-45)	Unit
$I_{DD,PDN}$	Device in PDN, self-refresh enabled and INIT.LSR=0.	-	6000	6000	6000	uA
$I_{DD,NAP}$	Device in NAP.	-	4	4	4	mA
$I_{DD,STBY}$	Device in STBY. This is the average for a device in STBY with (1) no packets on the Channel, and (2) with packets sent to other devices.	-	115	105	95	mA
$I_{DD,REFRESH}$	Device in STBY and refreshing rows at the $t_{REF,MAX}$ period.	-	115	105	95	mA
$I_{DD,ATTN}$	Device in ATTN. This is the average for a device in ATTN with (1) no packets on the Channel, and (2) with packets sent to other devices.	-	170	160	135	mA
$I_{DD,ATTN-W}$	Device in ATTN. ACT command every 8•t_{CYCLE}, PRE command every 8•t_{CYCLE}, WR command every 4•t_{CYCLE}, and data is 1100..1100	-	830(x18)[b]	740(x18)	580(x18)	mA
$I_{DD,ATTN-R}$	Device in ATTN. ACT command every 8•t_{CYCLE}, PRE command every 8•t_{CYCLE}, RD command every 4•t_{CYCLE}, and data is 1111..1111[c]	-	830(x18)	750(x18)	600(x18)	mA

a. CMOS interface consumes power in all power states.
b. x18 RDRAM device data width.
c. This does not include the I_{OL} sink current. The RDRAM device dissipates I_{OL}•V_{OL} in each output driver when a logic one is driven.

Table 16: Supply Current at Initialization

Symbol	Parameter	Allowed Range of t_{CYCLE}	V_{DD}	Min	Max	Unit
$I_{DD,PWRUP,D}$	I_{DD} from power -on to SETR	1.667ns to 2.5ns	$V_{DD,MIN}$	-	200[a]	mA
$I_{DD,SETR,D}$	I_{DD} from SETR to CLRR	1.667ns to 2.5ns	$V_{DD,MIN}$	-	332	mA

a. The supply current will be 150mA when t_{CYCLE} is in the range 15ns to 1000ns.

Capacitance and Inductance

Table 17: RSL Pin Parasitics

Symbol	Parameter and Conditions - RSL pins	Min	Max	Unit	Figure
L_I	RSL effective input inductance @ t_{CYCLE}=1.667ns	-	3.5	nH	Figure 63
	RSL effective input inductance @ t_{CYCLE}=1.875ns	-	3.5		
	RSL effective input inductance @ t_{CYCLE}=2.5ns	-	4.0		
L_{12}	Mutual inductance between any DQA or DQB RSL signals.	-	0.2	nH	Figure 63
	Mutual inductance between any ROW or COL RSL signals.	-	0.6	nH	
ΔL_I	Difference in L_I value between any RSL pins of a single device.	-	1.8	nH	Figure 63
C_I	RSL effective input capacitance[a] @ t_{CYCLE}=1.667ns	2.0	2.3	pF	Figure 63
	RSL effective input capacitance[a] @ t_{CYCLE}=1.875ns	2.0	2.3		
	RSL effective input capacitance[a] @ t_{CYCLE}=2.5ns	2.0	2.4		
C_{12}	Mutual capacitance between any RSL signals.	-	0.1	pF	Figure 63
ΔC_I	Difference in C_I value between average of {CTM, CTMN, CFM, CFMN} and any RSL pins of a single device.	-	0.06	pF	Figure 63
R_I	RSL effective input resistance @ t_{CYCLE}=1.667ns	4	10	Ω	Figure 63
	RSL effective input resistance @ t_{CYCLE}=1.875ns	4	10		
	RSL effective input resistance @ t_{CYCLE}=2.5ns	4	15		

a. This value is a combination of the device IO circuitry and package capacitances

Table 18: CMOS Pin Parasitics

Symbol	Parameter and Conditions - CMOS pins	Min	Max	Unit	Figure
$L_{I,CMOS}$	CMOS effective input inductance	-	8.0	nH	Figure 63
$C_{I,CMOS}$	CMOS effective input capacitance (SCK,CMD)[a]	1.7	2.1	pF	
$C_{I,CMOS,SIO}$	CMOS effective input capacitance (SIO1, SIO0)[a]	-	7.0	pF	

a. This value is a combination of the device IO circuitry and package capacitances.

Center-Bonded WBGA Package (92balls)

Figure 4 shows the form and dimensions of the recommended package for the 92balls center-bonded WBGA device class.

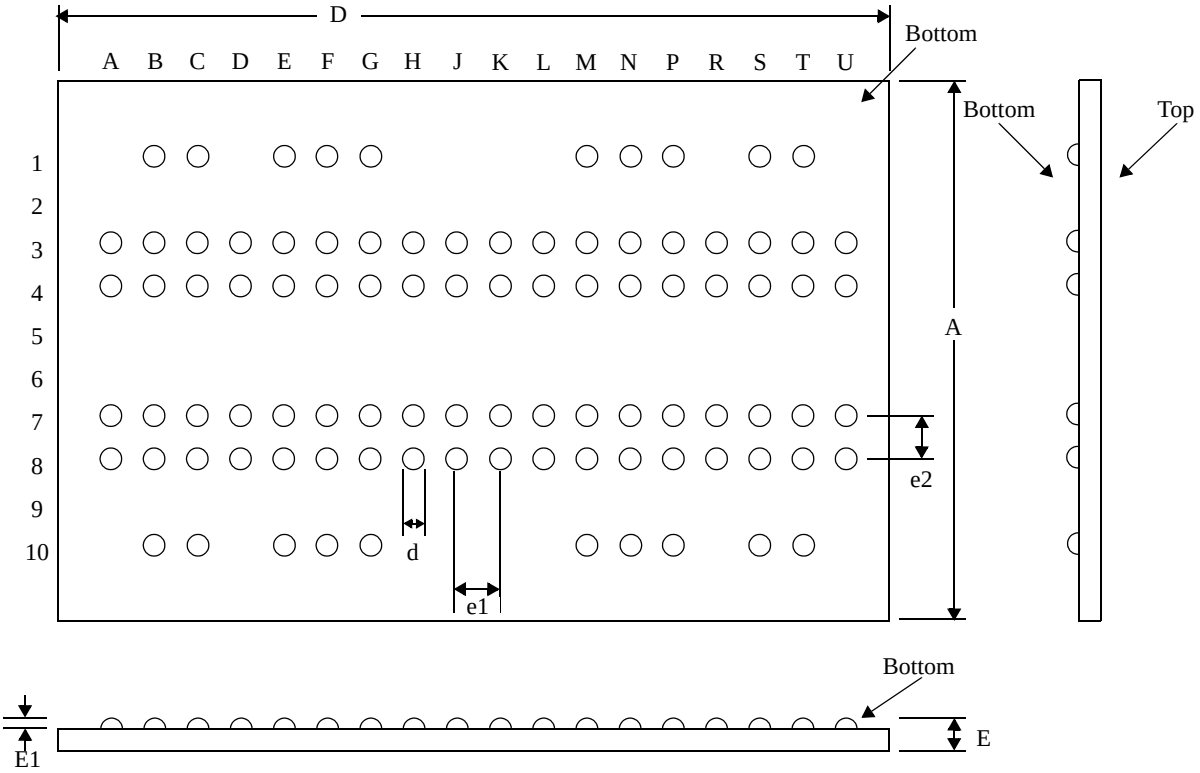


Figure 4: Center-Bonded WBGA Package

Table lists the numerical values corresponding to dimensions shown in Figure 4.

Table 19 : Center-Bonded WBGA Package Dimensions

Symbol	Parameter	Min.	Max.	Unit
e1	Ball pitch (x-axis)	0.80	0.80	mm
e2	Ball pitch (y-axis)	0.80	0.80	mm
A	Package body length	9.20	9.40	mm
D	Package body width	15.00	15.20	mm
E	Package total thickness	0.90	1.00	mm
E1	Ball height	0.30	0.40	mm
d	Ball diameter	0.40	0.50	mm