

Document Title

**64Kx16 Bit High Speed Static RAM(5.0V Operating), Revolutionary Pin out.
Operated at Commercial and Industrial Temperature Range.**

Revision History

<u>RevNo.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
Rev. 0.0	Initial release with Design Target.	Apr. 1st, 1997	Design Target
Rev. 1.0	Release to Preliminary Data Sheet. 1. Replace Design Target to Preliminary.	Jun. 1st, 1997	Preliminary
Rev. 2.0	Release to Final Data Sheet. 2.1. Delete Preliminary 2.2. Delete L-version. 2.3. Delete Data Retention Characteristics and Waveform. 2.4. Add Capacitive load of the test environment in A.C test load 2.5. Change D.C characteristics	Feb. 25th, 1998	Final
	Items	Previous spec. (8/10/12ns part)	Changed spec. (8/10/12ns part)
	Icc	200/190/180mA	200/195/190mA
	Isb	30mA	50mA

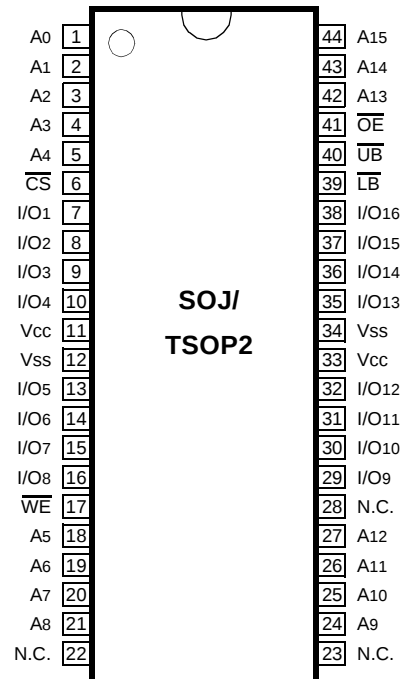
The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

64K x 16 Bit High-Speed CMOS Static RAM
FEATURES

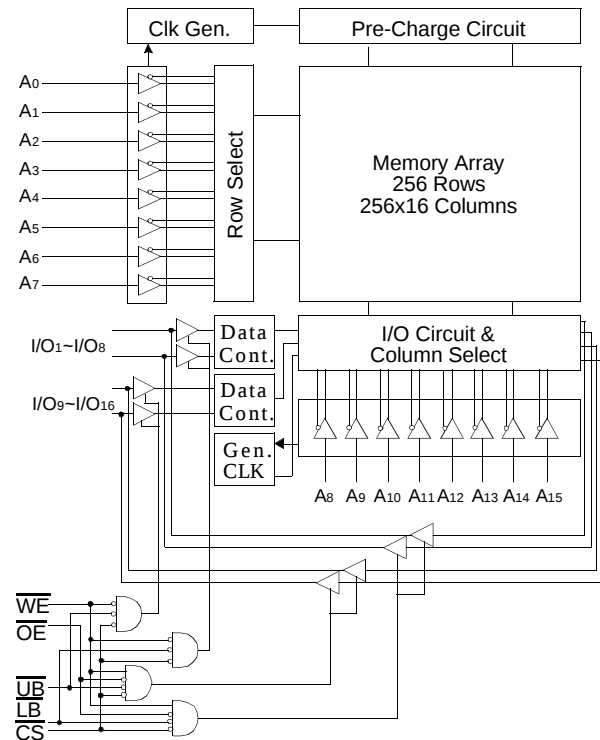
- Fast Access Time 8,10,12ns(Max.)
- Low Power Dissipation
 - Standby (TTL) : 50 mA(Max.)
 - (CMOS) : 10 mA(Max.)
- Operating KM6161002B - 8 : 200 mA(Max.)
- KM6161002B - 10 : 195 mA(Max.)
- KM6161002B - 12 : 190 mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Data Byte Control : $\overline{LB}$: I/O₁~ I/O₈, $\overline{UB}$: I/O₉~ I/O₁₆
- Standard Pin Configuration
 - KM6161002BJ : 44-SOJ-400
 - KM6161002BT : 44-TSOP2-400F

GENERAL DESCRIPTION

The KM6161002B is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits. The KM6161002B uses 16 common input and output lines and has at output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{UB}$, $\overline{LB}$). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM6161002B is packaged in a 400mil 44-pin plastic SOJ or TSOP2 forward.

PIN CONFIGURATION (Top View)

ORDERING INFORMATION

KM6161002B -8/10/12	Commercial Temp.
KM6161002BI -8/10/12	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM

PIN FUNCTION

Pin Name	Pin Function
A ₀ - A ₁₅	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O ₁ ~I/O ₈)
$\overline{UB}$	Upper-byte Control(I/O ₉ ~I/O ₁₆)
I/O ₁ ~ I/O ₁₆	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}		V _{IN} , V _{OUT}	-0.5 to 7.0	V
Voltage on V _{CC} Supply Relative to V _{SS}		V _{CC}	-0.5 to 7.0	V
Power Dissipation		P _D	1.0	W
Storage Temperature		T _{STG}	-65 to 150	°C
Operating Temperature	Commercial	T _A	0 to 70	°C
	Industrial	T _A	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A= to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.2	-	V _{CC} +0.5**	V
Input Low Voltage	V _{IL}	-0.5*	-	0.8	V

NOTE: The above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤6ns) for I_S≤20mA

** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width≤6ns) for I_S≤20mA

DC AND OPERATING CHARACTERISTICS (T_A=0 to 70°C, V_{CC}=5.0V±10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I _{LI}	V _{IN} =V _{SS} to V _{CC}		-2	2	μA
Output Leakage Current	I _{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{OUT} =V _{SS} to V _{CC}		-2	2	μA
Operating Current	I _{CC}	Min. Cycle, 100% Duty $\overline{CS}=V_{IL}$, V _{IN} = V _{IH} or V _{IL} , I _{OUT} =0mA	8ns	-	200	mA
			10ns	-	195	
			12ns	-	190	
Standby Current	I _{SB}	Min. Cycle, $\overline{CS}=V_{IH}$		-	50	mA
	I _{SB1}	f=0MHz, $\overline{CS} \geq V_{CC}-0.2V$, V _{IN} ≥V _{CC} -0.2V or V _{IN} ≤0.2V		-	10	
Output Low Voltage Level	V _{OL}	I _{OL} =8mA		-	0.4	V
Output High Voltage Level	V _{OH}	I _{OH} =-4mA		2.4	-	V
	V _{OH1} *	I _{OH1} =-0.1mA		-	3.95	V

NOTE: The above parameters are also guaranteed at industrial temperature range.

* V_{CC}=5.0V, Temp.=25°C

CAPACITANCE* (T_A=25°C, f=1.0MHz)

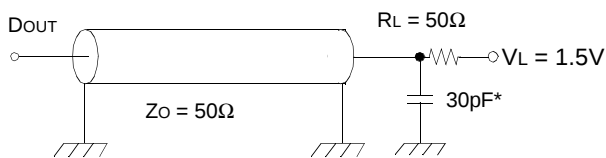
Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C _{I/O}	V _{I/O} =0V	-	8	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	6	pF

* NOTE : Capacitance is sampled and not 100% tested.

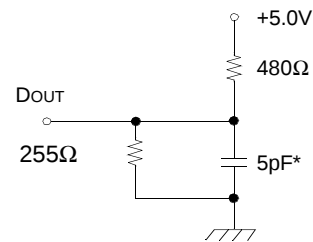
AC CHARACTERISTICS ($T_A=0$ to 70°C , $V_{CC}=5.0\text{V}\pm 10\%$, unless otherwise noted.)**TEST CONDITIONS**

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: The above test conditions are also applied at industrial temperature range.

Output Loads(A)**Output Loads(B)**

for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Capacitive Load consists of all components of the test environment.

* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM6161002B-8		KM6161002B-10		KM6161002B-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	8	-	10	-	12	-	ns
Address Access Time	tAA	-	8	-	10	-	12	ns
Chip Select to Output	tCO	-	8	-	10	-	12	ns
Output Enable to Valid Output	tOE	-	4	-	5	-	6	ns
$\overline{UB}$, $\overline{LB}$ Access Time	tBA	-	4	-	5	-	6	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5	0	6	ns
Output Disable to High-Z Output	tOHZ	0	4	0	5	0	6	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	tBHZ	0	4	0	5	0	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

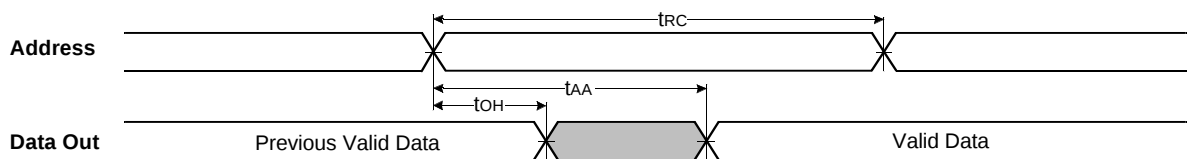
NOTE: The above parameters are also guaranteed at industrial temperature range.

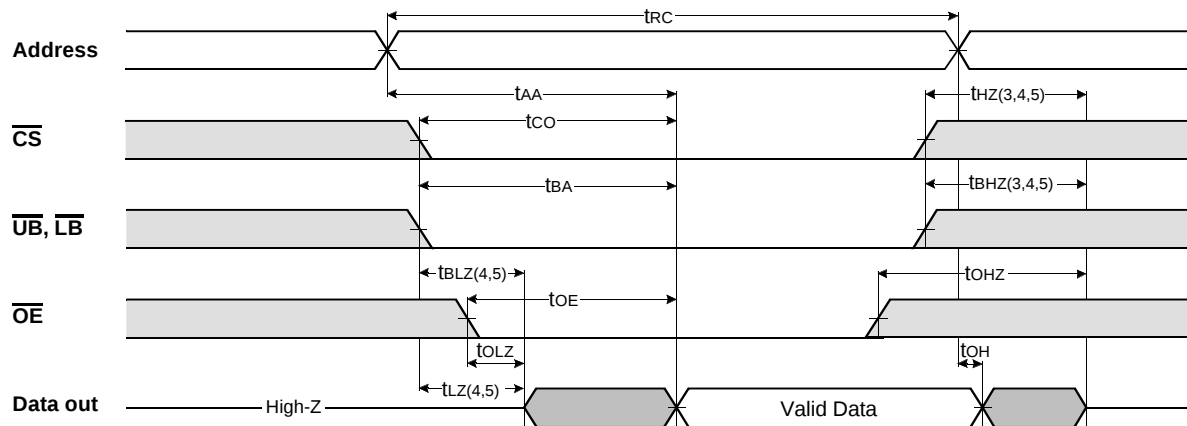
WRITE CYCLE

Parameter	Symbol	KM6161002B-8		KM6161002B-10		KM6161002B-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	8	-	10	-	12	-	ns
Chip Select to End of Write	t _{CW}	6	-	7	-	8	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t _{AW}	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ High)	t _{WP}	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ Low)	t _{WP1}	8	-	10	-	12	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t _{BW}	6	-	7	-	8	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t _{WHZ}	0	4	0	5	0	6	ns
Data to Write Time Overlap	t _{DW}	4	-	5	-	6	-	ns
Data Hold from Write Time	t _{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t _{OW}	3	-	3	-	3	-	ns

NOTE: The above parameters are also guaranteed at industrial temperature range.

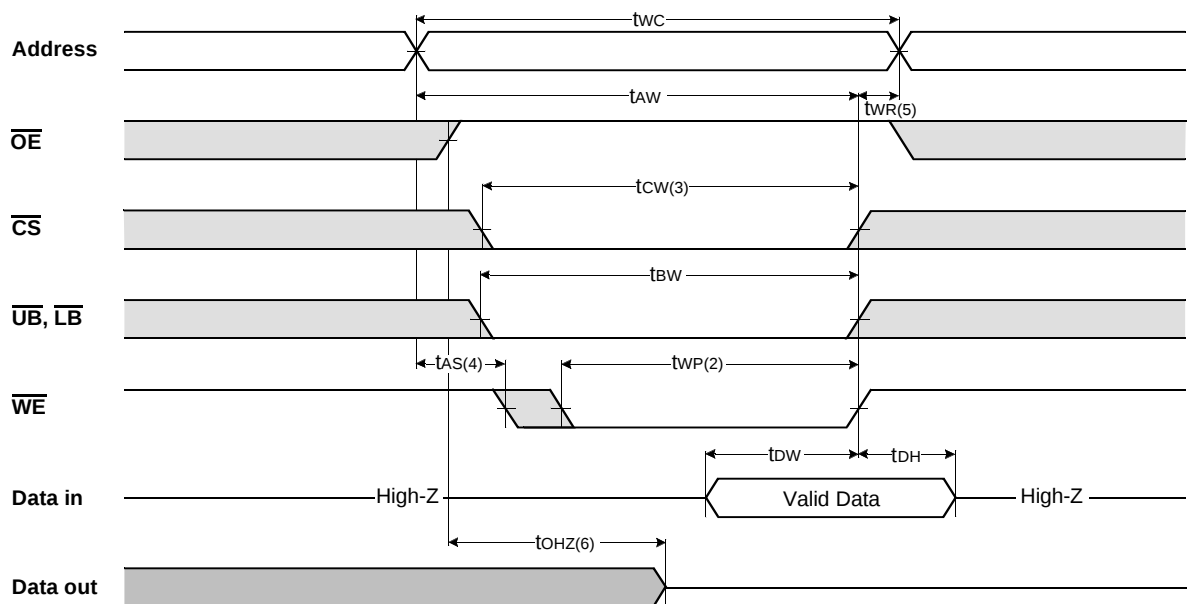
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, $\overline{UB}$, $\overline{LB}=V_{IL}$)

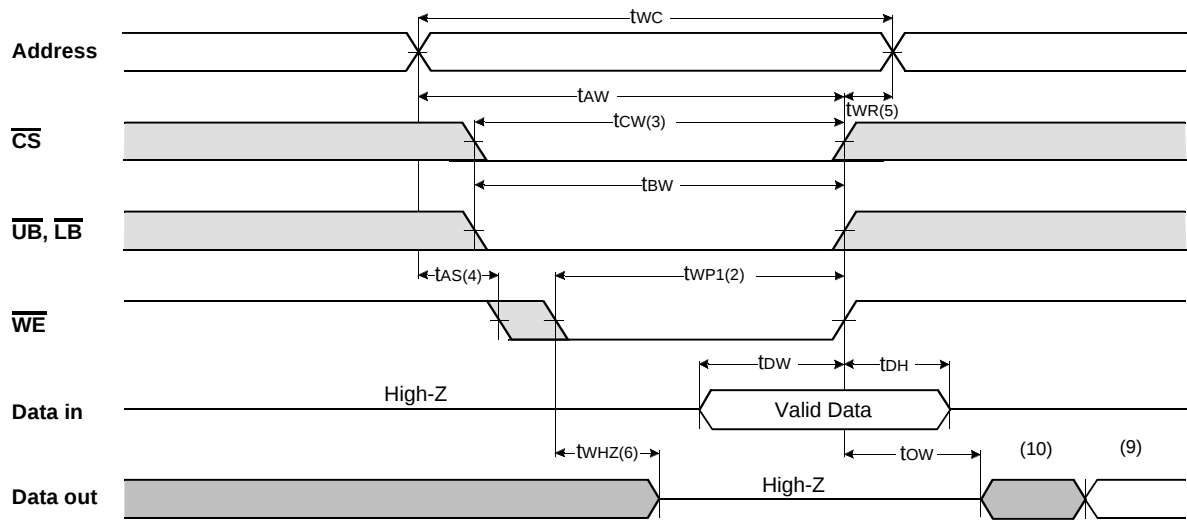
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)

NOTES(READCYCLE)

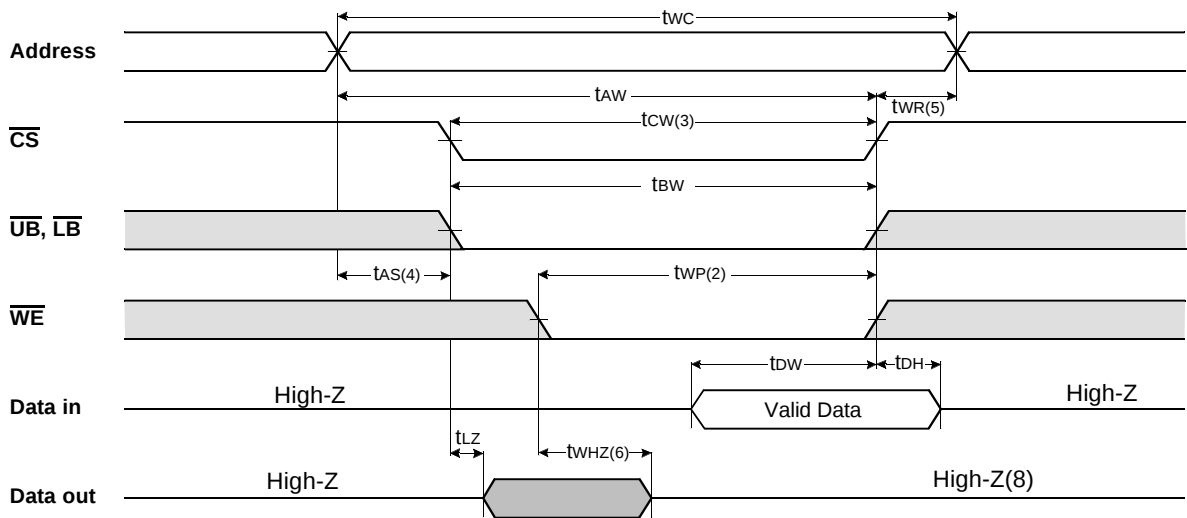
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}=V_{IL}$.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

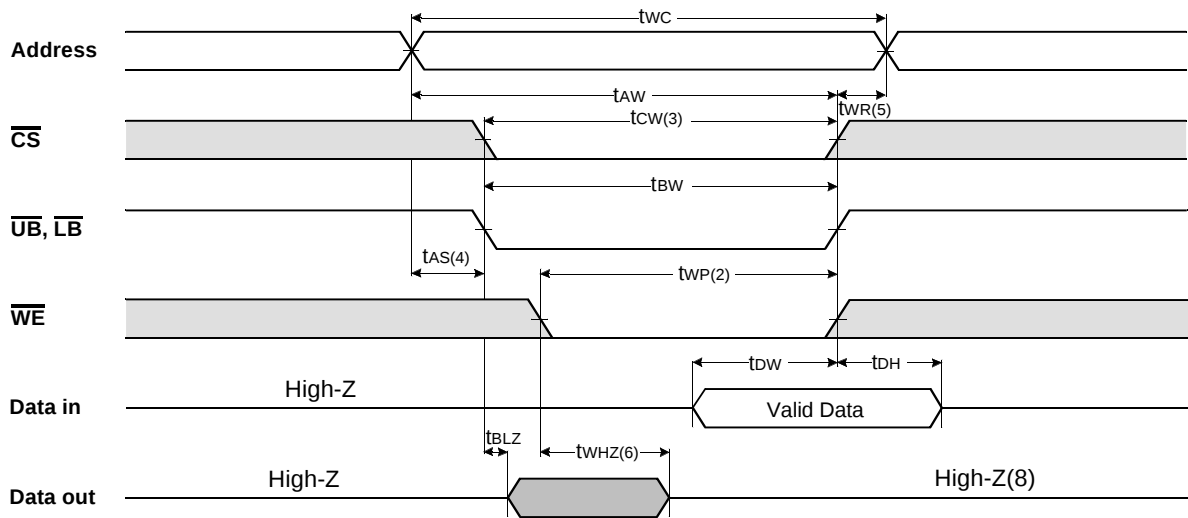
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)

TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ = Low fixed)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{CS}$ = Controlled)



TIMING WAVEFORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$, $\overline{WE}$, $\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

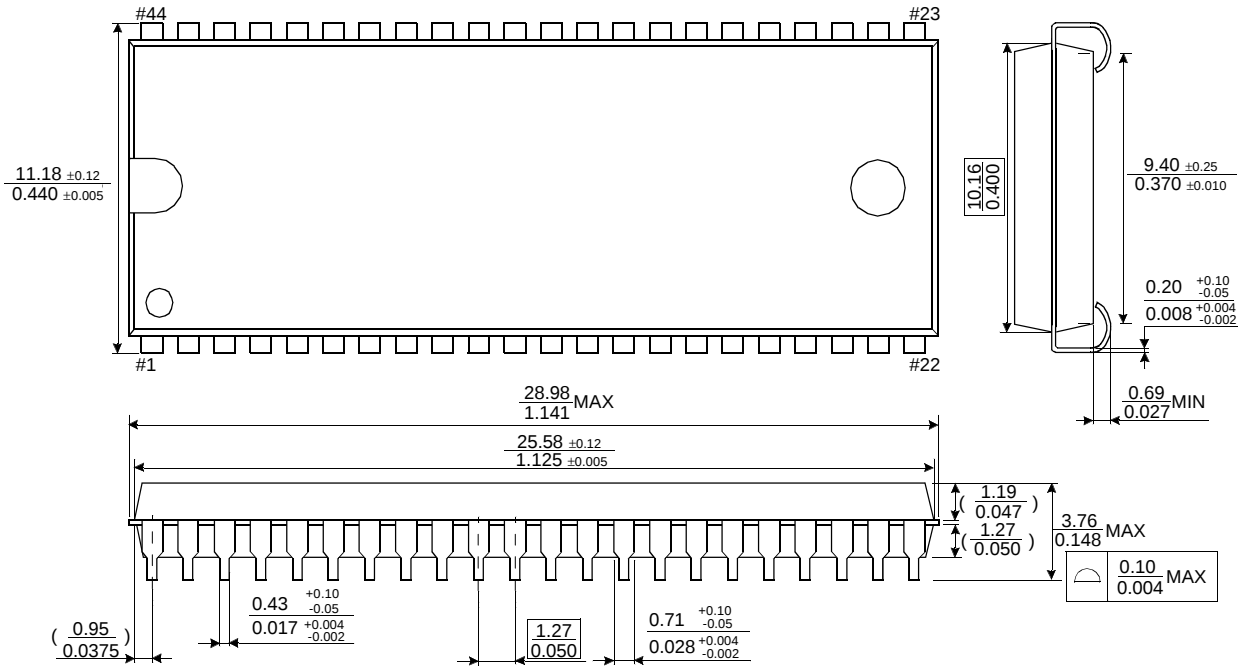
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X*	X	X	Not Select	High-Z	High-Z	ISB, ISB1
L	H	H	X	X	Output Disable	High-Z	High-Z	Icc
L	X	X	H	H				
L	H	L	L	H	Read	DOUT	High-Z	Icc
			H	L		High-Z	DOUT	
			L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	Icc
			H	L		High-Z	DIN	
			L	L		DIN	DIN	

* NOTE : X means Don't Care.

PACKAGE DIMENSIONS

44-SOJ-400

Units: millimeters/Inches



44-TSOP2-400F

Units: millimeters/Inches

