RF3315

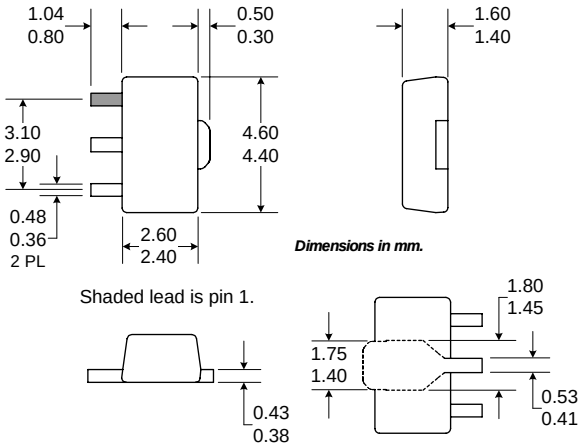
BROADBAND HIGH LINEARITY AMPLIFIER

Typical Applications

- Basestation Applications
- Cellular and PCS Systems
- WLL, W-CDMA Systems
- Final PA for Low-Power Applications

Product Description

The RF3315 is a high-efficiency GaAs Heterojunction Bipolar Transistor (HBT) amplifier packaged in a low-cost surface-mount package. This amplifier is ideal for use in applications requiring high-linearity and low noise figure over the 300MHz to 3GHz frequency range. The RF3315 operates from a single 5V power supply.



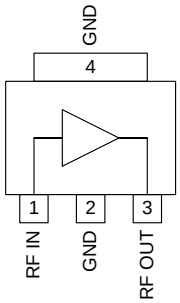
Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS
- ☐ InGaP/HBT
- ☐ GaN HEMT
- ☐ SiGe Bi-CMOS

Package Style: SOT89

Features

- 300MHz to 3GHz
- +40dBm Output IP3
- 12.5dB Gain at 2.0GHz
- +23dBm P1dB
- 3.0dB Typical Noise Figure at 2.0GHz
- Single 5V Power Supply



Functional Block Diagram

Ordering Information

RF3315	Broadband High Linearity Amplifier
RF3315PCBA-410	Fully Assembled Evaluation Board (2GHz)
RF3315PCBA-411	Fully Assembled Evaluation Board (900MHz)

RF Micro Devices, Inc.
7628 Thorndike Road
Greensboro, NC 27409, USA
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Fax (336) 664 0454
http://www.rfmd.com

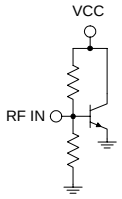
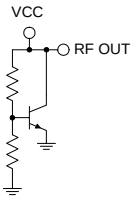
Absolute Maximum Ratings

Parameter	Rating	Unit
RF Input Power	+20	dBm
Device Voltage	-0.5 to +6.0	V
Device Current	250	mA
Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

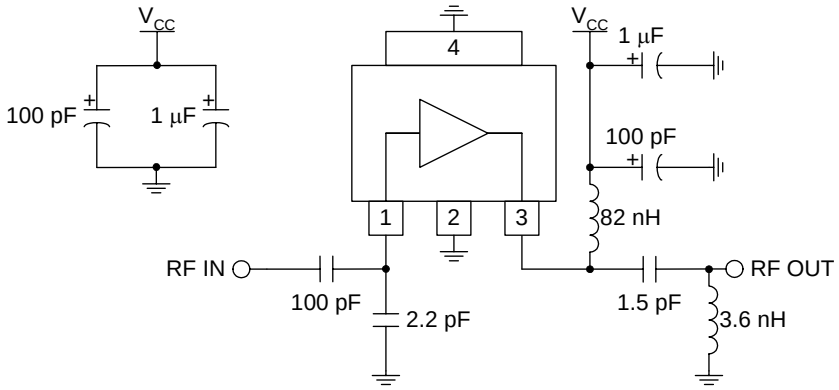
Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					
AC Specifications (2GHz)					V_{CC}=5V, RF_{IN}=-10dBm, Freq=2.0GHz, with 2GHz application schematic.
Frequency	300		3000	MHz	
Gain (Small Signal)	11.0	12.5		dB	F=2GHz
Input Return Loss		15		dB	F=2GHz
Output Return Loss		15		dB	F=2GHz
Output IP3	+36	+40.0		dBm	F_1= 1.99GHz, F_2=2.00GHz, P_{IN}=-5dBm
Output P1dB	+21	+23.0		dBm	
Noise Figure		3.0	4.0	dB	
AC Specifications (900MHz)					V_{CC}=5V, RF_{IN}=-10dBm, Freq=900MHz, with 900MHz application schematic.
Frequency	300		3000	MHz	
Gain (Small Signal)	16	18		dB	
Input Return Loss		20		dB	
Output Return Loss		20		dB	
Output IP3	+36	+41		dBm	F_1= 900MHz, F_2=901MHz, P_{IN}=-10dBm
Output P1dB	+23	+25		dBm	
Noise Figure		2.5	3.5	dB	
Thermal					I_{CC}=150mA, P_{DISS}=770mW. (See Note.)
$Theta_{JC}$		88		°C/W	
Maximum Measured Junction Temperature at DC Bias Conditions		154		°C	T_{CASE}=+85°C
Mean Time To Failure		370		years	T_{CASE}=+85°C
DC Specifications					
Device Voltage	4.5	5.0	5.5	V	I_{CC}=150mA
Operating Current Range	100	150	170	mA	V_{CC}=5V

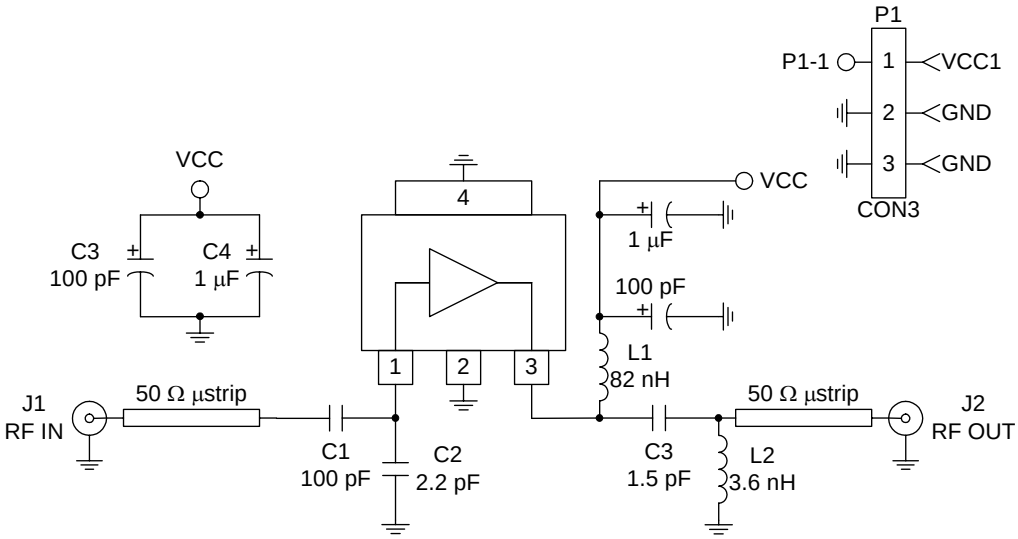
Note: The RF3315 must be operated at or below 170mA to ensure the highest possible reliability and electrical performance.

Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is not internally DC-blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications.	
2	GND	Ground connection.	
3	RF OUT	RF output and bias pin. For biasing, an RF choke is needed. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. See application schematic for configuration and value.	
4	GND	Ground connection.	
Pkg Base	GND	Ground connection.	

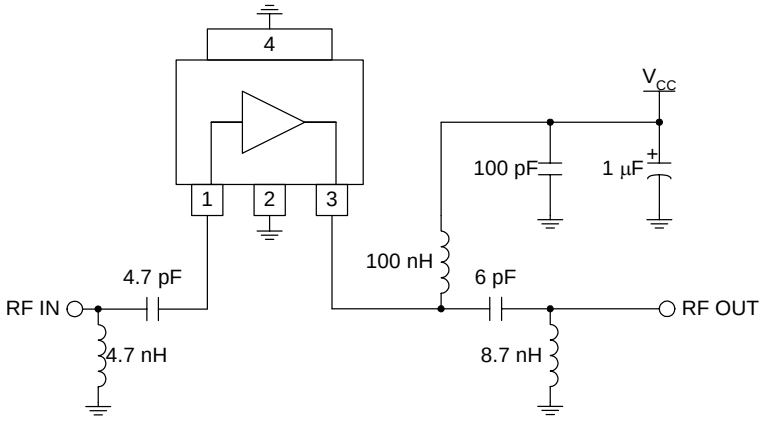
Typical Application Schematic for 2GHz



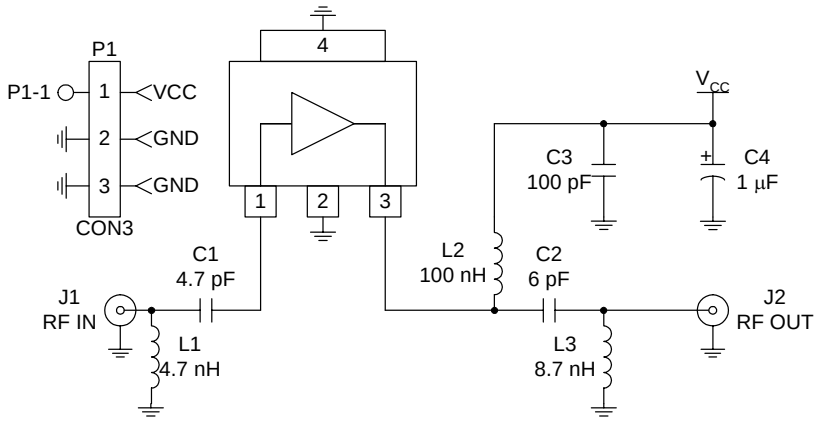
Evaluation Board Schematic for 2GHz



Typical Application Schematic for 900MHz



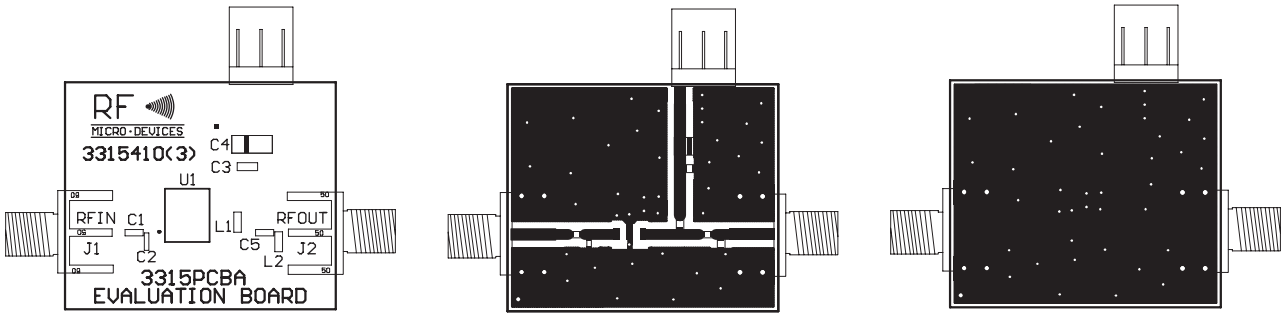
Evaluation Board Schematic for 900MHz



Evaluation Board Layout for 1.9GHz
Board Size 1.195” x 1.000”

Board Thickness 0.033”, Board Material FR-4

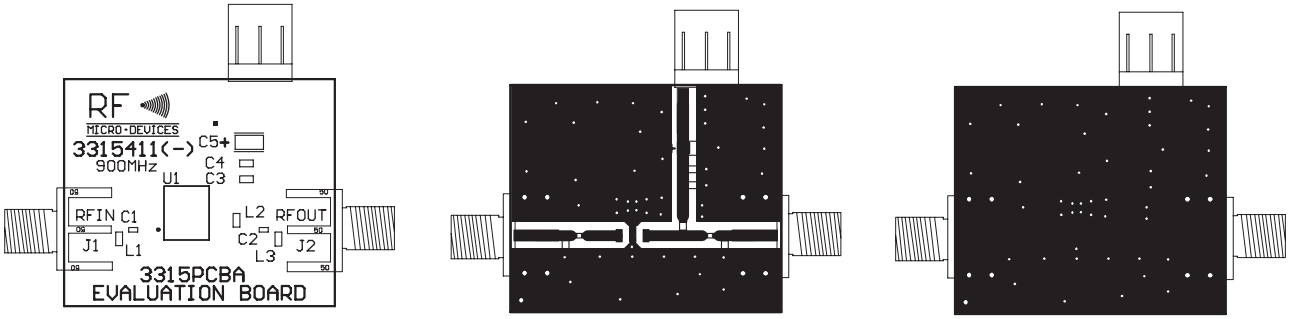
Note: A small amount of ground inductance is required to achieve datasheet performance. The necessary inductance may be generated by ensuring that no ground vias are placed directly below the footprint of the part.



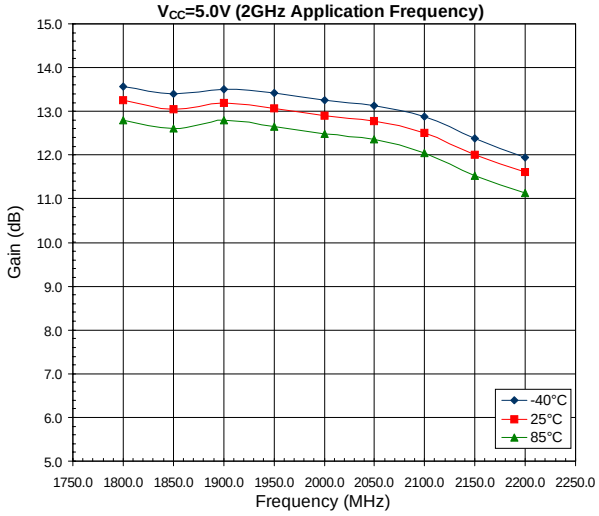
Evaluation Board Layout for 900MHz
Board Size 1.195” x 1.000”

Board Thickness 0.033”, Board Material FR-4

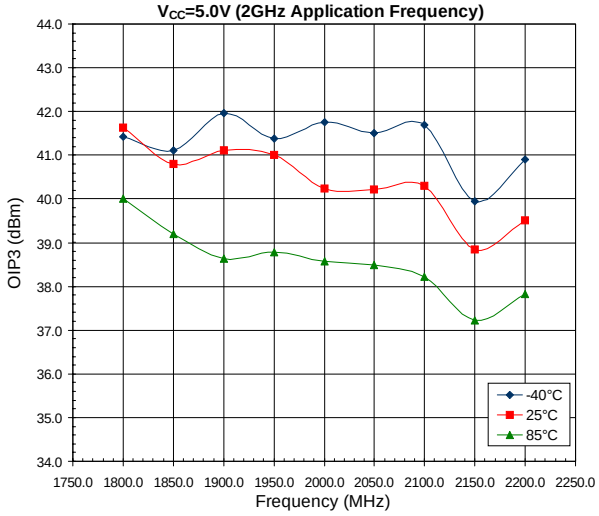
Note: A small amount of ground inductance is required to achieve datasheet performance. The necessary inductance may be generated by ensuring that no ground vias are placed directly below the footprint of the part.



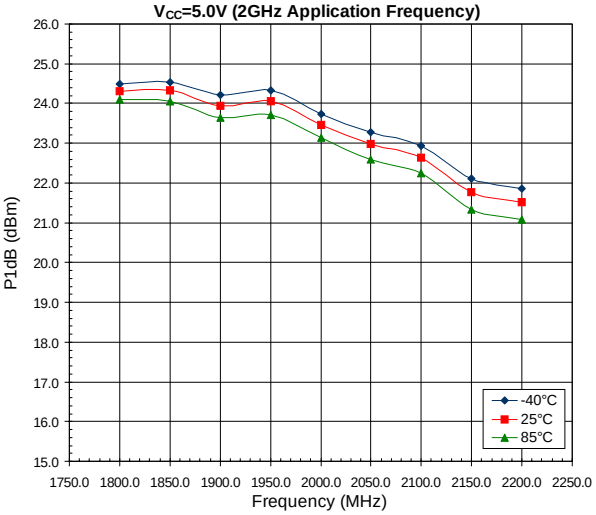
Gain versus Frequency Across Temperature,
V_{CC}=5.0V (2GHz Application Frequency)



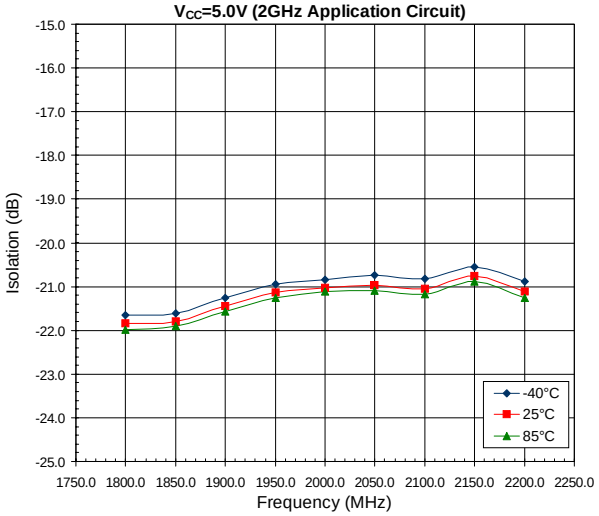
OIP3 versus Frequency Across Temperature
V_{CC}=5.0V (2GHz Application Frequency)



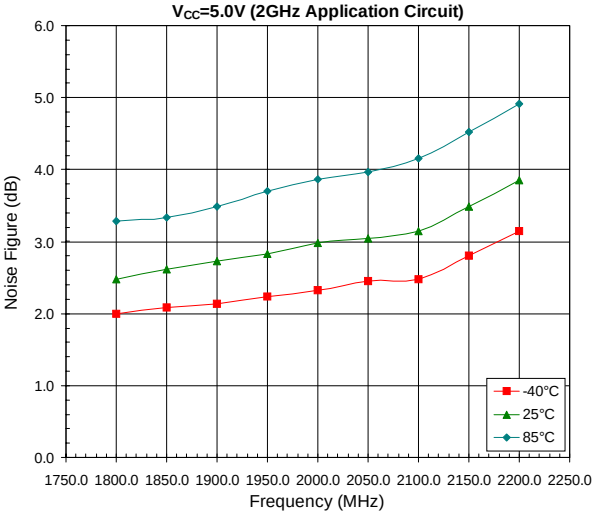
P1dB versus Frequency Across Temperature
V_{CC}=5.0V (2GHz Application Frequency)



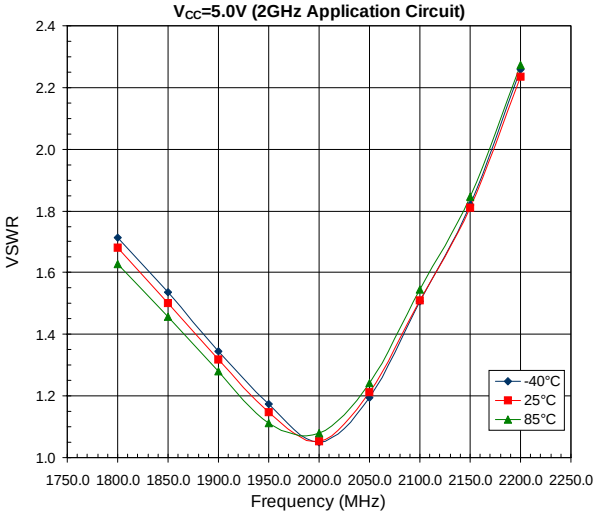
Reverse Isolation versus Frequency Across Temp
V_{CC}=5.0V (2GHz Application Circuit)



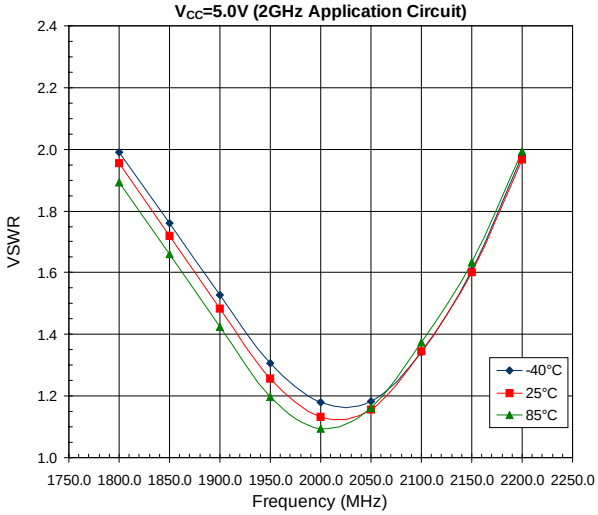
Noise Figure versus Frequency Across Temperature
V_{CC}=5.0V (2GHz Application Circuit)



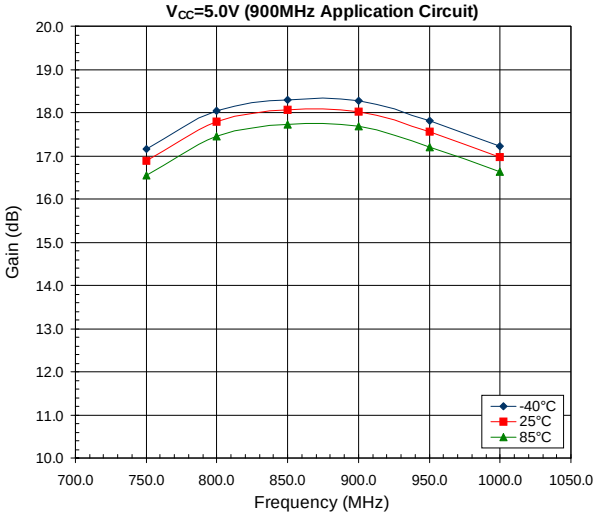
Input VSWR versus Frequency Across Temperature,
V_{CC}=5.0V (2GHz Application Circuit)



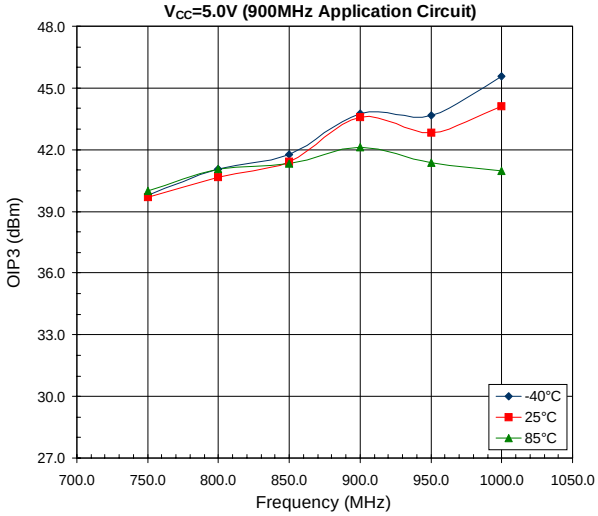
Output VSWR versus Frequency Across Temperature,
V_{CC}=5.0V (2GHz Application Circuit)



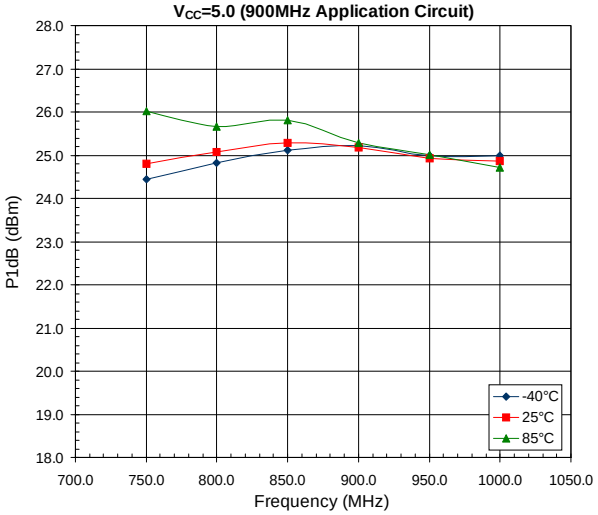
Gain versus Frequency Across Temperature,
V_{CC}=5.0V (900MHz Application Circuit)



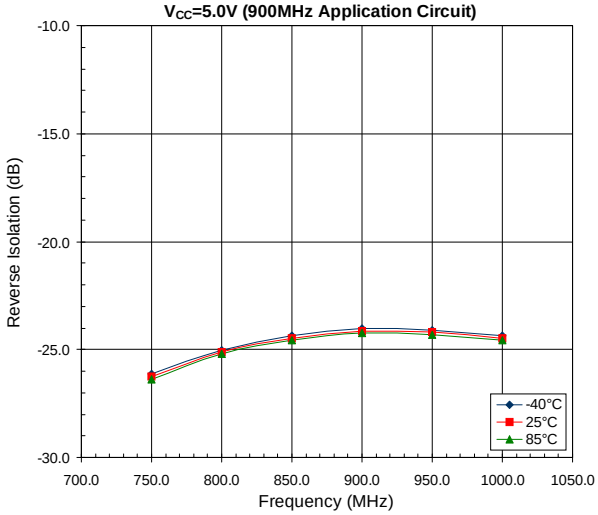
OIP3 versus Frequency Across Temperature
V_{CC}=5.0V (900MHz Application Circuit)



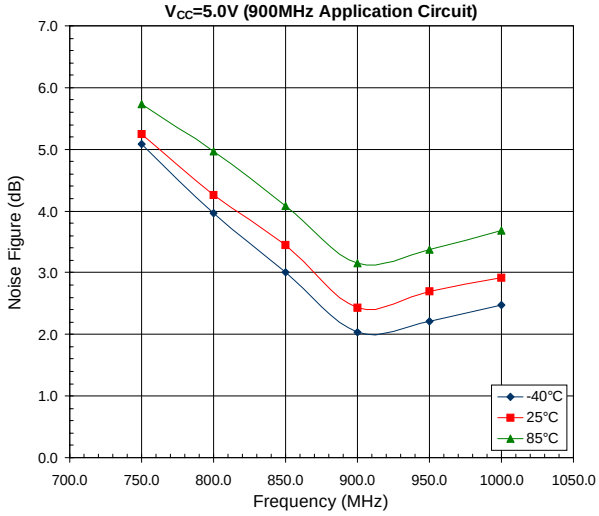
P1dB versus Frequency Across Temperature
V_{CC}=5.0 (900MHz Application Circuit)



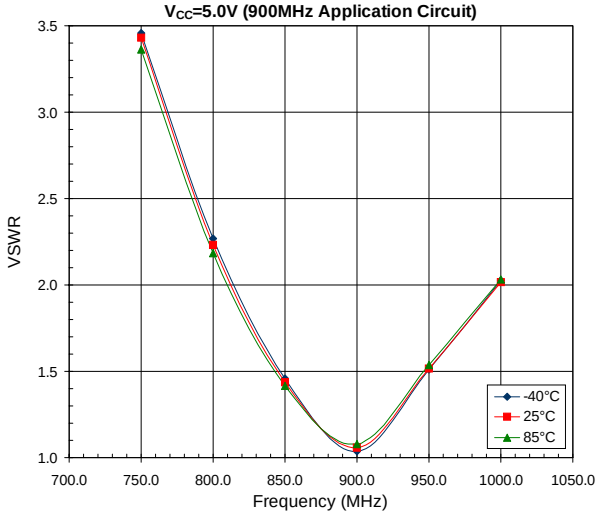
Reverse Isolation versus Frequency Across Temp,
V_{CC}=5.0V (900MHz Application Circuit)



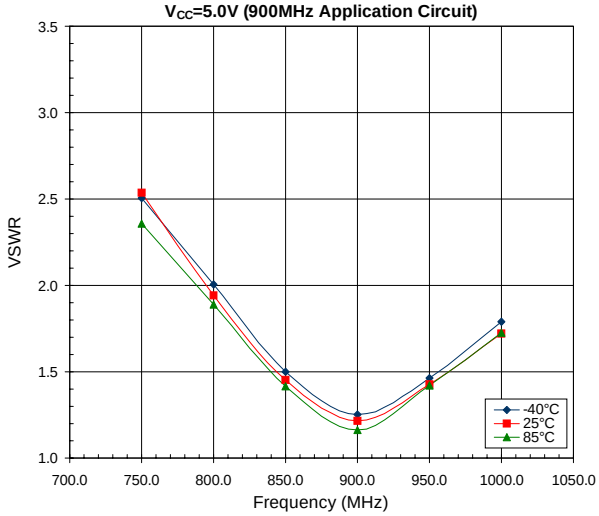
Noise Figure versus Frequency Across Temperature
V_{CC}=5.0V (900MHz Application Circuit)



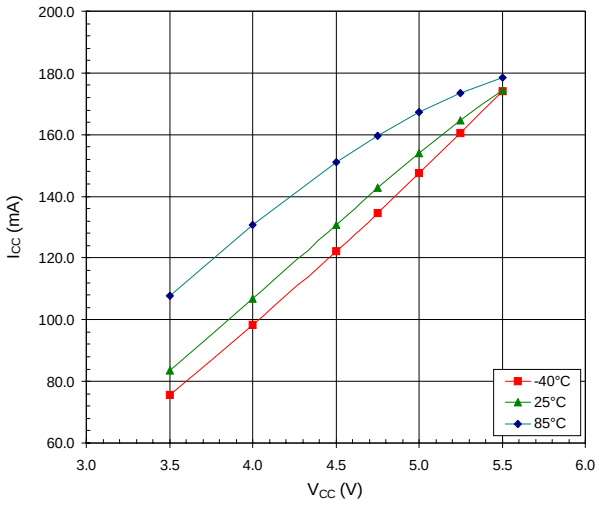
Input VSWR versus Frequency Across Temperature
V_{CC}=5.0V (900MHz Application Circuit)



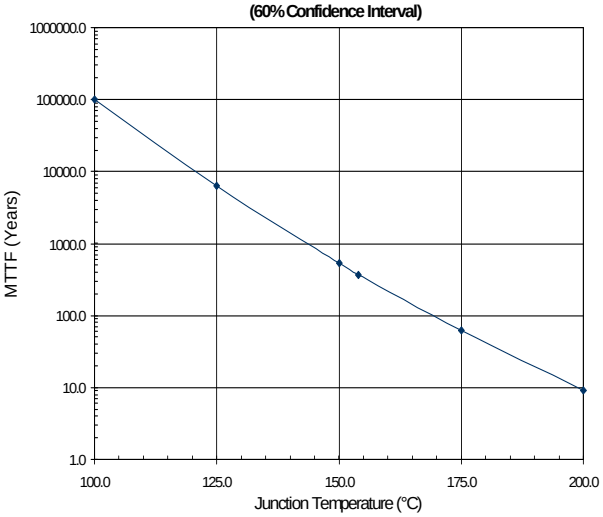
Output VSWR versus Frequency Across Temperature,
V_{CC}=5.0V (900MHz Application Circuit)

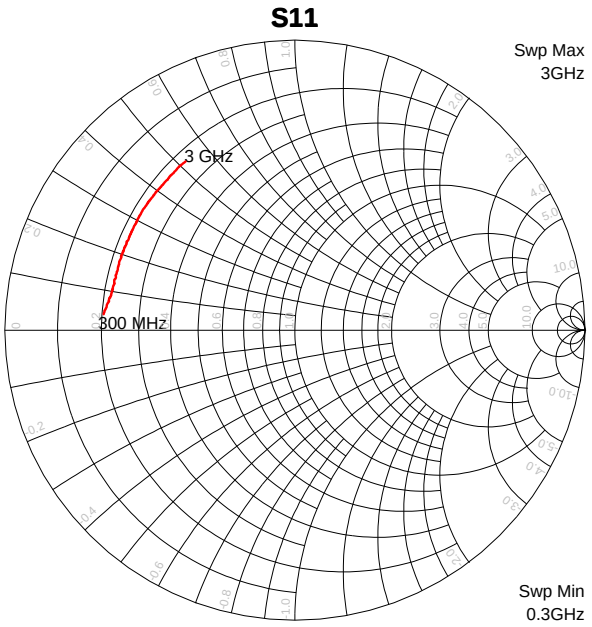


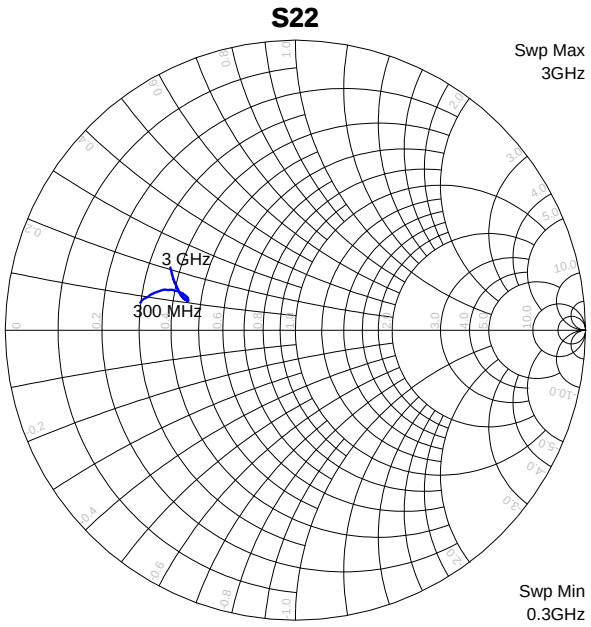
I_{CC} versus V_{CC} Across Temperature



MTTF versus Junction Temperature,
(60% Confidence Interval)




S11
Swp Max
3GHz
3 GHz
300 MHz
Swp Min
0.3GHz


S22
Swp Max
3GHz
3 GHz
300 MHz
Swp Min
0.3GHz

PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Pattern

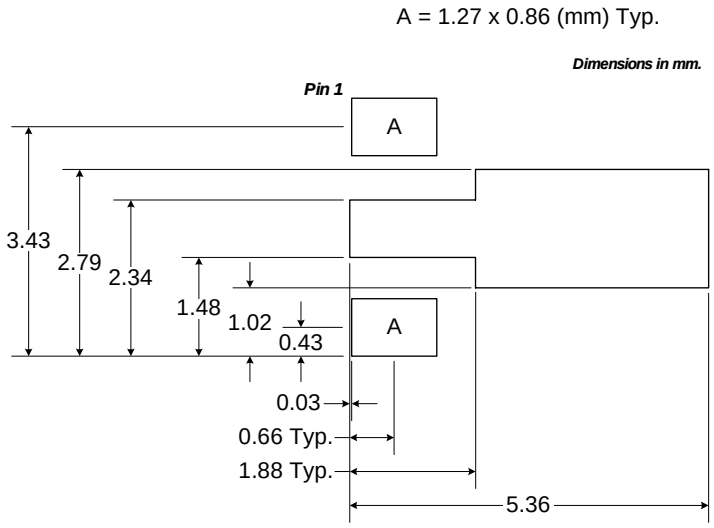


Figure 1. PCB Metal Land Pattern (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

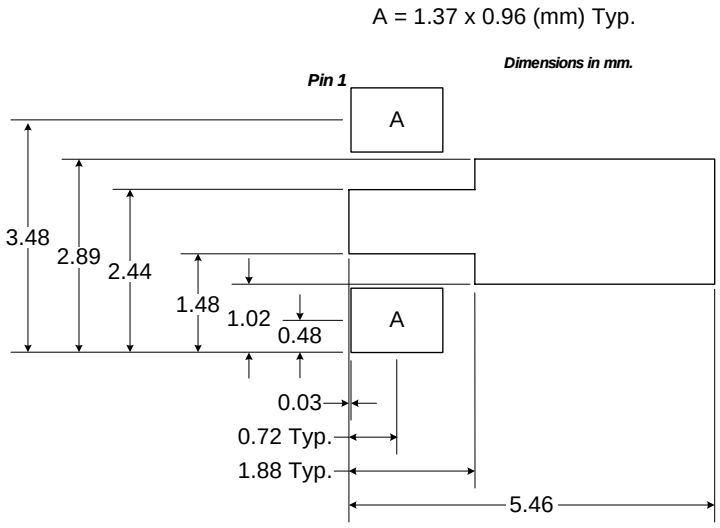


Figure 2. PCB Solder Mask Pattern (Top View)

Thermal Pad and Via Design

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.