PYRAMID
SEMICONDUCTOR CORPORATION

P4C422

HIGH SPEED 256 X 4 STATIC CMOS RAM

FEATURES

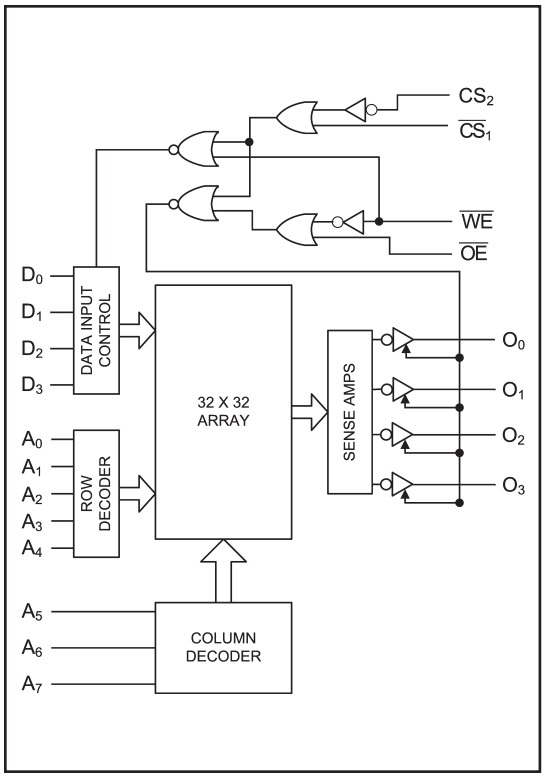
- **High Speed (Equal Access and Cycle Times)**
  - **– 10/12/15/20/25/35 ns (Commercial)**
  - **– 15/20/25/35 ns (Military)**
- **CMOS for Low Power**
  - **– 495 mW Max. – 10/12/15/20/25 (Commercial)**
  - **– 495 mW Max. – 15/20/25/35 (Military)**
- **Single 5V±10% Power Supply**
- **Separate I/O**
- **Fully TTL Compatible Inputs and Outputs**
- **Resistant to single event upset and latchup resulting from advanced process and design improvements.**
- **Standard Pinout (JEDEC Approved)**
  - **– 22-Pin 400 mil DIP**
  - **– 24-Pin 300 mil SOIC**
  - **– 24-Pin Square LCC**
  - **– 24-Pin CERPACK**

DESCRIPTION

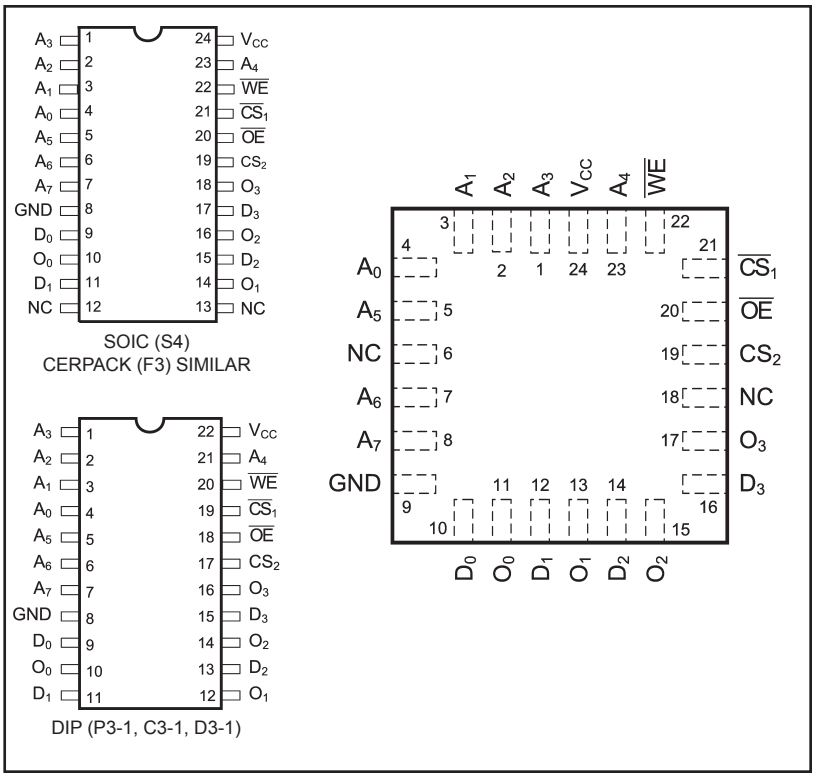
The P4C422 is a 1,024-bit high-speed (10ns) Static RAM with a 256 x 4 organization. The memory requires no clocks or refreshing and has equal access and cycle times. Inputs and outputs are fully TTL compatible. Operation is from a single 5 Volt supply. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS}_1$) and active HIGH chip select two (CS_2) as well as 3-state outputs.

In addition to high performance and high density, the device features latch-up protection, single event and upset protection. The P4C422 is offered in several packages: 22-pin 400 mil DIP (plastic and ceramic), 24-pin 300 mil SOIC, 24-pin square LCC and 24-pin CERPACK. Devices are offered in both commercial and military temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



MAXIMUM RATINGS[1]

Sym	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	-0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to VCC + 0.5	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	DC Output Current	50	mA

RECOMMENDED OPERATING CONDITIONS

Grade[2]	Ambient Temp	GND	V_{cc}
Commercial	0°C to 70°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

CAPACITANCES[4]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Sym	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	7	pF

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)[2]

Sym	Parameter	Test Conditions	P4C422		Unit
			Min	Max	
V_{OH}	Output High Voltage	I_{OH} = -5.2 mA, V_{CC}=Min 2.4	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = +8 mA, V_{CC}=Min		0.4	V
V_{IH}	Input High Voltage		2.1		V
V_{IL}	Input Low Voltage			0.8	V
V_{CL}	Input Clamp Diode Voltage	I_{IN}= -10 mA	-1.5		V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}	-10	10	µA
I_{OZ}	Output Current (High Z)	V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled	-10	10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC}=Max, V_{OUT}=GND		90	mA

POWER DISSIPATION CHARACTERISTICS VS. SPEED

Sym	Parameter	Temperature Range	-10	-12	-15	-20	-25	-35	Unit
I_{CC}	Dynamic Operating Current	Commercial	90	90	90	90	65	65	mA
		Military	N/A	N/A	90	90	90	90	mA

Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. This parameter is sampled and not 100% tested.
5. Transition time is ≤ 3ns for 10,12, and 15 ns products and ≤ 5ns for 20, 25, and 35 ns products, see Fig 1d. Timing is referenced at input and output levels of 1.5V. The output loading is equivalent to the specified I_{OL}/I_{OH} with a load capacitance of 15 pF (10,12) or 30 pF (15, 20, 25, 35) as in Fig.1a and 1b respectively.
6. Transition time is ≤ 3ns for 10, 12, and 15ns products and ≤ 5ns for 20, 25, and 35ns products, see Fig 1d. Transition is measured at steady state HIGH level -500mV or steady state LOW level +500mV on the output from a level on the input with load shown in Fig. 1c.
7. t_W is measured at t_{WSA}=min.; t_{WSA} is measured at t_W=min.

FUNCTIONAL DESCRIPTION

An active LOW write enable ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select one ($\overline{CS_1}$) and the write enable ($\overline{WE}$) are LOW and the chip select two (CS_2) is HIGH, the information on data inputs (D_0 through D_3) is written into the addressed memory word and preconditions the output circuitry so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch." Reading is performed with chip select one ($\overline{CS_1}$) LOW, chip select two (CS_2) HIGH, write enable ($\overline{WE}$) HIGH and output enable ($\overline{OE}$) LOW. The information stored in the addressed word is read out on the noninverting outputs (O_0 through O_3). The outputs of the memory go to an inactive high impedance state whenever chip select one ($\overline{CS_1}$) is HIGH, or during the write operation when write enable ($\overline{WE}$) is LOW.

TRUTH TABLE

Mode	CS_2	$\overline{CS_1}$	$\overline{WE}$	$\overline{OE}$	Output
Standby	L	X	X	X	High Z
Standby	X	H	X	X	High Z
D_{OUT} Disabled	H	L	X	H	High Z
Read	H	L	H	L	D_{OUT}
Write	H	L	L	X	High Z

Notes:

H = HIGH
L = LOW
X = Don't Care
HIGH Z = Implies outputs are disabled or off. This condition is defined as high impedance state for the P4C422.

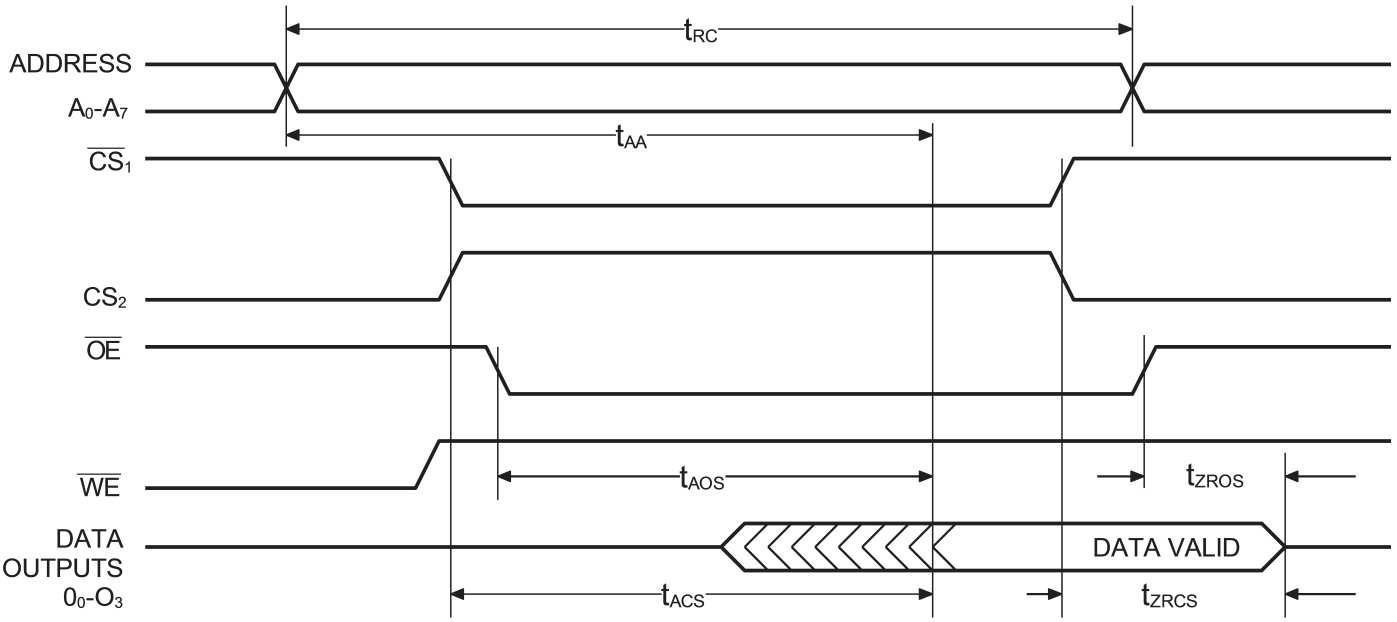
AC ELECTRICAL CHARACTERISTICS—READ CYCLE

(V_{CC} = 5V ± 10% except as noted, All Temperature Ranges)[2]

Sym	Parameter	-10*		-12		-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time [5]	12		12		15		20		25		35		ns
t_{ACS}	Chip Select Time [5]		7.5		8		8		12		15		25	ns
t_{ZRCS}	Chip Select to High-Z [6]		8		10		12		15		20		30	ns
t_{AOS}	Output Enable Time		7.5		8		8		12		15		25	ns
t_{ZROS}	Output Enable to High-Z [6]		8		10		12		15		20		30	ns
t_{AA}	Address Access Time [5]		10		12		15		20		25		35	ns

V_{CC} = 5V ± 5%

TIMING WAVEFORM OF READ CYCLE

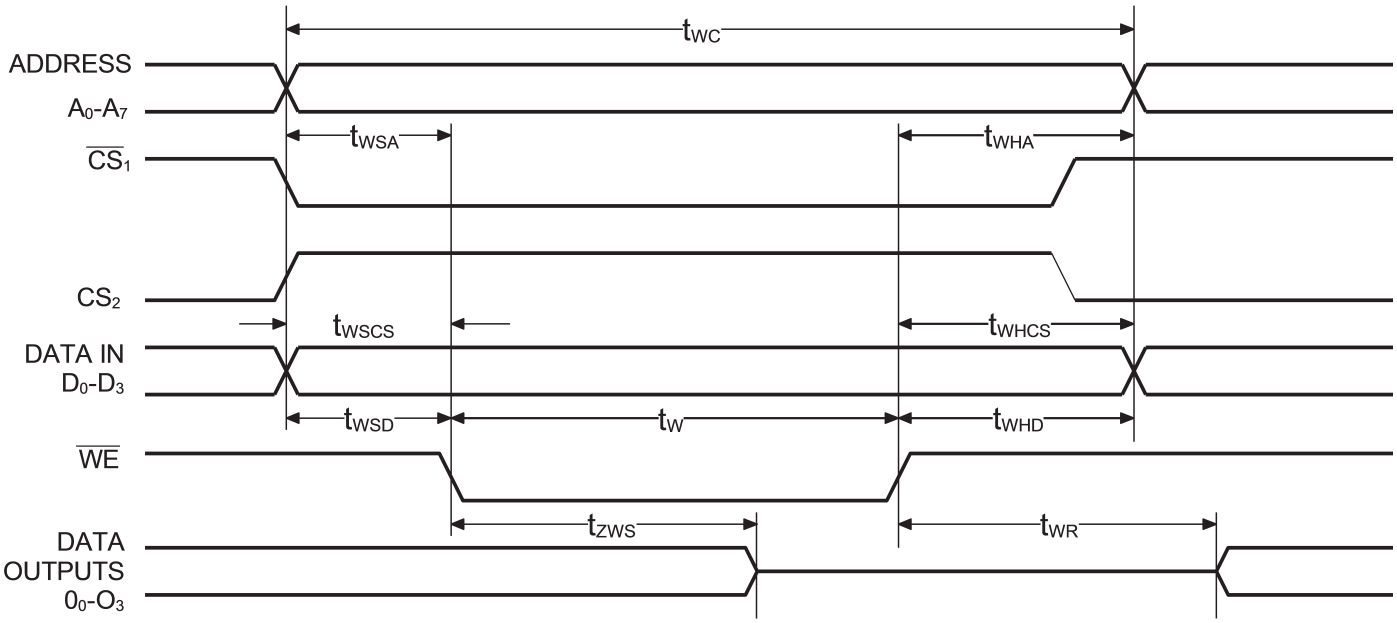


AC CHARACTERISTICS—WRITE CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym	Parameter	-10*		-12		-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time[5]	10		12		15		20		25		35		ns
t_{ZWS}	Write Enable to High-Z[6]		8		10		12		15		20		30	ns
t_{WR}	Write Recovery Time		8		10		12		15		20		25	ns
t_{W}	Write Pulse Width[5,7]	8		9		11		13		15		20		ns
t_{WSD}	Data Setup Time Prior to Write[5]	0		0		0		2		5		5		ns
t_{WHD}	Data Hold Time[5]	2		2		2		5		5		5		ns
t_{WSA}	Address Setup Time[5]	0		0		0		2		5		5		ns
t_{WHA}	Address Hold Time[5]	2		2		4		5		5		5		ns
t_{WSCS}	Chip Select Setup Time[5]	0		0		0		2		5		5		ns
t_{WHCS}	Chip Select Hold Time[5]	2		2		2		5		5		5		ns

TIMING WAVEFORM OF WRITE CYCLE



Notes:
10. $\overline{CE}$ and $\overline{WE}$ must be LOW for WRITE cycle.
11. $\overline{OE}$ is LOW for this WRITE cycle to show t_{WZ} and t_{OW}.
12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state
13. Write Cycle Time is measured from the last valid address to the first transitioning address.

AC TEST LOADS & WAVEFORMS

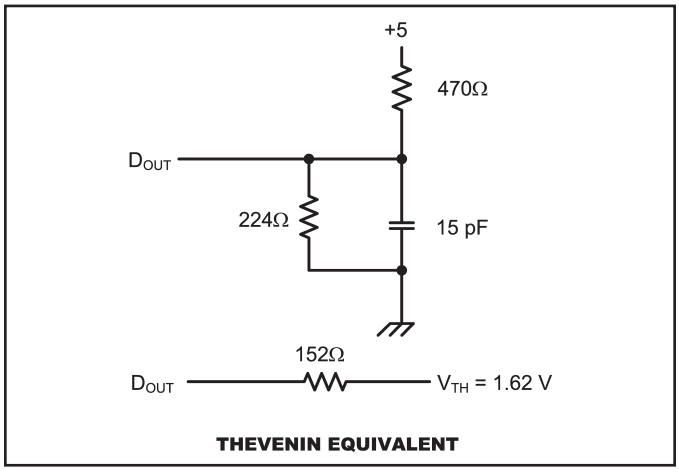


Figure 1A

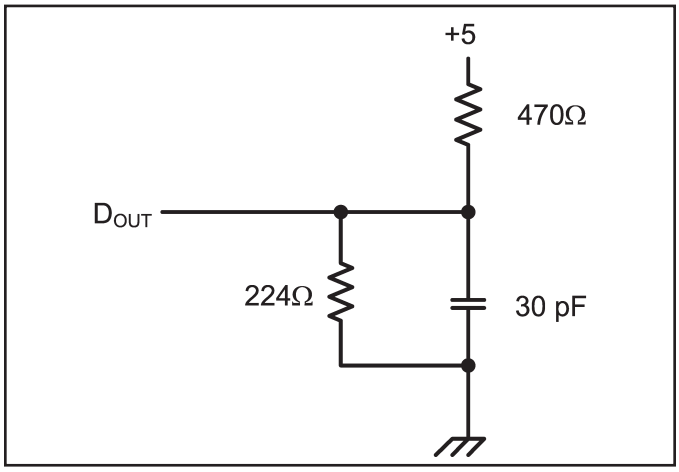


Figure 1B

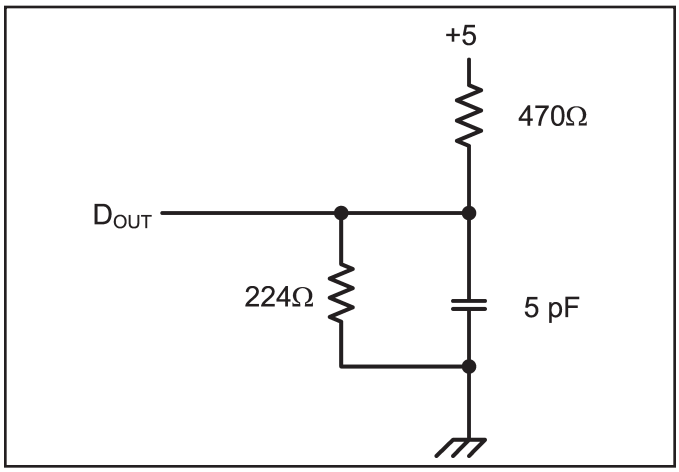


Figure 1C

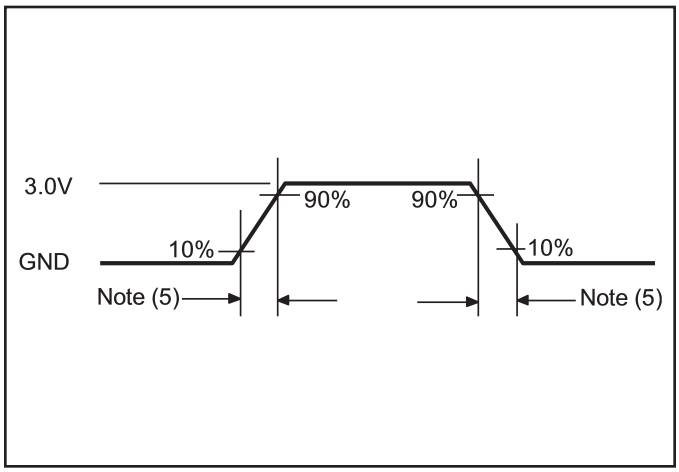
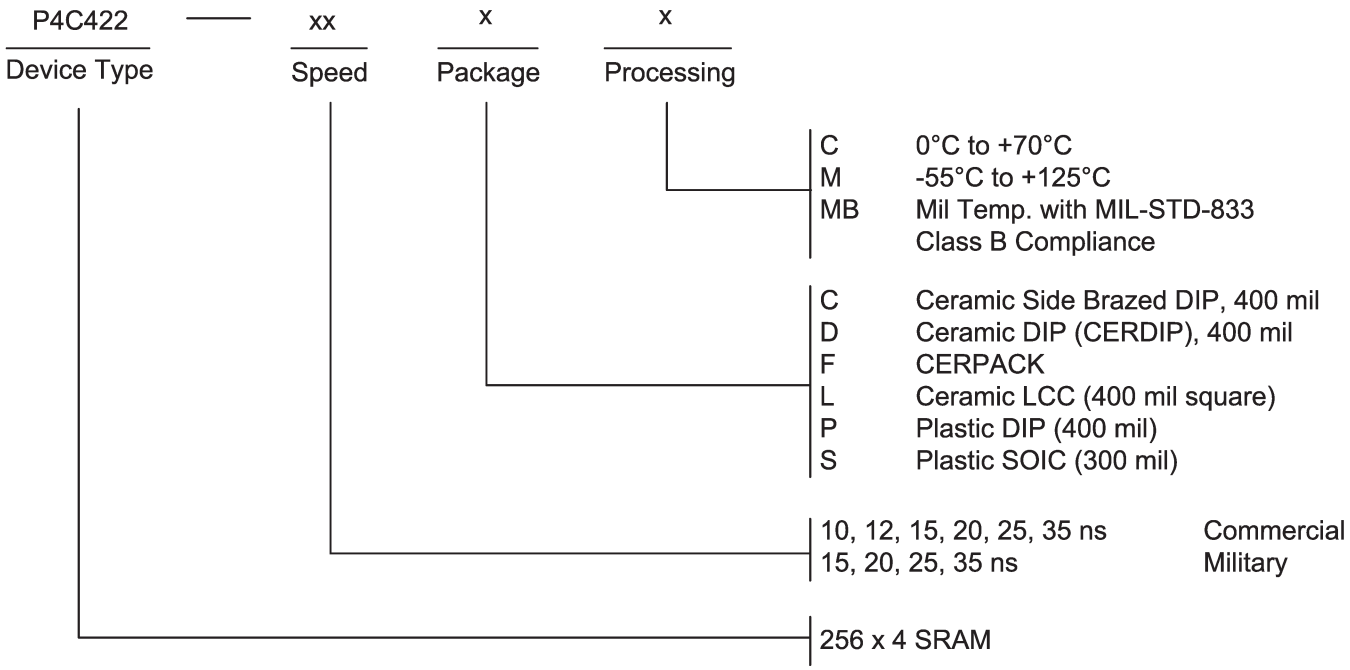


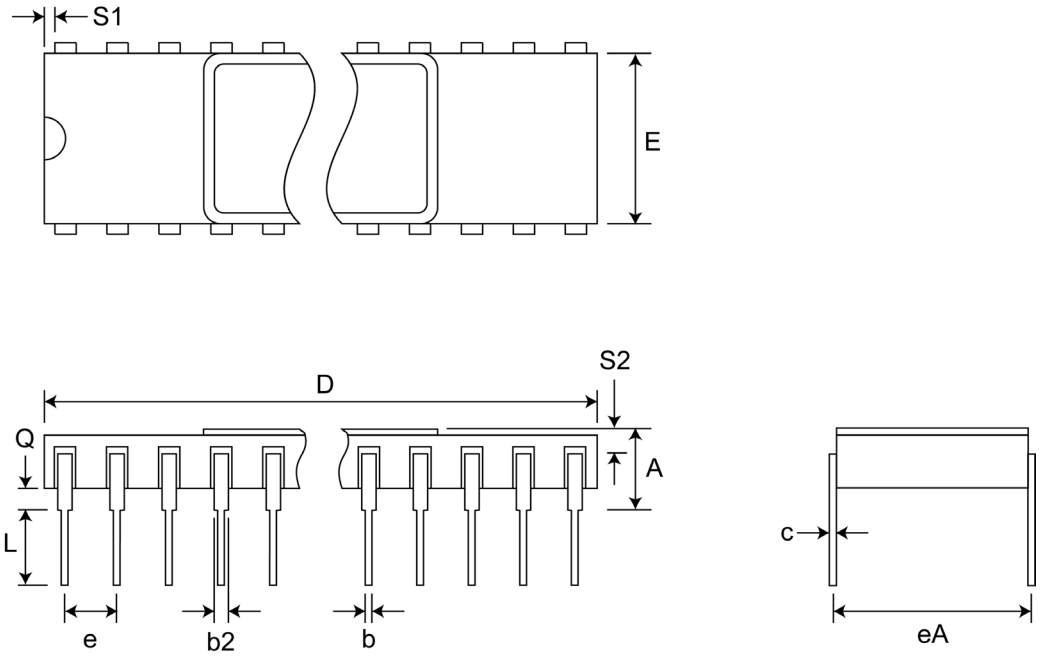
Figure 1D

ORDERING INFORMATION



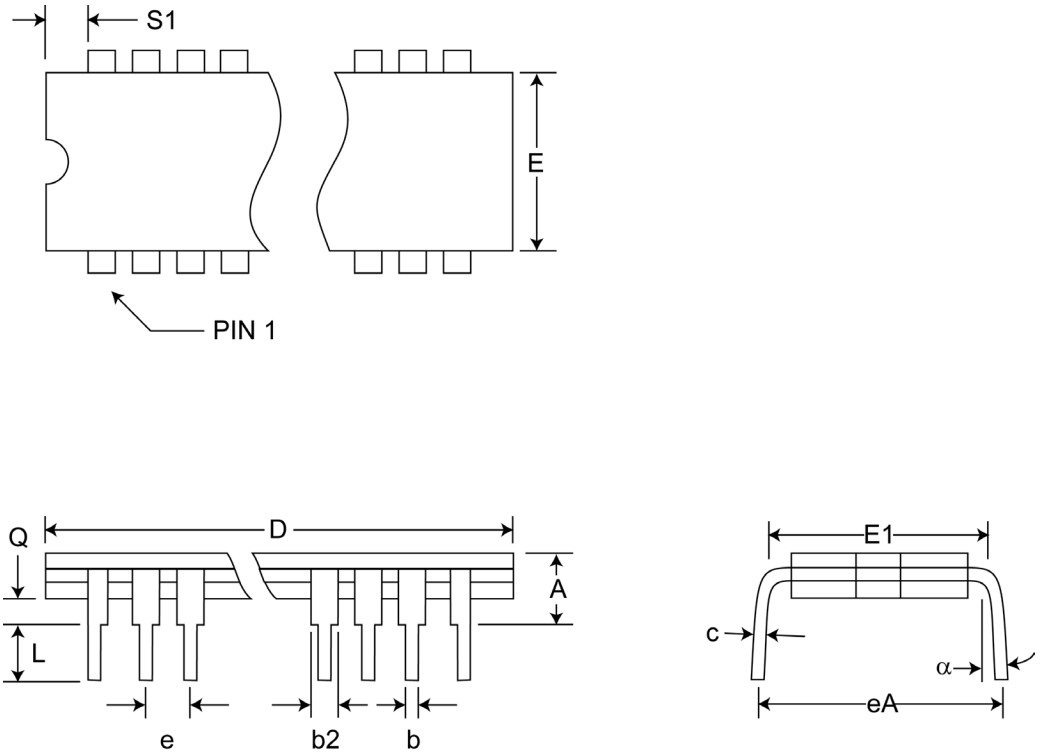
Pkg #	C3-1	
# Pins	22 (400 Mil)	
Symbol	**Min**	**Max**
A	-	0.200
b	0.014	0.026
b2	0.035	0.060
C	0.008	0.015
D	-	1.100
E	0.360	0.410
eA	0.400 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
S2	0.005	-

SIDEBRAZED DUAL IN-LINE PACKAGE



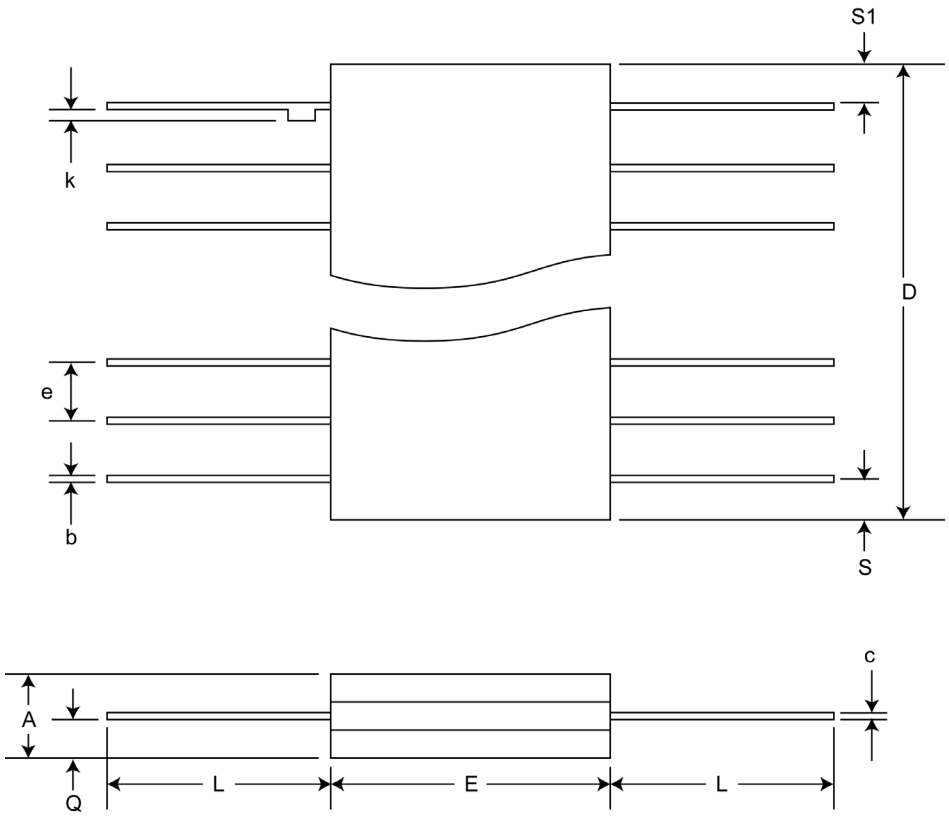
Pkg #	D3-1	
# Pins	22 (400 Mil)	
Symbol	**Min**	**Max**
A	-	0.225
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.111
E	0.350	0.410
eA	0.400 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	-
α	0°	15°

CERDIP DUAL IN-LINE PACKAGE



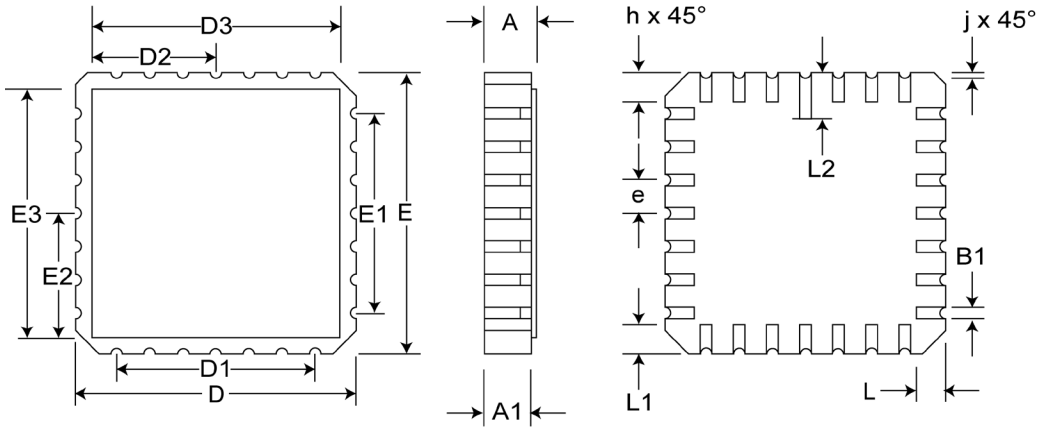
Pkg #	F3	
# Pins	24	
Symbol	**Min**	**Max**
A	0.060	0.090
b	0.015	0.022
c	0.004	0.009
D	-	0.630
E	0.330	0.380
e	0.050 BSC	
k	0.008	0.015
L	0.250	0.370
Q	0.026	0.045
S	-	0.085
S1	0.005	-

CERPACK CERAMIC FLAT PACKAGE



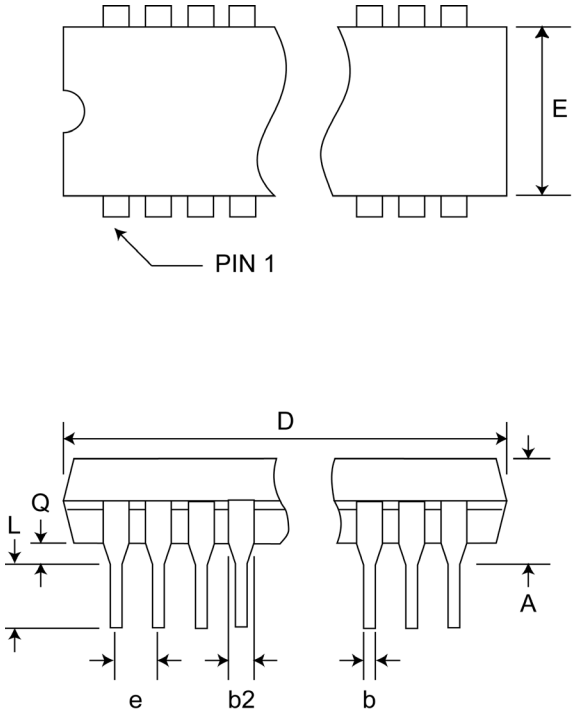
Pkg #	L4	
# Pins	24	
Symbol	**Min**	**Max**
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D/E	0.395	0.410
D1/E1	0.250 BSC	
D2/E2	0.125 BSC	
D3/E3	-	0.410
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	6	
NE	6	

SQUARE LEADLESS CHIP CARRIER



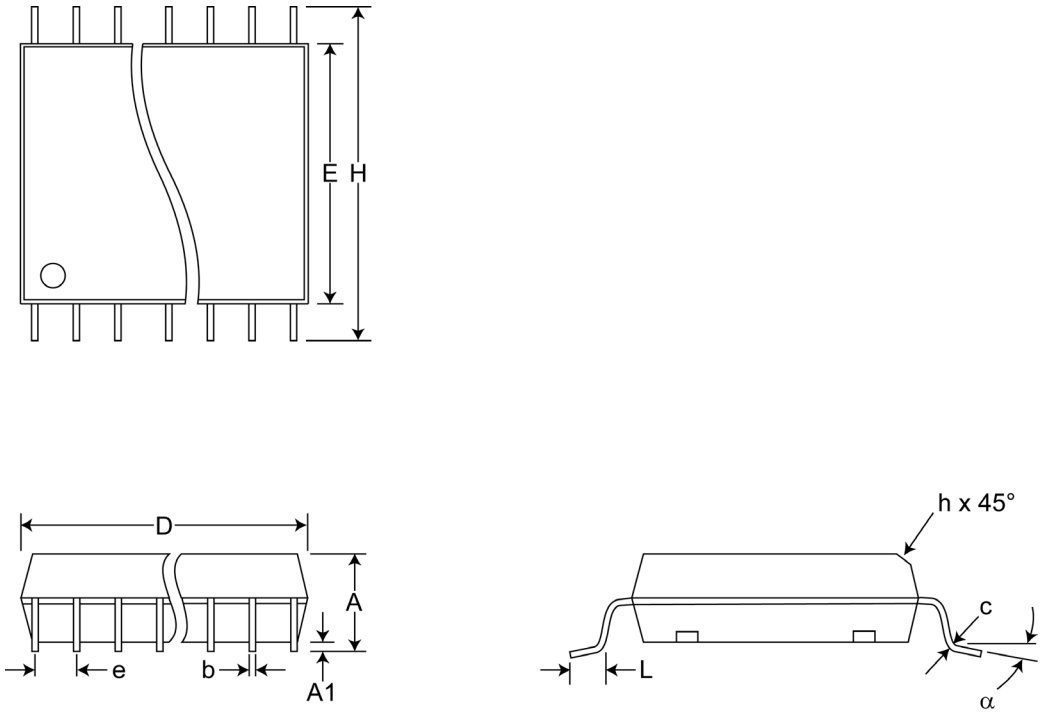
Pkg #	P3-1	
# Pins	22 (400 Mil)	
Symbol	**Min**	**Max**
A	-	0.210
A1	0.015	-
b	0.014	0.022
b2	0.045	0.065
C	0.009	0.015
D	1.065	1.120
E1	0.330	0.390
E	0.390	0.425
e	0.100 BSC	
eB	-	0.500
L	0.115	0.160
α	0°	15°

PLASTIC DUAL IN-LINE PACKAGE



Pkg #	S4	
# Pins	24 (300 Mil)	
Symbol	**Min**	**Max**
A	0.093	0.104
A1	0.004	0.012
b2	0.013	0.020
C	0.009	0.012
D	0.598	0.614
e	0.050 BSC	
E	0.291	0.299
H	0.394	0.419
h	0.010	0.029
L	0.016	0.050
α	0°	8°

SMALL OUTLINE IC PLASTIC PACKAGE



REVISIONS

DOCUMENT NUMBER	SRAM 101
DOCUMENT TITLE	P4C422 - HIGH SPEED 256 X 4 STATIC CMOS RAM

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	1997	DAB	New Data Sheet
A	Oct-2005	JDB	Changed logo to Pyramid
B	Aug-2009	JDB	Corrected DC Electrical Characteristics table