SUPERSEDES DATA OF APRIL 1988

DUAL NON-RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

FEATURES

- Pulse width variance is typically less than ± 5%
- Pin-out identical to "123"
- Overriding reset terminates output pulse
- nB inputs have hysteresis for improved noise immunity
- Output capability: standard (except for nR_{EXT}/C_{EXT})
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT221 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT221 are dual non-retriggerable monostable multivibrators. Each multivibrator features an active LOW-going edge input ($n\overline{A}$) and an active HIGH-going edge input (nB), either of which can be used as an enable input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the nB inputs allow jitter-free triggering from inputs with slow transition rates, providing the circuit with excellent noise immunity.

Once triggered, the outputs (nQ, $n\overline{Q}$) are independent of further transitions of $n\overline{A}$ and nB inputs and are a function of the timing components. The output pulses can be terminated by the overriding active LOW reset inputs ($n\overline{R}_D$). Input pulses may be of any duration relative to the output pulse.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications pulse stability will only be limited by the accuracy of the external timing components.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL} t_{PLH}	propagation delay $n\overline{A}$, nB, $n\overline{R}_D$ to nQ, $n\overline{Q}$ $n\overline{A}$, nB, $n\overline{R}_D$ to nQ, $n\overline{Q}$	C_L = 15 pF V_{CC} = 5 V R_{EXT} = 5 kΩ C_{EXT} = 0 pF	29 35	32 36	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	90	96	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) + 0.33 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 28 \times V_{CC}$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_{EXT} = timing capacitance in pF
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   D = duty factor in %
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	$1\overline{A}$, $2\overline{A}$	trigger inputs (negative-edge triggered)
2, 10	1B, 2B	trigger inputs (positive-edge triggered)
3, 11	$1\overline{R}_D$, $2\overline{R}_D$	direct reset inputs (active LOW)
4, 12	$1\overline{Q}$, $2\overline{Q}$	outputs (active LOW)
7	$2R_{EXT}/C_{EXT}$	external resistor/capacitor connection
8	GND	ground (0 V)
13, 5	1Q, 2Q	outputs (active HIGH)
14, 6	$1C_{EXT}$, $2C_{EXT}$	external capacitor connection
15	$1R_{EXT}/C_{EXT}$	external resistor/capacitor connection
16	V_{CC}	positive supply voltage

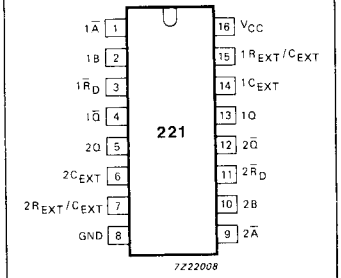

Fig. 1 Pin configuration.

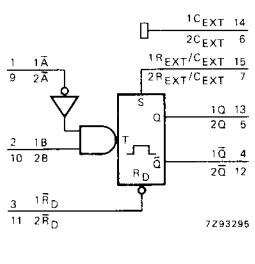

Fig. 2 Logic symbol.

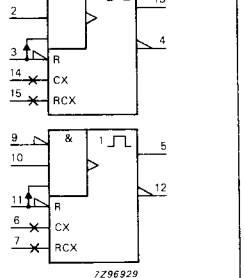

Fig. 3 IEC logic symbol.

GENERAL DESCRIPTION

The output pulse width is defined by the following relationship:

$t_W = C_{EXT}R_{EXT}ln2$
$t_W = 0.7C_{EXT}R_{EXT}$

Pin assignments for the "221" are identical to those of the "123" so that the "221" can be substituted for those products in systems not using the retrigger by merely changing the value of R_{EXT} and/or C_{EXT}.

FUNCTION TABLE

INPUTS			OUTPUTS	
$n\overline{R}_D$	$n\overline{A}$	nB	nQ	$n\overline{Q}$
L	X	X	L	H
X	H	X	L (1)	H (1)
X	X	L	L (1)	H (1)
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍ (2)	⎍ (2)

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level
↓ = HIGH-to-LOW level
⎍ = one HIGH-level output pulse
⎍ = one LOW-level output pulse

Notes to the function table

1. If the monostable was triggered before this condition was established the pulse will continue as programmed.
2. For this combination the reset input must be LOW and the following sequence must be used: pin 1 (or 9) must be set HIGH or pin 2 (or 10) set LOW; then pin 1 (or 9) must be LOW and pin 2 (or 10) set HIGH. Now the reset input goes from LOW-to-HIGH and the device will be triggered.

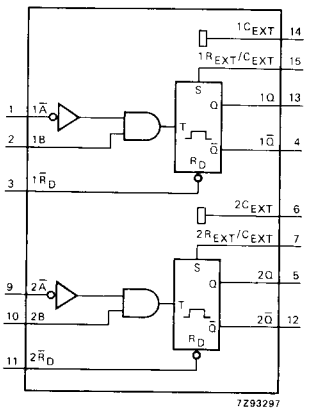

Fig. 4 Functional diagram.

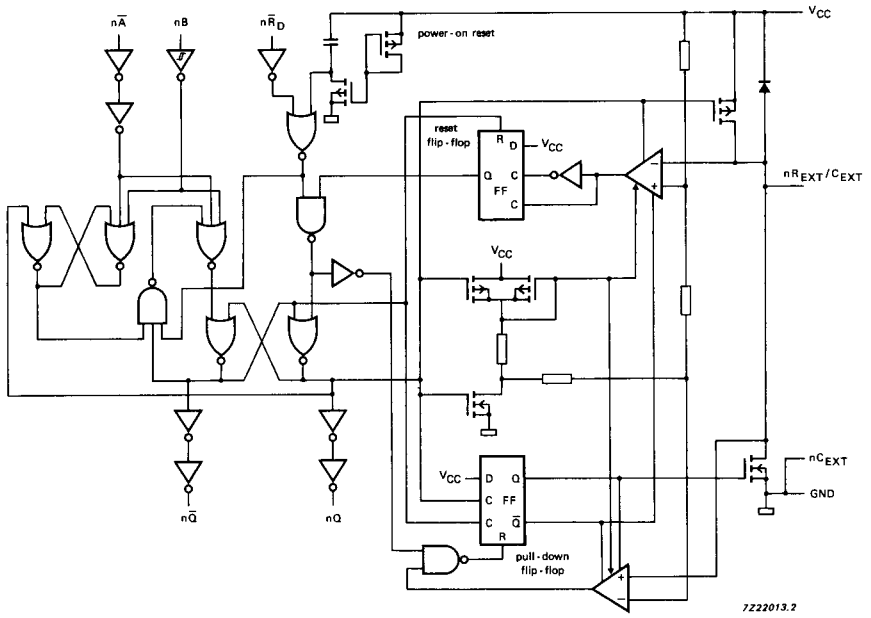

Fig. 5 Logic diagram.

Note

It is recommended to ground pins 6 ($2C_{EXT}$) and 14 ($1C_{EXT}$) externally to pin 8 (GND).

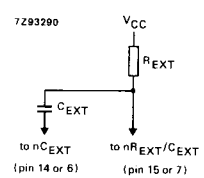

Fig. 6 Timing component connections.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except nR_{EXT}/C_{EXT})
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PLH}	propagation delay (trigger) nA, nB to nQ		72 26 21	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 10
t_{PLH}	propagation delay (trigger) $n\overline{R}_D$ to nQ		80 29 23	245 49 42		305 61 52		370 74 63	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 10
t_{PHL}	propagation delay (trigger) nA, nB to $n\overline{Q}$		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 10
t_{PHL}	propagation delay (trigger) $n\overline{R}_D$ to $n\overline{Q}$		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6,0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 10
t_{PLH}	propagation delay (reset) $n\overline{R}_D$ to $n\overline{Q}$		66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 11
t_{PHL}	propagation delay (reset) $n\overline{R}_D$ to nQ		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 11
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 10
t_W	trigger pulse width nA = LOW	75 15 13	25 9 7		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 7
t_W	trigger pulse width nB = HIGH	90 18 15	30 11 9		115 23 20		135 27 23		ns	2.0 4.5 6.0	Fig. 7
t_W	trigger pulse width $n\overline{R}_D$ = LOW	75 15 13	25 9 7		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 8
t_W	output pulse width $n\overline{Q}$ = LOW nQ = HIGH	630	700	770	602	798	595	805	μs	5.0	C_{EXT} = 100 nF; R_{EXT} = 10 kΩ; Fig. 10
t_W	output pulse width nQ or $n\overline{Q}$		140		–		–		ns	2.0 4.5 6.0	C_{EXT} = 28 pF; R_{EXT} = 2 kΩ; Fig. 10
t_W	output pulse width nQ or $n\overline{Q}$		1.5		–		–		μs	2.0 4.5 6.0	C_{EXT} = 1 nF; R_{EXT} = 2 kΩ; Fig. 10
t_W	output pulse width nQ or $n\overline{Q}$		7		–		–		μs	2.0 4.5 6.0	C_{EXT} = 1 nF; R_{EXT} = 10 kΩ; Fig. 10
t_W	pulse width match between circuits in the package		±2		–		–		%	4.5 to 5.5	C_{EXT} = 1000 pF; R_{EXT} = 10 kΩ

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{rem}	removal time $n\overline{R}_D$ to $n\overline{A}$ or nB	100 20 17	30 11 9		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9
R_{EXT}	external timing resistor	10 2		1000 1000	– –		– –		kΩ	2.0 5.0	Fig. 12 Fig. 13
C_{EXT}	external timing capacitor	no limits							pF	2.0 5.0	Fig. 12 Fig. 13

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except for nR_{EXT}/C_{EXT})
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nB	0.30
$n\overline{A}$	0.50
$n\overline{R}_D$	0.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PLH}	propagation delay (trigger) nA, $n\overline{R}_D$ to nQ		30	50		63		75	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 10
t_{PLH}	propagation delay (trigger) nB to nQ		24	42		53		63	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 10
t_{PHL}	propagation delay (trigger) $n\overline{A}$ to $n\overline{Q}$		26	44		55		66	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 10
t_{PHL}	propagation delay (trigger) nB to $n\overline{Q}$		21	35		44		53	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 10
t_{PHL}	propagation delay (trigger) $n\overline{R}_D$ to $n\overline{Q}$		26	43		54		65	ns	4.5	C_{EXT} = 0 pF R_{EXT} = 5 kΩ; Fig. 10
t_{PHL}	propagation delay (reset) $n\overline{R}_D$ to nQ		26	43		54		65	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 11
t_{PLH}	propagation delay (reset) $n\overline{R}_D$ to $n\overline{Q}$		31	51		64		77	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 11

AC CHARACTERISTICS FOR 74HCT

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 10
t_W	trigger pulse width nA = LOW	20	13		25		30		ns	4.5	Fig. 10
t_W	trigger pulse width nB = HIGH	20	13		25		30		ns	4.5	Fig. 10
t_W	pulse width $n\overline{R}_D$ = LOW	22	13		28		33		ns	4.5	Fig. 8
t_W	output pulse width $n\overline{Q}$ = LOW nQ = HIGH	630	700	770	602	798	595	805	μs	5.0	C_{EXT} = 100 nF; R_{EXT} = 10 kΩ; Fig. 10
t_W	trigger pulse width nQ or $n\overline{Q}$		140		–		–		ns	4.5	C_{EXT} = 28 pF; R_{EXT} = 2 kΩ; Fig. 10
t_W	trigger pulse width nQ or $n\overline{Q}$		1.5		–		–		μs	4.5	C_{EXT} = 1 nF; R_{EXT} = 2 kΩ; Fig. 10
t_W	trigger pulse width nQ or $n\overline{Q}$		7		–		–		μs	4.5	C_{EXT} = 1 nF; R_{EXT} = 10 kΩ; Fig. 10
t_{rem}	removal time $n\overline{R}_D$ to nA or nB	20	12		25		30		ns	4.5	Fig. 9
R_{EXT}	external timing resistor	2		1000	–		–		kΩ	5.0	Fig. 13
C_{EXT}	external timing capacitor	no limits							pF	5.0	Fig. 13

AC WAVEFORMS

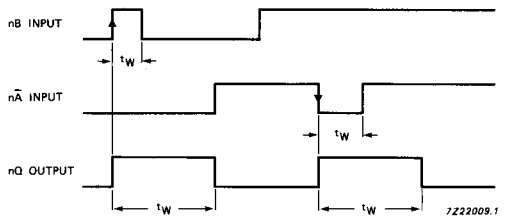

Fig. 7 Output pulse control; $n\overline{R}_D$ = HIGH.

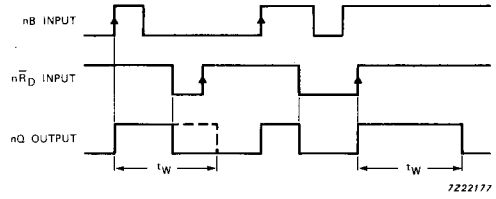

Fig. 8 Output pulse control using reset input $n\overline{R}_D$; nĀ = LOW.

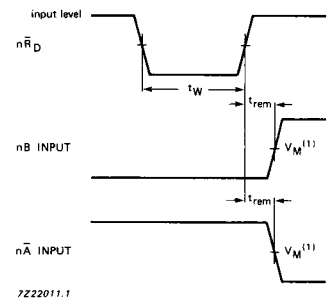

Fig. 9 Waveforms showing the removal times; $n\overline{R}_D$ to nĀ or nB.

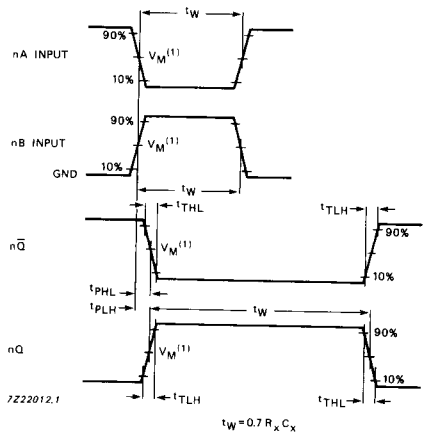

Fig. 10 Waveforms showing the triggering of One Shot by input $n\overline{A}$ or input nB for one period (t_W) and minimum pulse widths of the trigger inputs $n\overline{A}$ and nB.

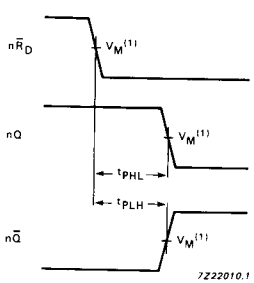

Fig. 11 Waveforms showing the reset to nQ and $n\overline{Q}$ output propagation delays.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

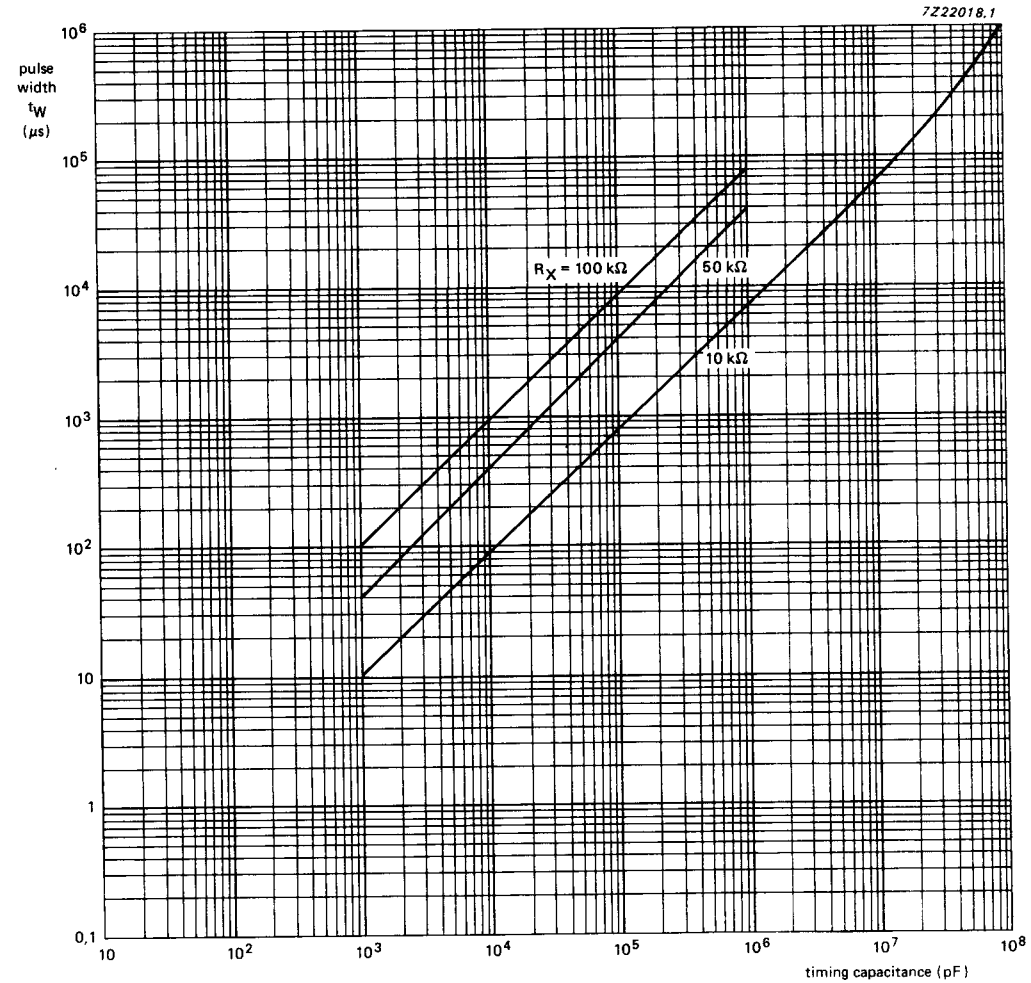

Fig. 12 HC typical output pulse width as a function of timing capacitance (V_{CC} = 2 V).

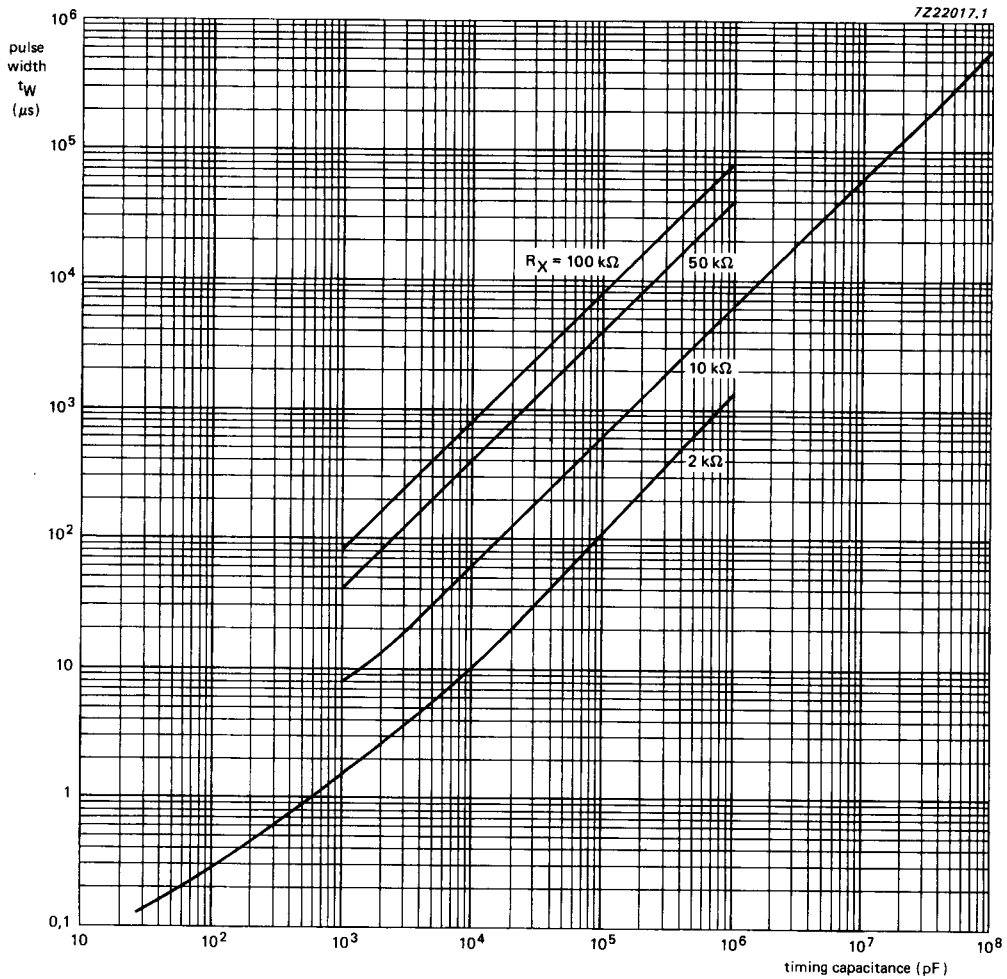

Fig. 13 HC/HCT typical output pulse width as a function of timing capacitance (V_{CC} = 4.5 V).

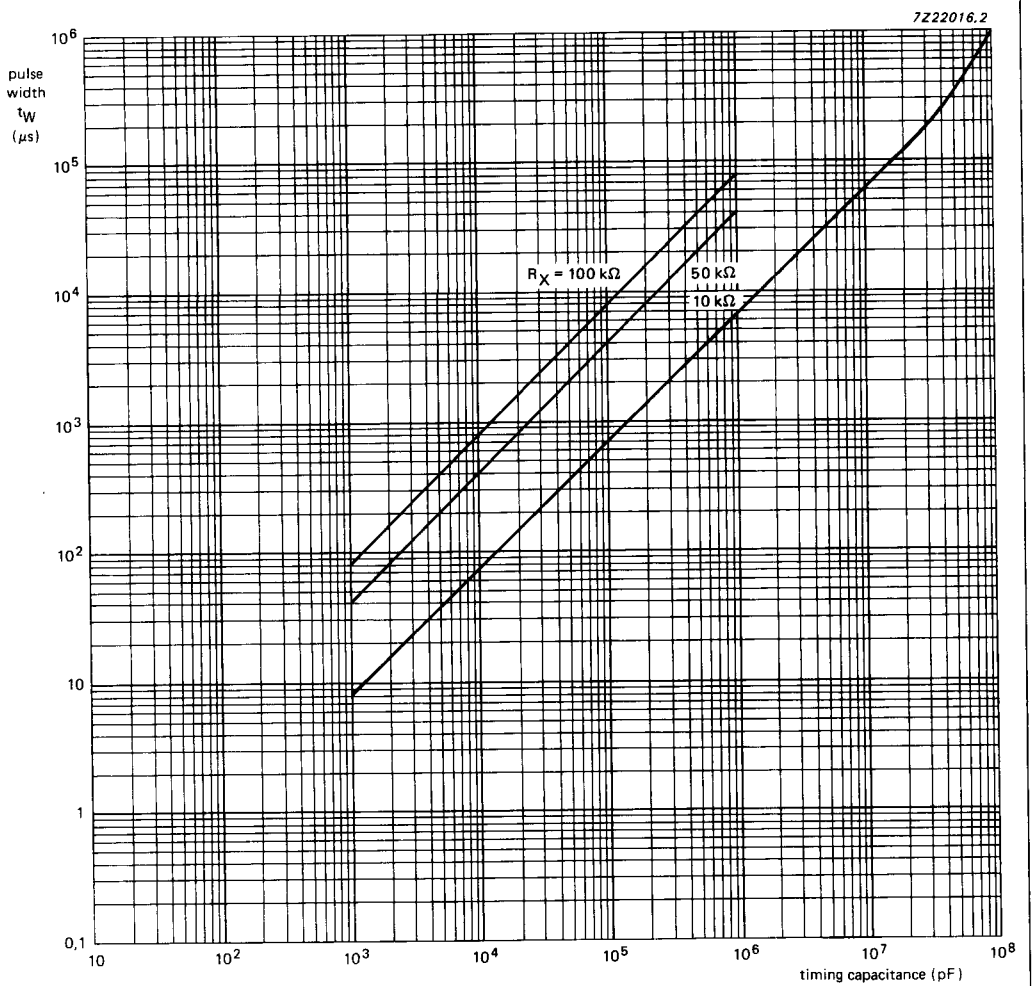

Fig. 14 HC typical output pulse width as a function of timing capacitance (V_{CC} = 6 V).

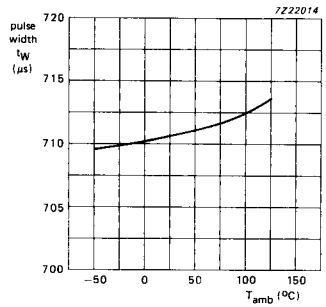

Fig. 15 Typical output pulse width as a function of temperature; C_X = 0.1 μF; R_X = 10 KΩ; V_{CC} = 5 V.

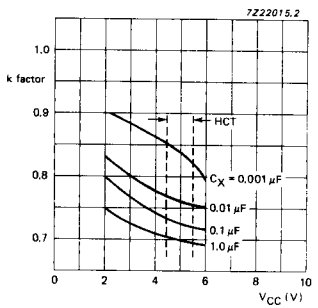

Fig. 16 k factor as a function of supply voltage; R_X = 10 KΩ; T_{amb} = 25 °C.

Power-down consideration

A large capacitor (C_X) may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may substain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_X) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Fig. 17.

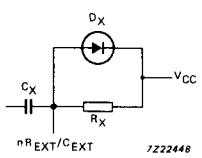

Fig. 17 Power-down protection circuit.