T-77-07-13

Video analog input interface

TDA8709

FEATURES

- 8-bit resolution
- Sampling rate up to 30 MHz
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Low level AC clock inputs and outputs
- Clamp function with selection for '16' or '128'
- No sample-and-hold circuit required
- Three selectable video inputs

APPLICATIONS

- Video signal processing
- Digital picture processing
- Frame grabbing
- Colour difference signals (U, V)
- Y, R, G, B signals
- Chrominance signal (C)

DESCRIPTION

The TDA8709 is a bipolar analog input interface for video signal processing. It includes an input selector (1 out of three video signals), video amplifier with clamp and external gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 30 MHz.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	40	47	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±1/2	LSB
f_{CLK}	maximum clock frequency	30	–	–	MHz
B	maximum –3 dB bandwidth (preamplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	380	512	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8709	28	DIL	plastic	SOT117
TDA8709T	28	SO28	plastic	SOT136A

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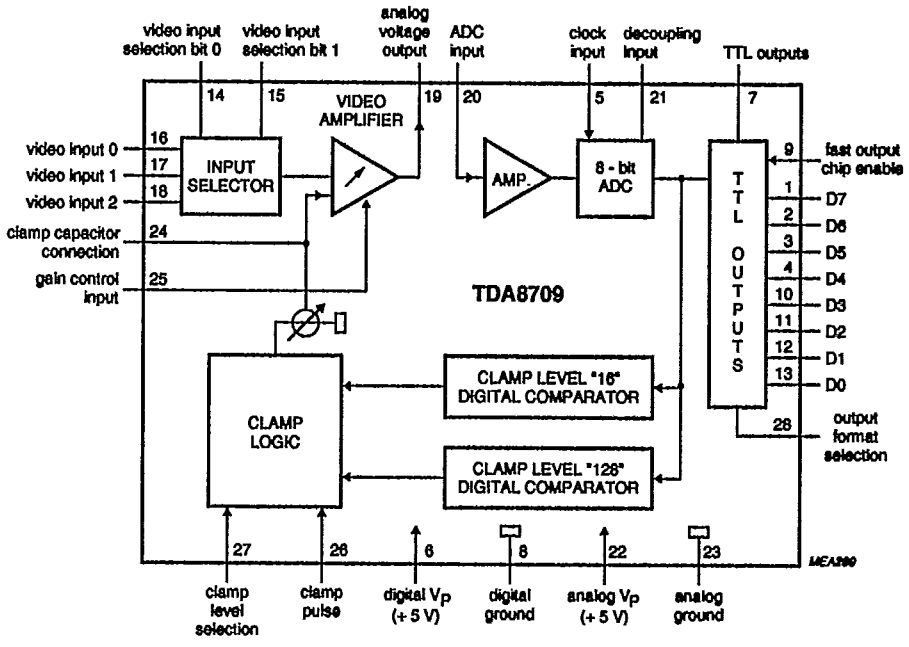

Fig.1 Block diagram.

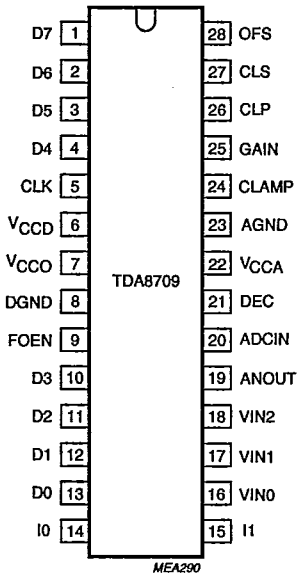

Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output, bit 7 (MSB)
D6	2	data output, bit 6
D5	3	data output, bit 5
D4	4	data output, bit 4
CLK	5	clock input
V_{CCD}	6	digital positive supply voltage (+5 V)
V_{CCO}	7	TTL outputs positive supply voltage (+5 V)
DGND	8	digital ground
FOEN	9	fast output chip enable
D3	10	data output, bit 3
D2	11	data output, bit 2
D1	12	data output, bit 1
D0	13	data output, bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog positive supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
GAIN	25	gain control input
CLP	26	clamp pulse
CLS	27	clamp level selection
OFS	28	output format selection

FUNCTIONAL DESCRIPTION

The TDA8709 is an 8-bit ADC with internal clamping and a preamplifier with adjustable gain.

The clamping value is switched via pin 27 between digital 16 (for luminance or R, G, B signals) and digital 128 (for chrominance or colour difference signals). While clamping pulse at pin 27 is logic 1, the device will adjust the clamp level to the chosen value. The output format can be selected between binary and two's complement at pin 28.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	−0.3	+7.0	V
V_{CCD}	digital supply voltage range	−0.3	+7.0	V
V_{CCO}	output supply voltage range	−0.3	+7.0	V
$V_{CCA} - V_{CCD}$	supply voltage difference	−0.5	+0.5	V
$V_{CCO} - V_{CCD}$	supply voltage difference	−0.5	+0.5	V
$V_{CCA} - V_{CCO}$	supply voltage difference	−1.0	+1.0	V
V_I	input voltage range	−0.3	+7.0	V
I_O	output current	−	+10	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
T_j	junction temperature	0	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air (SOT117)	55 K/W
$R_{th\ j-a}$	from junction to ambient in free air (SOT136A)	70 K/W

CHARACTERISTICS

$V_{CCA} = V_{22} - V_{23} = 4.5$ to 5.5 V; $V_{CCD} = V_6 - V_8 = 4.5$ to 5.5 V; $V_{CCO} = V_7 - V_8 = 4.2$ to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCA} - V_{CCO} = -0.5$ to +0.5 V; $T_{amb} = 0$ to +70 °C; Typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	40	47	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	output supply current	TTL load (see Fig.8)	–	12	16	mA
Preamplifier inputs						
VIN(0-2) INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)		0.3	1	1.6	V
$\|Z_i\|$	input impedance	f = 6 MHz	10	20	–	kΩ
C_I	input capacitance	f = 6 MHz	–	1	–	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	–	20	µA
CLS, OFS, CLP, TTL INPUTS (SEE FIG 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	–	20	µA
GAIN INPUT (PIN 25)						
V_{25}	voltage for minimum gain	see Fig.3	–	1.5	–	V
V_{25}	voltage for maximum gain	see Fig.3	–	4.2	–	V
I_I	input current		–	1.0	–	µA
	stability gain/temperature	see Fig.3	–	6	–	%
CLAMP INPUT (PIN 24)						
I_{24}	CLAMP output current	see Table 2	–	–	–	
Video amplifier outputs						
ANOUT OUTPUT (PIN 19)						
$V_{19(p-p)}$	output AC voltage (peak-to-peak value)	$V_{VIN} = 1$ V (p-p); $V_{25} = 3$ V	–	1.0	–	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	–	mA
$I_{O(p-p)}$	output current driven by the load	$V_{ANOUT} = 1$ V (p-p); note 1	-	-	1.0	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{19}	output DC voltage for black level	CLS = logic 1	–	V_{CCA}–2.65	–	V
V_{19}	output DC voltage for black level	CLS = logic 0	–	V_{CCA}–3.1	–	V
Z_{19}	output impedance		–	20	–	Ω
Preamplifier dynamic characteristics						
α	crosstalk between VIN inputs	note 2	–	–60	–55	dB
G_d	differential gain	V_{VIN} = 1 V (p-p); V_{25} = 3 V	–	2	–	%
ϕ_d	differential phase		–	2	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 3	60	–	–	dB
SVRR	supply voltage ripple rejection	note 4	–	45	–	dB
ΔG	gain range		–4.5	–	10	dB
Analog-to-digital converter inputs						
CLK INPUT (PIN 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	100	μA
$\|Z_i\|$	input impedance	f_{CLK} = 10 MHz	–	4	–	kΩ
C_i	input capacitance	f_{CLK} = 10 MHz	–	4.5	–	pF
FOEN TTL input (see Table 3)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_9 = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_9 = 2.7 V	–	–	+20	μA
ADCIN INPUT (PIN 20) (SEE TABLE 4)						
V_{20}	input voltage	digital out = 00	–	V_{CCA} –1.6	–	V
V_{20}	input voltage	digital out = 255	–	V_{CCA} –1.1	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	0.5	–	V
I_{20}	input current		–	1.0	10	μA
$\|Z_i\|$	input impedance	f = 6 MHz	–	50	–	MΩ
C_i	input capacitance	f = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
DIGITAL OUTPUTS D(0-7)						
V_{OL}	LOW level output voltage	I_O = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_O = –0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics						
f_{CLK}	CLK input maximum frequency	see Fig.6; note 5	30	–	–	MHz
Analog signal processing (f_{CLK} = 30 MHz; see Fig.8)						
G_{diff}	differential gain	V_{20} = 0.5 V (p-p); note 6; see Fig.4	–	2	–	%
ϕ_{diff}	differential phase	note 6; see Fig.4	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 6	–	–	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43 MHz; note 6	–	–55	–	dB
SVRR	supply voltage ripple rejection	note 7	–	1	5	%/V
Transfer function						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 8	–	–	±2	LSB
Timing (f_{CLK} = 30 MHz; see Figs 6, 7 and 8)						
DIGITAL OUTPUTS (C_L = 15 pF; I_{OL} = 2 mA)						
t_{dS}	sampling delay		–	2	–	ns
t_{HD}	output hold time		–	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time - output enable		–	16	25	ns
t_{dDZ}	3-state delay time - output disable		–	12	25	ns

Notes to the characteristics

1. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referred to V_{CC} and is defined as:

   AC impedance ≥ 1 kΩ and DC impedance > 2.7 kΩ

   The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
2. Input signals with the same amplitude. Gain is adjusted to obtain ANOUT = 1 V (p-p)
3. Signal-to-noise ratio measured with 5 MHz bandwidth

$$SN = 20 \log \frac{V_{ANNOUT(p-p)}}{V_{ANNOUT}\ noise\ RMS\ (B = 5\ MHz)}$$

4. The voltage ratio is expressed as:

$$SVRR = 20 \log \frac{\Delta V_{CCA}}{\Delta G/G}$$

   for V_I = 1 V (p-p), 100 kHz gain = 1 and 1 V supply variation.

Notes to the characteristics

5. It is recommended that the rise and fall times of the clock are not less than 2 ns. In addition, a 'good lay-out' for the digital and analog grounds is recommended.
6. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
7. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

$$SVRR = \frac{\Delta[V_{IN(00)} - V_{IN(FF)}] + [V_{IN(00)} - V_{IN(FF)}]}{\Delta V_{CCA}}$$

8. Full-scale sinewave (f_I = 4.4 MHz; f_{CLK}, $f_{\overline{CLK}}$ = 27 MHz).

Table 1 Video input selection (CVBS)

I1	I0	SELECTED INPUT
0	0	VIN0
1	0	VIN2
0	1	VIN1
1	1	VIN1

Table 2 CLAMP output current

CLS	CLP	DIGITAL OUTPUT	I_{CLAMP}
1	1	output < 128 output > 128	+50 µA −50 µA
X	0	X	0
0	1	output < 16 16 < output	+50 µA −50 µA

Table 3 FOEN input current

FOEN	D0 TO D7
0	active
1	high impedance

Note

Where; X = don't care

Table 4 ADC output current

		OFS = 0 BINARY OUTPUTS								OFS = 1 TWO'S COMPLEMENT							
STEP	V_{ADCIN}	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} - 1.6 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1		0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
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254		1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} - 1.1 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow		1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

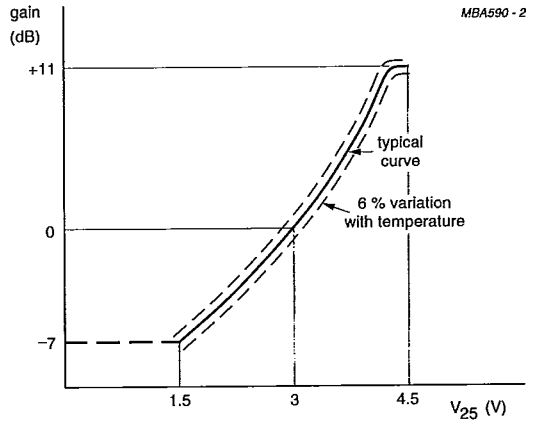


Fig.3 Typical gain control curve as a function of gain voltage.

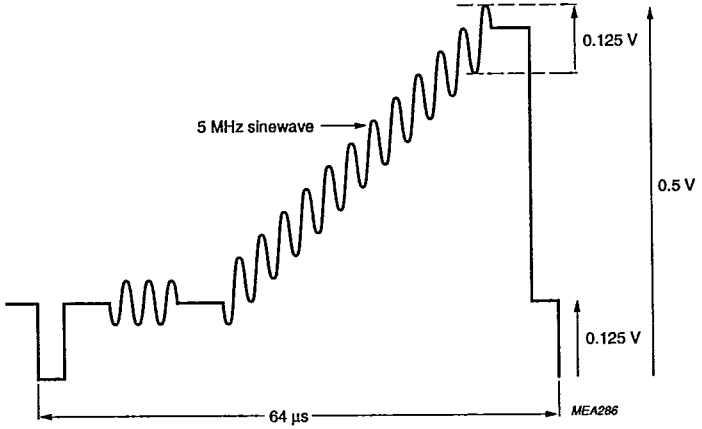


Fig.4 Test signal on the ADCIN pin for differential gain and phase measurements.

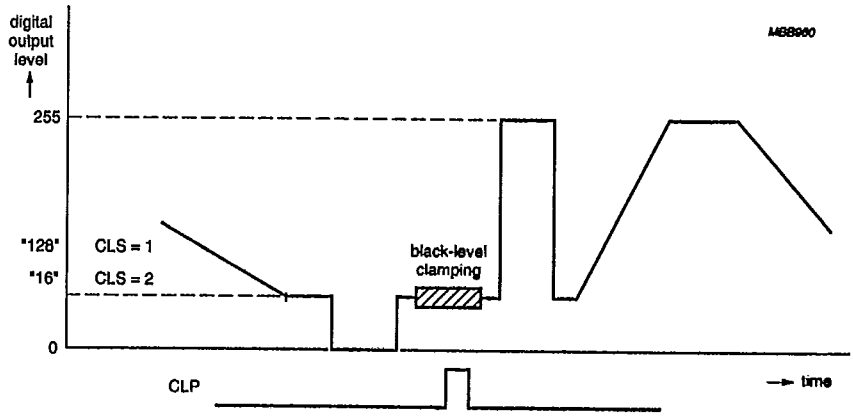


Fig.5 Control mode selection.

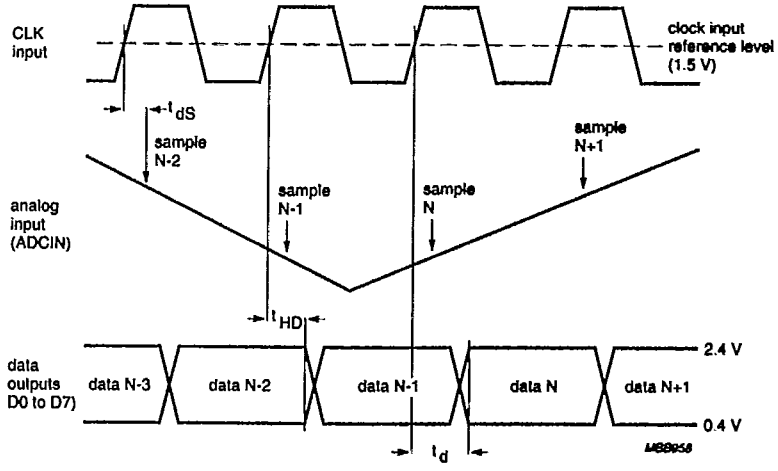


Fig.6 Timing diagram.

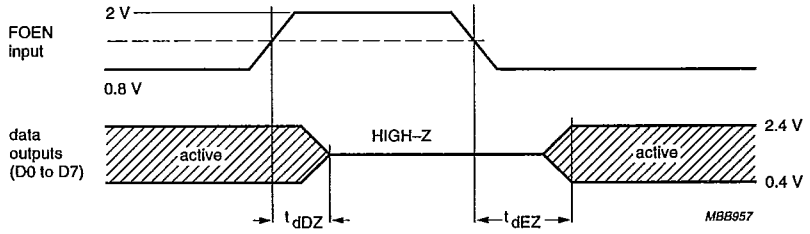


Fig.7 Output format timing diagram.

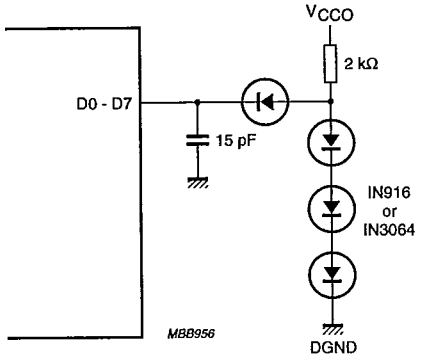


Fig.8 Load circuit for timing measurement; data outputs (FOEN = LOW).

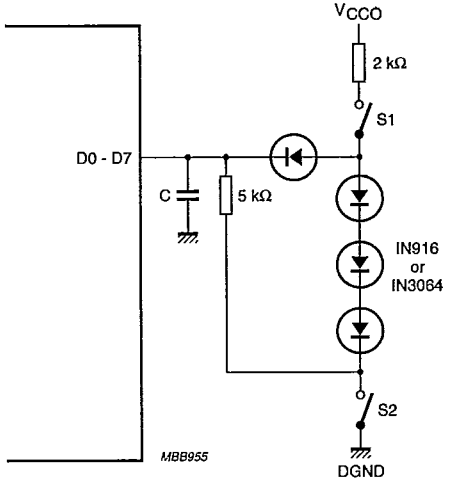


Fig.9 Load circuit for timing measurement; 3-state outputs (FOEN: f_i = 1 MHz; V_{FOEN} = 3 V).

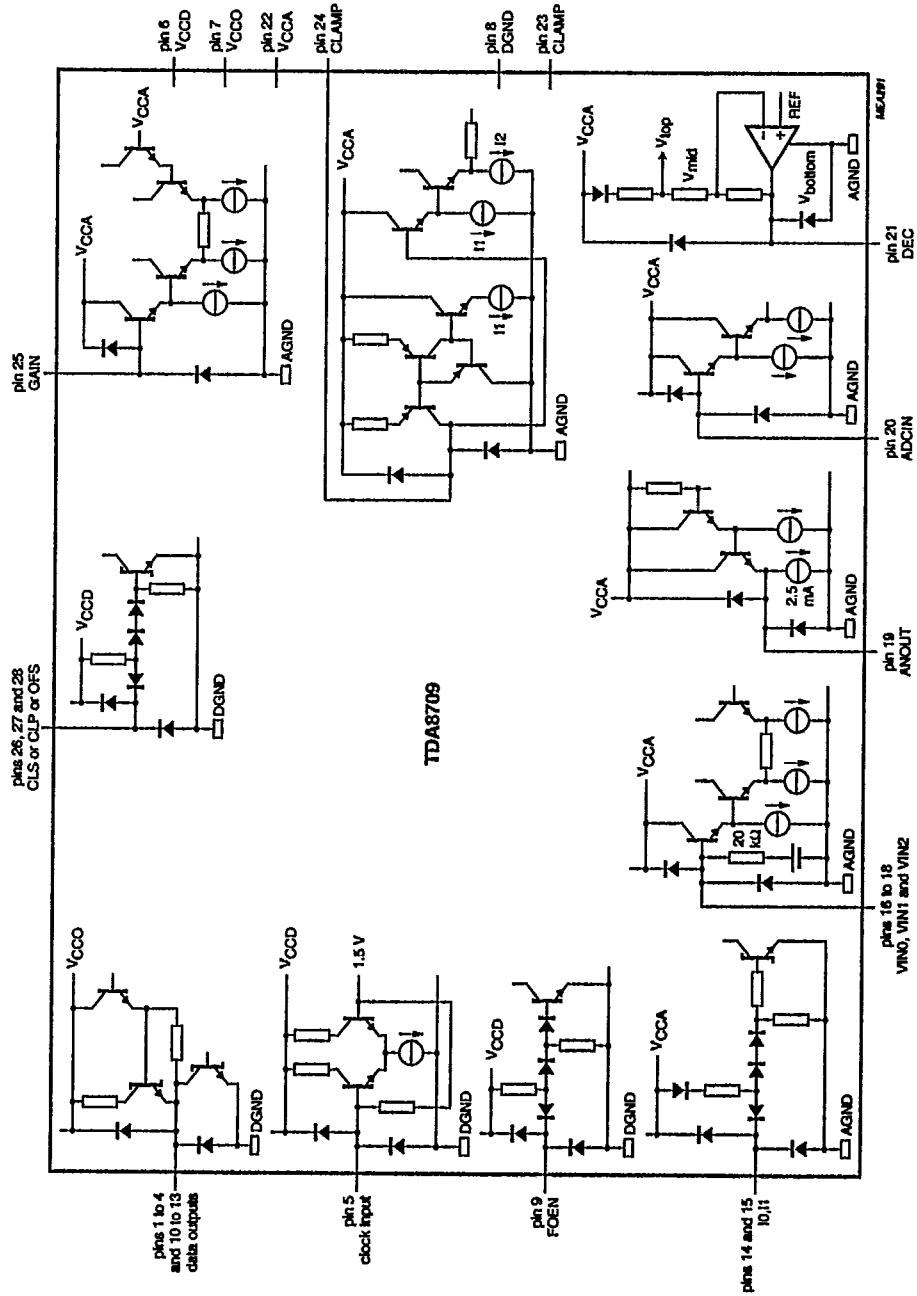
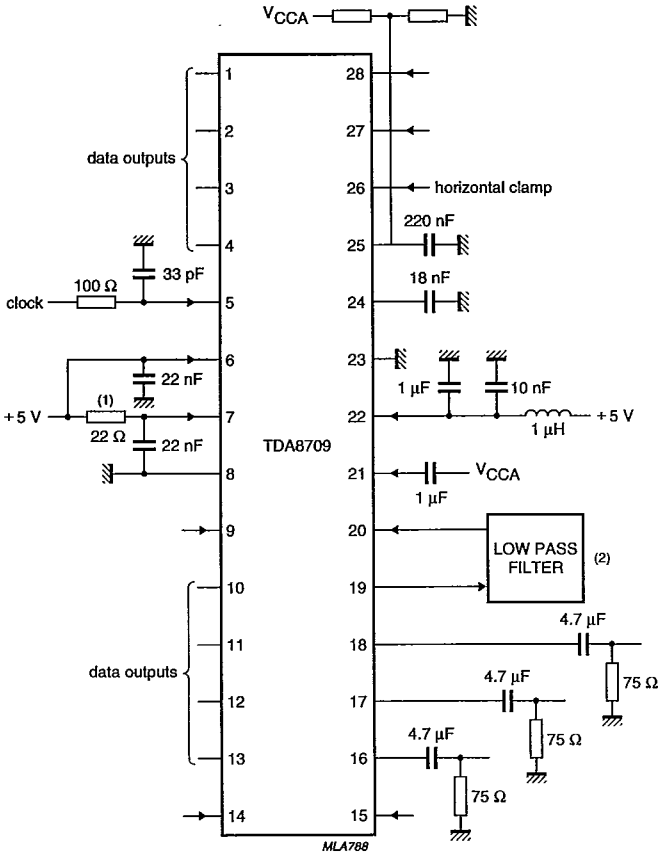


Fig.10 Internal pin configuration.

APPLICATION INFORMATION

Additional information can be found in the laboratory report FTV/9002.



(1) It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of TDA8709 interfaces with a capacitive CMOS load device.

(2) See Figs 12 and 13 for filter examples.

Fig.11 Application diagram.

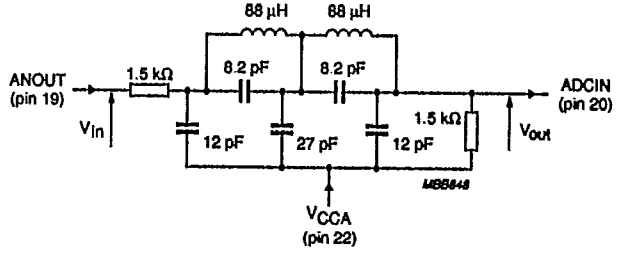


Fig.12 Example of lowpass filter for Y and C signals.

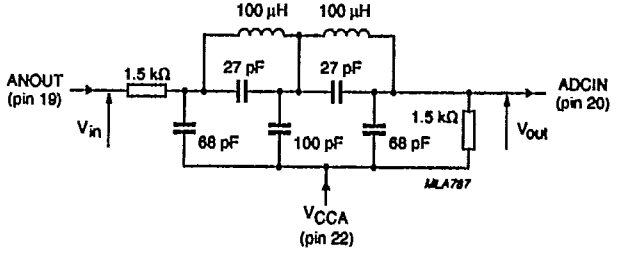


Fig.13 Example of lowpass filter for U, V and RGB signals.

Note to figures 12 and 13

These filters can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 1.5 kΩ must in any case be applied.