NTA4151P, NTE4151P

MOSFET – Single, P-Channel, Small Signal, Gate Zener, SC-75, SC-89

-20 V, -760 mA

Features

- Low $R_{DS(on)}$ for Higher Efficiency and Longer Battery Life
- Small Outline Package (1.6 x 1.6 mm)
- SC−75 Standard Gullwing Package
- ESD Protected Gate
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- High Side Load Switch
- DC−DC Conversion
- Small Drive Circuits
- Battery Operated Systems such as Cell Phones, PDAs, Digital Cameras, etc.

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter		Symbol	Value	Units
Drain−to−Source Voltage		V_{DSS}	−20	V
Gate−to−Source Voltage		V_{GS}	±6.0	V
Continuous Drain Current (Note 1)	Steady State	I_D	−760	mA
Power Dissipation (Note 1) SC−75 SC−89	Steady State	P_D	 301 313	mW
Pulsed Drain Current	tp =10 μs	I_{DM}	±1000	mA
Operating Junction and Storage Temperature		T_J, T_{STG}	−55 to 150	°C
Continuous Source Current (Body Diode)		I_S	−250	mA
Lead Temperature for Soldering Purposes (1/8 in from case for 10 s)		T_L	260	°C
Gate−to−Source ESD Rating − (Human Body Model, Method 3015)		ESD	1800	V

THERMAL RESISTANCE RATINGS

Junction−to−Ambient − Steady State (Note 1) SC−75 SC−89	$R_{\theta JA}$	 415 400	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

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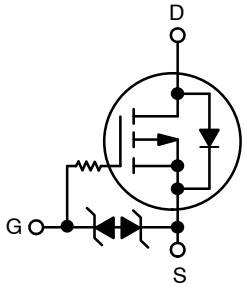
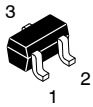
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
−20 V	0.26 Ω @ −4.5 V	−760 mA
	0.35 Ω @ −2.5 V	
	0.49 Ω @ −1.8 V	

P−Channel MOSFET

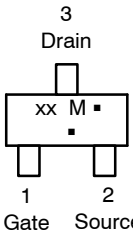


MARKING DIAGRAM & PIN ASSIGNMENT



SC−75 / SOT−416
CASE 463
STYLE 5

SC−89
CASE 463C



xx = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA	−20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −16 V		−1.0	−100	nA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±4.5 V		±1.0	±10	μA
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = −250 μA	−0.45		−1.2	V
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = −4.5 V, I_D = −350 mA		0.26	0.36	Ω
		V_{GS} = −2.5 V, I_D = −300 mA		0.35	0.45	
		V_{GS} = −1.8 V, I_D = −150 mA		0.49	1.0	
Forward Transconductance	g_{FS}	V_{DS} = −10 V, I_D = −250 mA		0.4		S
CHARGES AND CAPACITANCES						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −5.0 V		156		pF
Output Capacitance	C_{OSS}			28		
Reverse Transfer Capacitance	C_{RSS}			18		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DD} = −10 V, I_D = −0.3 A		2.1		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.125		
Gate−to−Source Charge	Q_{GS}			0.325		
Gate−to−Drain Charge	Q_{GD}			0.5		
SWITCHING CHARACTERISTICS (Note 3)						
Turn−On Delay Time	$td_{(ON)}$	V_{GS} = −4.5 V, V_{DD} = −10 V, I_D = −200 mA, R_G = 10 Ω		8.0		ns
Rise Time	t_r			8.2		
Turn−Off Delay Time	$td_{(OFF)}$			29		
Fall Time	t_f			20.4		
DRAIN−SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −250 mA		−0.72	−1.1	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTA4151PT1G	TN	SC−75 (Pb−Free)	3000 / Tape & Reel
NTE4151PT1G	TM	SC−89 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL ELECTRICAL CHARACTERISTICS

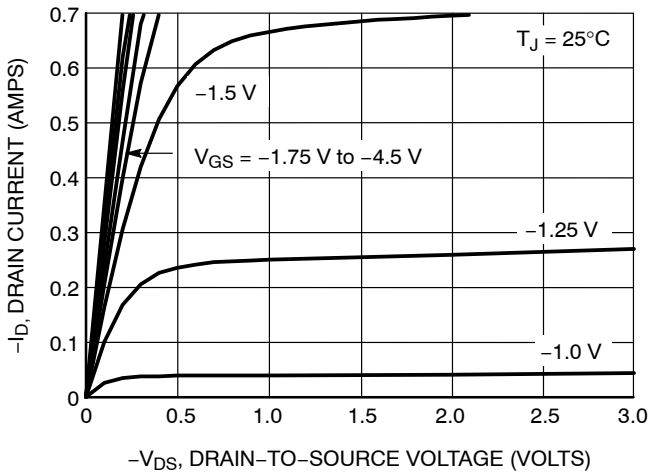


Figure 1. On−Region Characteristics

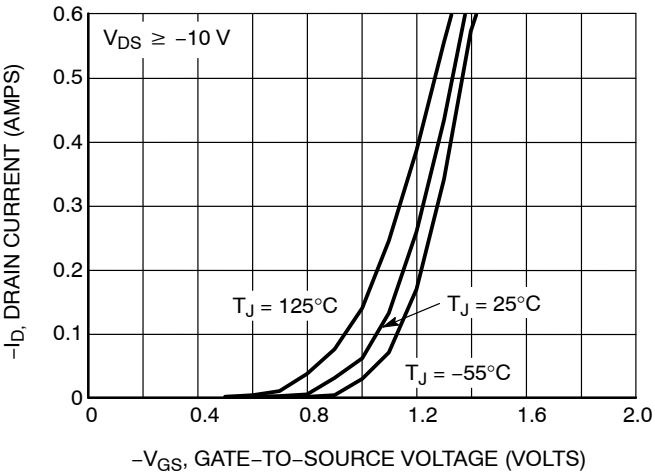


Figure 2. Transfer Characteristics

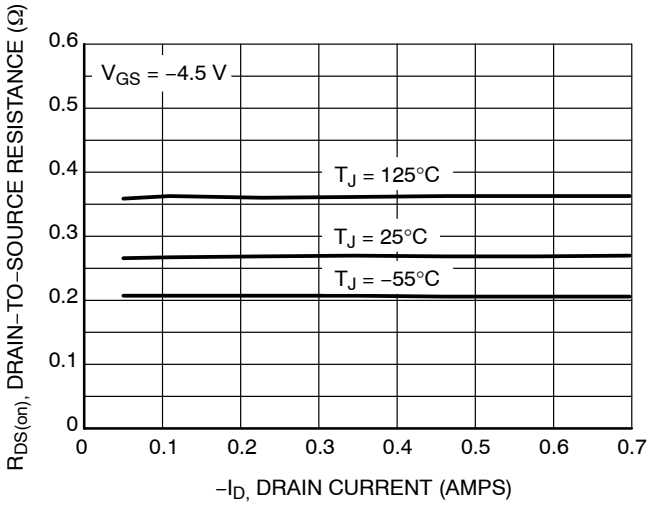


Figure 3. On−Resistance vs. Drain Current and Temperature

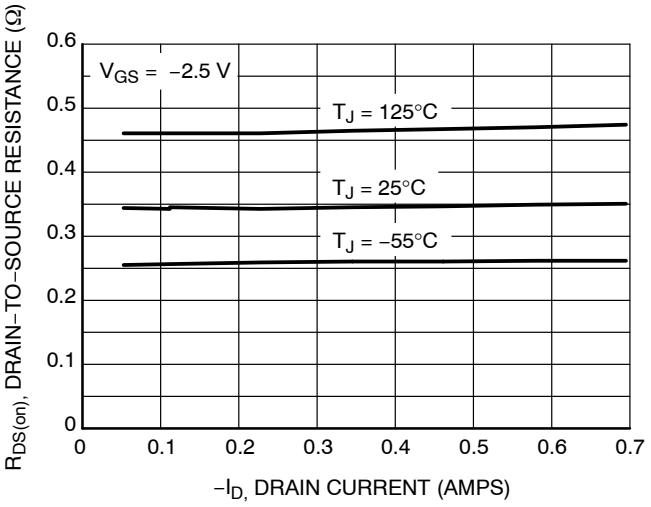


Figure 4. On−Resistance vs. Drain Current and Temperature

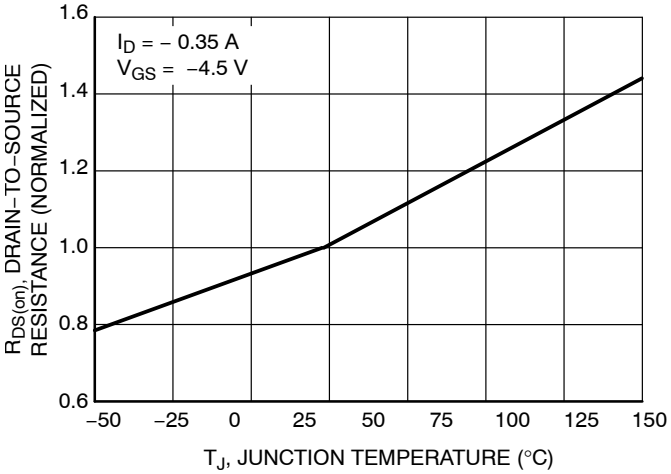


Figure 5. On−Resistance Variation with Temperature

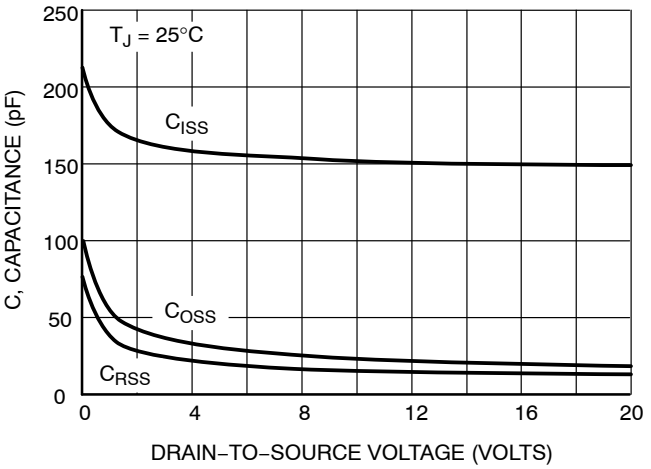


Figure 6. Capacitance Variation

TYPICAL ELECTRICAL CHARACTERISTICS

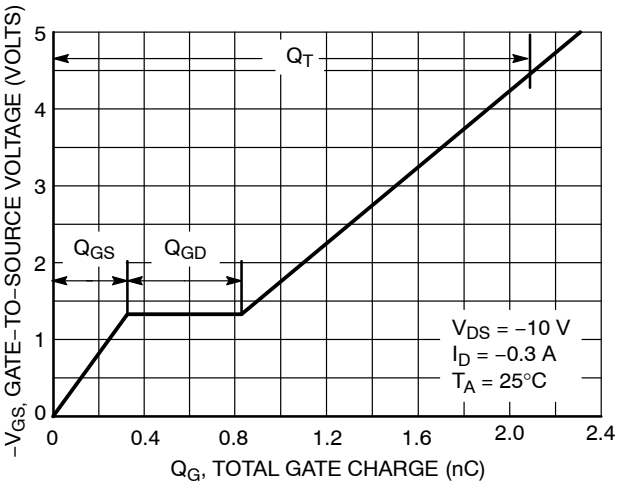


Figure 7. Gate−to−Source Voltage vs. Total Gate Charge

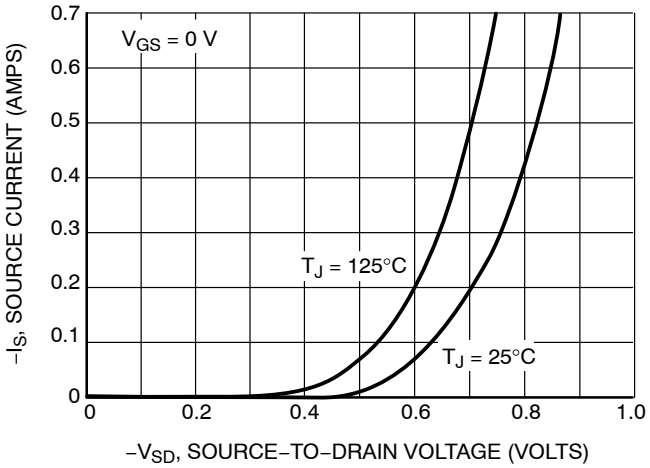


Figure 8. Diode Forward Voltage vs. Current

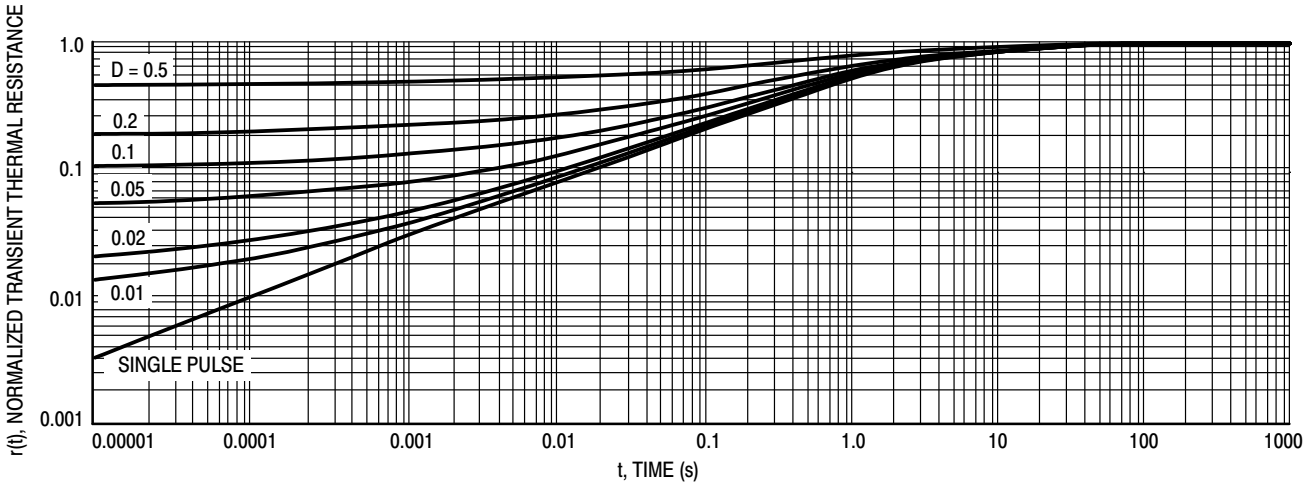


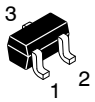
Figure 9. Normalized Thermal Response

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

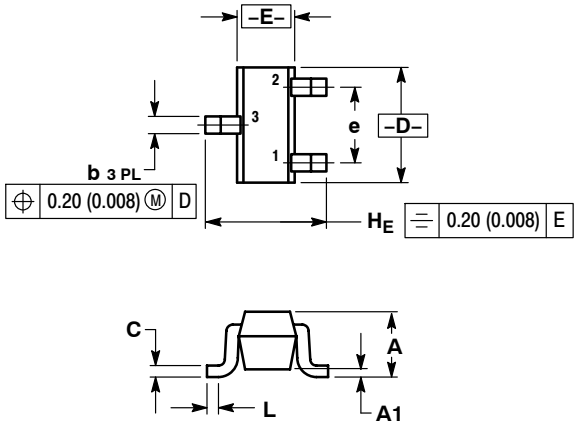
ON Semiconductor®

SC−75/SOT−416
CASE 463−01
ISSUE G

DATE 07 AUG 2015



SCALE 4:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.80	0.90	0.027	0.031	0.035
A1	0.00	0.05	0.10	0.000	0.002	0.004
b	0.15	0.20	0.30	0.006	0.008	0.012
C	0.10	0.15	0.25	0.004	0.006	0.010
D	1.55	1.60	1.65	0.061	0.063	0.065
E	0.70	0.80	0.90	0.027	0.031	0.035
e	1.00 BSC			0.04 BSC		
L	0.10	0.15	0.20	0.004	0.006	0.008
H_E	1.50	1.60	1.70	0.060	0.063	0.067

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

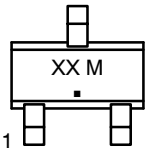
STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN

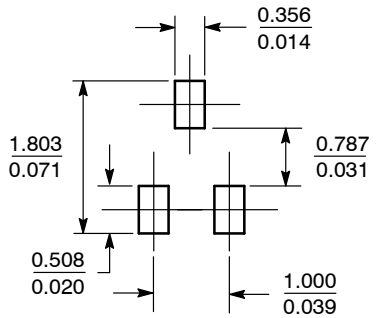
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



SCALE 10:1 $\left(\frac{mm}{inches}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**SC−75/SOT−416**	**PAGE 1 OF 1**

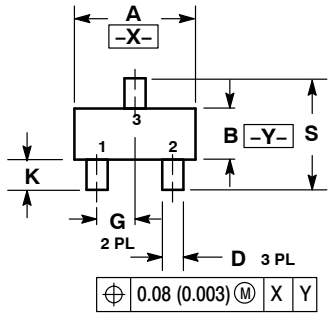
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

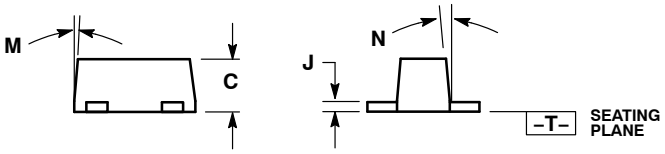
ON Semiconductor®

SC−89, 3 LEAD
CASE 463C−03
ISSUE C

DATE 31 JUL 2003

SCALE 4:1





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 463C−01 OBSOLETE, NEW STANDARD 463C−02.

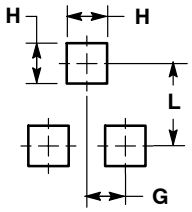
	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.60	1.70	0.059	0.063	0.067
B	0.75	0.85	0.95	0.030	0.034	0.040
C	0.60	0.70	0.80	0.024	0.028	0.031
D	0.23	0.28	0.33	0.009	0.011	0.013
G	0.50 BSC			0.020 BSC		
H	0.53 REF			0.021 REF		
J	0.10	0.15	0.20	0.004	0.006	0.008
K	0.30	0.40	0.50	0.012	0.016	0.020
L	1.10 REF			0.043 REF		
M	−−−	−−−	10	−−−	−−−	10
N	−−−	−−−	10	−−−	−−−	10
S	1.50	1.60	1.70	0.059	0.063	0.067

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

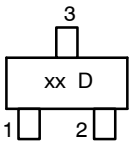
STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE



RECOMMENDED PATTERN OF SOLDER PADS

GENERIC MARKING DIAGRAM*



xx = Specific Device Code
D = Date Code

*This information is generic. Please refer to device data sheet for actual part marking.

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DESCRIPTION:	**SC−89, 3 LEAD**	**PAGE 1 OF 1**

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