

T-46-23-15

NMB Semiconductor

**AAA1M300 Fast Page Mode
CMOS 1M $\times$ 1 Dynamic RAM**

PRELIMINARY

FEATURES

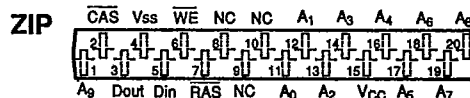
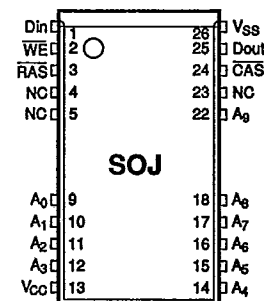
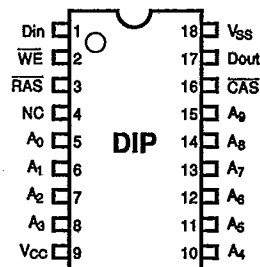
- 1,048,576 $\times$ 1 bit Organization
- Single 5V $\pm$ 10% Power Supply
- Performance Ranges:

Parameter	-06	-07	-08
Max. $\overline{\text{RAS}}$ Access Time	60ns	70ns	80ns
Max. $\overline{\text{CAS}}$ Access Time	15ns	20ns	20ns
Max. Column Address Access Time	30ns	35ns	40ns
Min. Read/Write Cycle Time	110ns	130ns	150ns

- Fast page mode operation

- Low Power Operation
 - Standby current (CMOS) 1mA
 - Operating current 60mA
- 512 Refresh cycles distributed across 8ms
- All input and output clocks are fully TTL and CMOS compatible
- Refresh modes:
 - RAS only, CAS before RAS and hidden refresh
- High reliability plastic
 - 18 pin 300 mil wide DIP,
 - plastic 26pin SOJ, and
 - plastic 20pin ZIP.

PIN CONFIGURATION



DESCRIPTION

The AAA1M300 is a high speed, 1,048,576 $\times$ 1 bit CMOS dynamic random access memory. Fabricated with leading edge CMOS technology, the AAA1M300 offers a combination of features which are unattainable with NMOS technology, namely, speed, power and inherently high CMOS reliability.

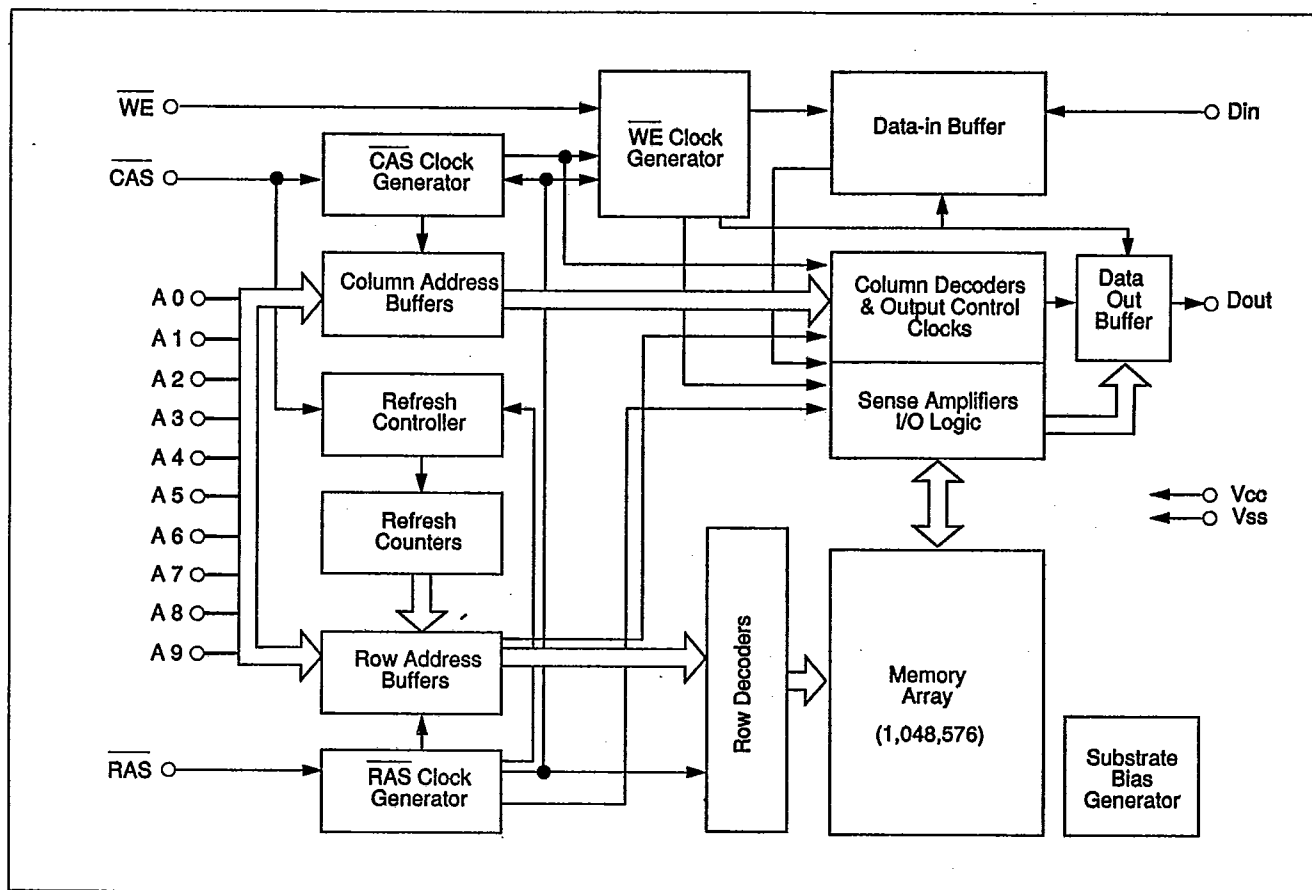
The AAA1M300, with its fast page mode operation can allow random or sequential access of up to 1,024 bits within a row with cycle times as fast as 35ns. Because of static circuitry, the $\overline{\text{CAS}}$ clock is no longer in the critical timing path.

The flow-through column latch allows address pipelining while relaxing many critical system timing requirements for fast speed.

Multiplexed address inputs permit AAA1M300 to be packaged in a standard 18-pin plastic DIP, 26-pin plastic SOJ and 20-pin plastic ZIP. The package sizes provide high system bit densities and are compatible with widely available automated testing and insertion equipment. System level features include single power supply of 5V $\pm$ 10% tolerance and direct interface with high performance TTL logic families.

PIN NAMES

A0~A9	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
Din	Data Input
Dout	Data Output
$\overline{\text{WE}}$	Write Enable
Vcc	+5V Supply
Vss	Ground
NC	No Connection

AAA1M300
CMOS1M × 1 Dynamic RAM
FUNCTIONAL BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Voltage on Any Pin Relative to V_{SS}	V_{in}, V_{out}	-1 to 7	V
Voltage on V_{CC} Relative to V_{SS}	V_{CC}	-1 to 7	V
Storage Temperature (Plastic)	T_{stg}	-55 to 125	°C
Power Dissipation	P_d	600	mW
Ambient Operating Temperature	T_a	0 to +70	°C

* Permanent device damage can occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	NOM	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage		0		V
V_{IH}	Input High Voltage, All Inputs	2.4		6.5	V
V_{IL}	Input Low Voltage, All Inputs	-1.0		0.8	V

Note: All voltage values in this data sheet are with respect to V_{SS} .

DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0 V ±10%)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTES
I _{CC1}	Average V _{CC} Power Supply Current (Operating)	-06 -07 -08		80 70 60	mA mA mA	t _{RC} = t _{RC} (min.) RAS, CAS, Address cycling	1, 2
I _{CC2}	V _{CC} Supply Current (TTL standby)			2	mA	RAS and CAS at V _{IH} . All Other Inputs ≥ V _{SS}	
I _{CC3}	V _{CC} Supply Current (RAS only Refresh)	-06 -07 -08		80 70 60	mA mA mA	t _{RC} = t _{RC} (min.) RAS cycling, CAS = V _{IH}	1
I _{CC4}	V _{CC} Supply Current (Fast page mode)	-06 -07 -08		50 40 30	mA mA mA	t _{PC} = t _{PC} (min.) RAS = V _{IL} CAS, Address cycling	1, 2
I _{CC5}	V _{CC} Supply Current (CAS before RAS Refresh)	-06 -07 -08		80 70 60	mA mA mA	t _{RC} = t _{RC} (min.) RAS, CAS cycling	1
I _{CC6}	V _{CC} Supply Current (CMOS standby)			1	mA	RAS and CAS ≥ V _{CC} -0.2V All Other Inputs ≥ V _{SS}	
I _{IL1}	Input Leakage Current (Any input pin)		-10	10	μA	0V ≤ V _{IN} ≤ 5.5V Others = 0V	
I _{LO}	Output Leakage Current (For high impedance state)		-10	10	μA	RAS at V _{IH} , CAS at V _{IH} 0V ≤ V _{OUT} ≤ 5.5V	
V _{OH}	Output High Voltage		2.4		V	I _{OH} = -5.0 mA	
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 4.2 mA	

Notes: 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rate.2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with outputs open.CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0 V ±10%, f = 1 MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C _{IN}	Address, D _{IN}	—	4	pF ₄
C _{IN}	RAS, CAS, WE	—	4	pF
C _{OUT}	Dout	—	6	pF

AAA1M300
CMOS 1M × 1 Dynamic RAM
A.C. OPERATING CONDITIONS ($0^{\circ}\text{C} \leq T_a \leq 70^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$) (NOTES 3, 4, 5)

NO.	SYMBOL		PARAMETER	AAA1M300-06		AAA1M300-07		AAA1M300-08		UNIT	NOTES
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{CL1QV}	t_{CAC}	Access Time from $\overline{\text{CAS}}$	—	15	—	20	—	20	ns	6
2	t_{CH2QV}	t_{CPA}	Access Time from $\overline{\text{CAS}}$ Precharge	—	30	—	35	—	40	ns	13
3	t_{AVQV}	t_{AA}	Access Time from Column Address	—	30	—	35	—	40	ns	7
4	t_{RL1QV}	t_{RAC}	Access Time from $\overline{\text{RAS}}$	—	60	—	70	—	80	ns	6
5	t_{RL1CH1}	t_{CSH}	$\overline{\text{CAS}}$ Hold Time	60	—	70	—	80	—	ns	
6	t_{RL1CH1}	t_{CHR}	$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	30	—	30	—	30	—	ns	
7	t_{CH2CL2}	t_{CPN}	$\overline{\text{CAS}}$ Precharge Time	10	—	10	—	10	—	ns	
8	t_{CH2CL2}	t_{CPT}	$\overline{\text{CAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Counter Test)	30	—	40	—	40	—	ns	
9	t_{CH2CL2}	t_{CP}	$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	10	—	10	—	10	—	ns	
10	t_{CL1CH1}	t_{CAS}	$\overline{\text{CAS}}$ Pulse Width	15	10K	20	10K	20	10K	ns	
11	t_{CL1RL2}	t_{CSR}	$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	10	—	10	—	10	—	ns	
12	t_{CL1QV}	t_{CLZ}	$\overline{\text{CAS}}$ to Output in Low-Z	0	—	0	—	0	—	ns	8
13	t_{CH2RL2}	t_{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5	—	5	—	5	—	ns	
14	t_{CL1WL2}	t_{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	15	—	20	—	20	—	ns	11
15	t_{CL1AX} t_{WL1AX}	t_{CAH}	Column Address Hold Time	10	—	15	—	15	—	ns	
16	t_{RL1AX}	t_{AR}	Column Address Hold Time Referenced to $\overline{\text{RAS}}$	50	—	55	—	60	—	ns	
17	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	ns	
18	t_{AVRH1}	t_{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	30	—	35	—	40	—	ns	
19	t_{AVWL2}	t_{AWD}	Column Address to $\overline{\text{WE}}$ Delay Time	30	—	35	—	40	—	ns	11
20	t_{CL1DX} t_{WL1DX}	t_{DH}	Data Hold Time	10	—	15	—	15	—	ns	12
21	t_{RL1DX}	t_{DHR}	Data Hold Time Referenced to $\overline{\text{RAS}}$	50	—	55	—	60	—	ns	
22	t_{DVCL2} t_{DVWL2}	t_{DS}	Data Setup Time	0	—	0	—	0	—	ns	12
23	t_{CH2QX}	t_{OFF}	Output Buffer Turn-off Delay Time	0	15	0	20	0	20	ns	10
24	t_{CL1RH1}	t_{RSH}	$\overline{\text{RAS}}$ Hold Time	15	—	20	—	20	—	ns	
25	t_{RH2RL2}	t_{RP}	$\overline{\text{RAS}}$ Precharge Time	40	—	50	—	60	—	ns	
26	t_{RL1RH1}	t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	60	100K	70	100K	80	100K	ns	
27	t_{RL1RH1}	t_{RASP}	$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	60	100K	70	100K	80	100K	ns	
28	t_{RL1CL1}	t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	15	45	20	50	20	60	ns	6
29	t_{RH2CL2}	t_{RPC}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	0	—	0	—	0	—	ns	
30	t_{RL1AV}	t_{RAD}	$\overline{\text{RAS}}$ to Column Address Delay Time	15	30	15	35	15	40	ns	7
31	t_{RL1WL2}	t_{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	60	—	70	—	80	—	ns	11
32	t_{CH2WL2}	t_{RCH}	Read Command Hold Time	0	—	0	—	0	—	ns	9
33	t_{RH2WL2}	t_{RRH}	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	0	—	0	—	0	—	ns	9
34	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0	—	0	—	0	—	ns	
35	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	110	—	130	—	150	—	ns	
36	t_{CL2CL2}	t_{PC}	Read or Write Cycle Time (Fast Page Mode)	35	—	40	—	45	—	ns	13,14
37	t_{RL2RL2}	t_{RWC}	Read-Modify-Write Cycle Time	135	—	155	—	175	—	ns	
38	t_{CL2CL2}	t_{PRWC}	Read-Modify-Write Cycle Time (Fast Page Mode)	60	—	75	—	80	—	ns	13,14

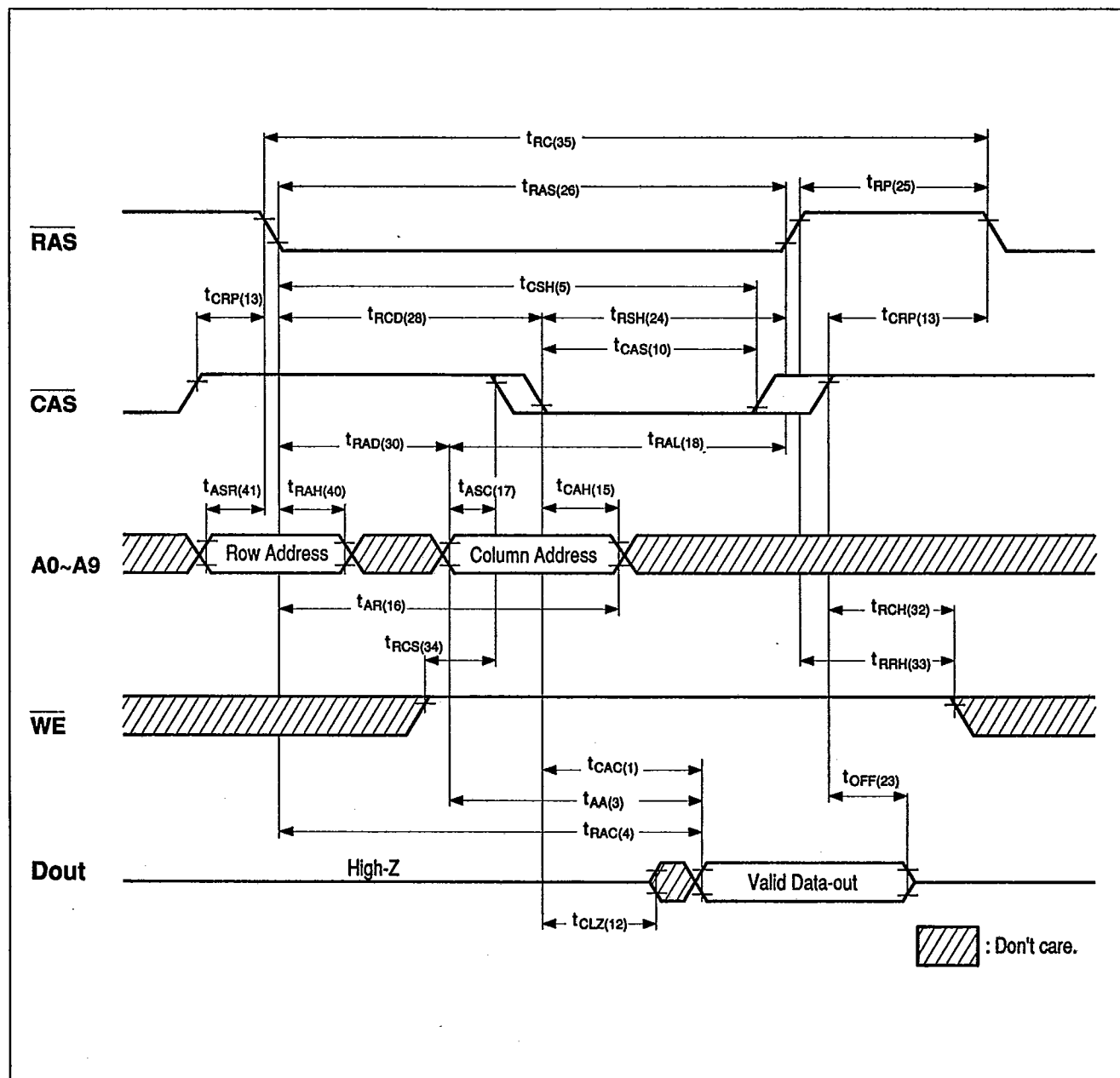
NO.	SYMBOL		PARAMETER	AAA1M300-06		AAA1M300-07		AAA1M300-08		UNIT	NOTES
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
39	t_{REF}	t_{REF}	Refresh Period	—	8	—	8	—	8	ms	
40	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10	—	12	—	12	—	ns	
41	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0	—	0	—	0	—	ns	
42	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	4, 5
43	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10	—	15	—	15	—	ns	
44	t_{RL1WH1}	t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	50	—	55	—	60	—	ns	
45	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	10	—	15	—	15	—	ns	
46	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0	—	0	—	0	—	ns	11
47	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	20	—	ns	
48	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	20	—	ns	

Notes:

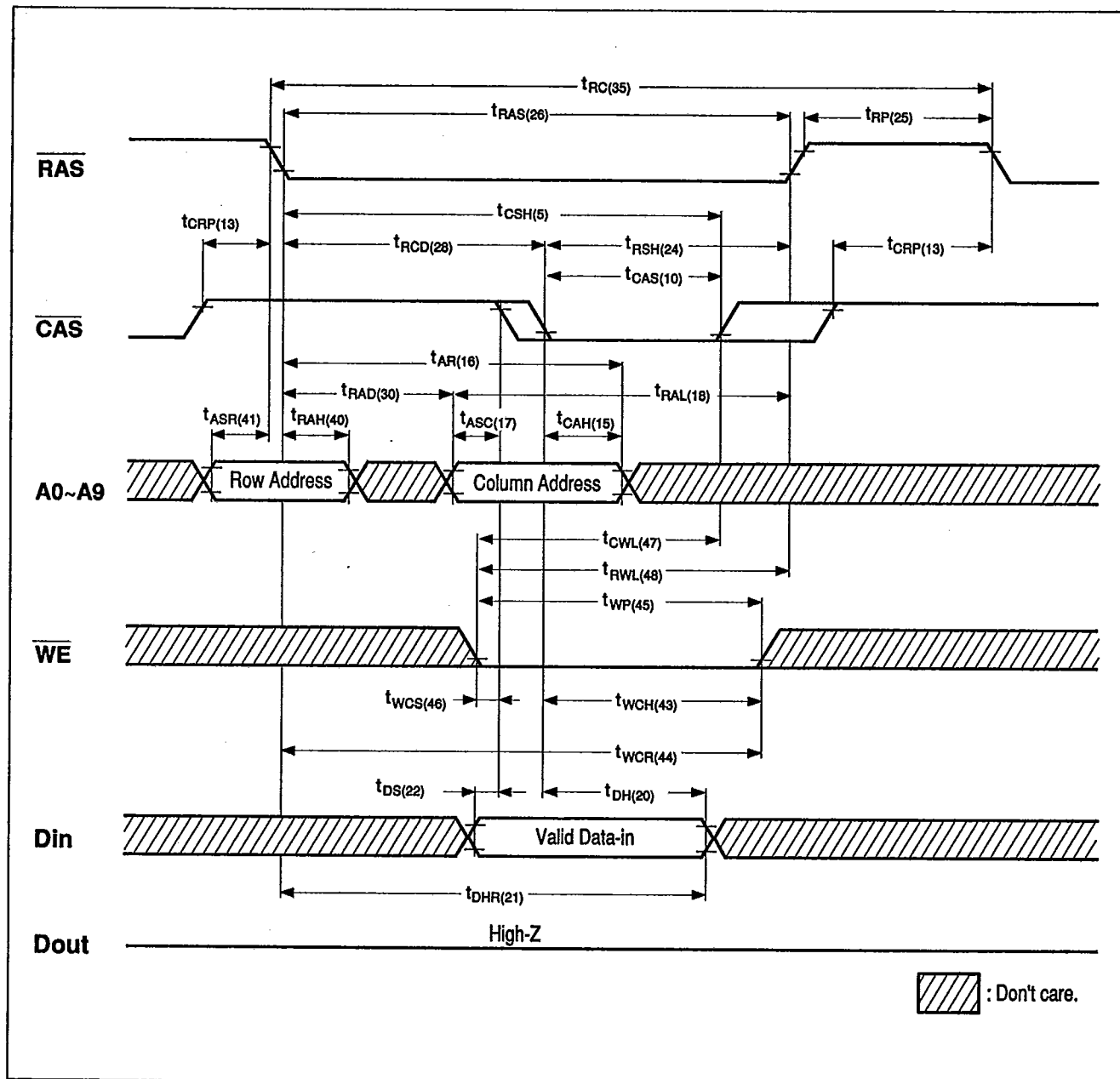
- An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required. Eight initialization cycles are required after extended periods of bias without clocks (greater than 8ms).
- AC measurements assume $t_T=5$ ns. All AC parameters are measured with $V_{IL}(\text{min.}) \geq V_{SS}$ and $V_{IH}(\text{max.}) \leq V_{CC}$ and with a load equivalent to two TTL loads and 100pF.
- $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
- Operation within the $t_{RAD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled exclusively by t_{AA} .
- Assumes three state test load (5pF and a 380 Ohm Thevenin equivalent).
- Either t_{RCH} or t_{RRH} must be satisfied for a Read cycle.
- $t_{OFF}(\text{max.})$ defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
- t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data-out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$ and $t_{AWD} \geq t_{AWD}(\text{min.})$, the cycle is a read-modify-write cycle and the data-out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data-out (at access time) is indeterminate.
- These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycles.
- Access time is determined by the longer of t_{AA} , t_{CAC} or t_{CPA} .
- $t_{ASC} \geq t_{CP}$ to achieve $t_{PC}(\text{min.})$ and $t_{CPA}(\text{max.})$ values.

AAA1M300
CMOS 1M × 1 Dynamic RAM

READ CYCLE

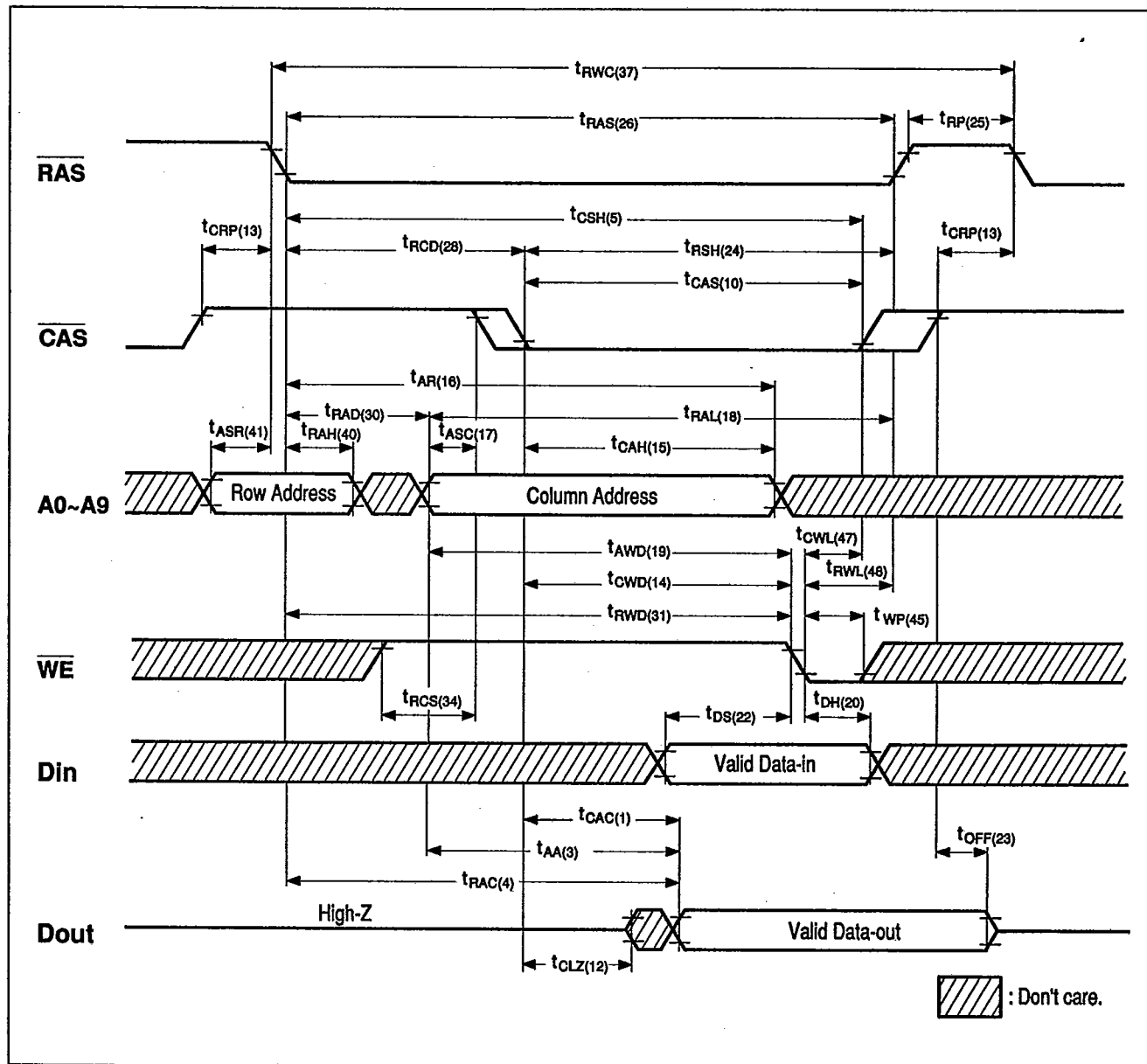


EARLY WRITE CYCLE



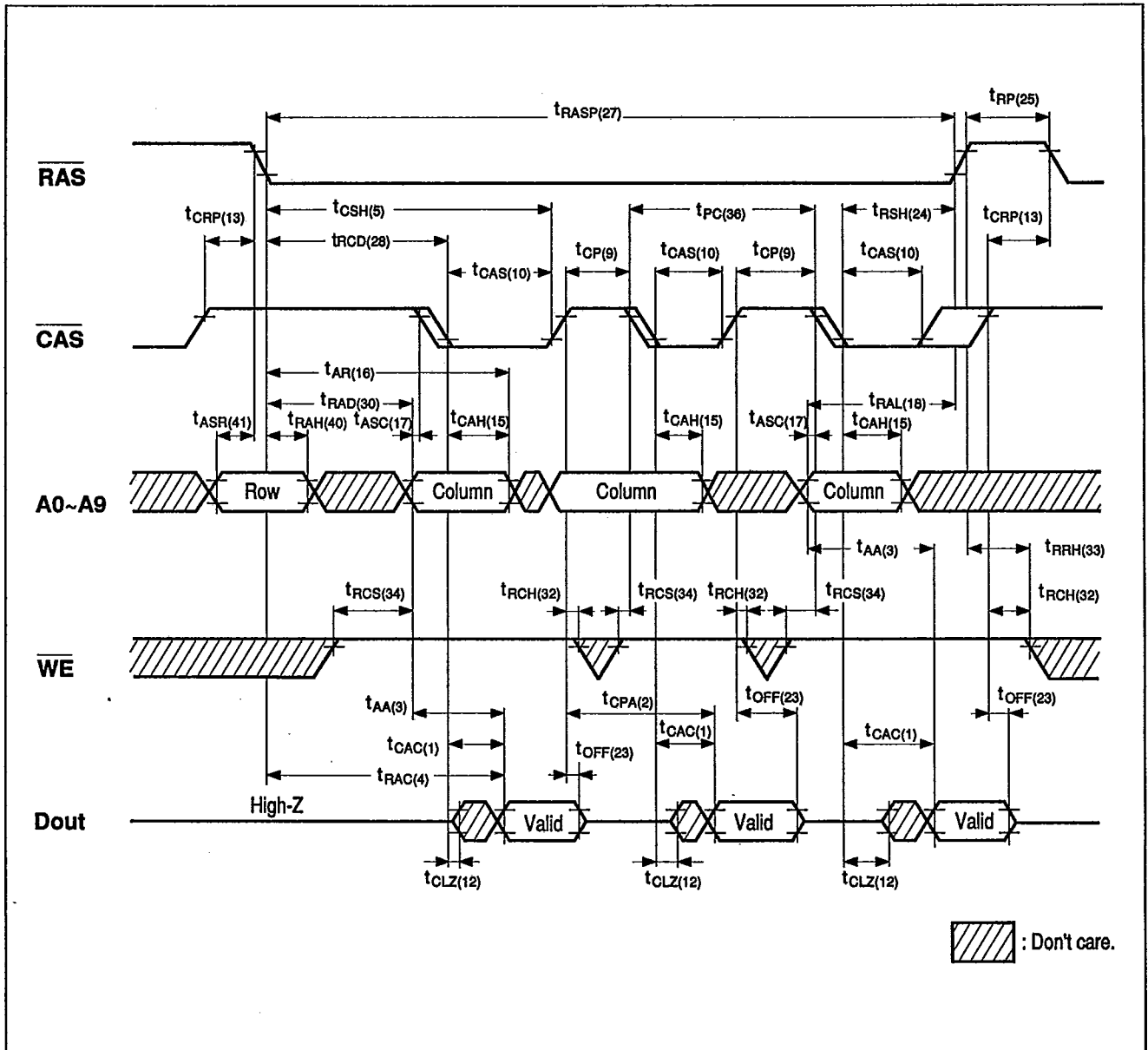
AAA1M300
CMOS 1M × 1 Dynamic RAM

READ-MODIFY-WRITE CYCLE



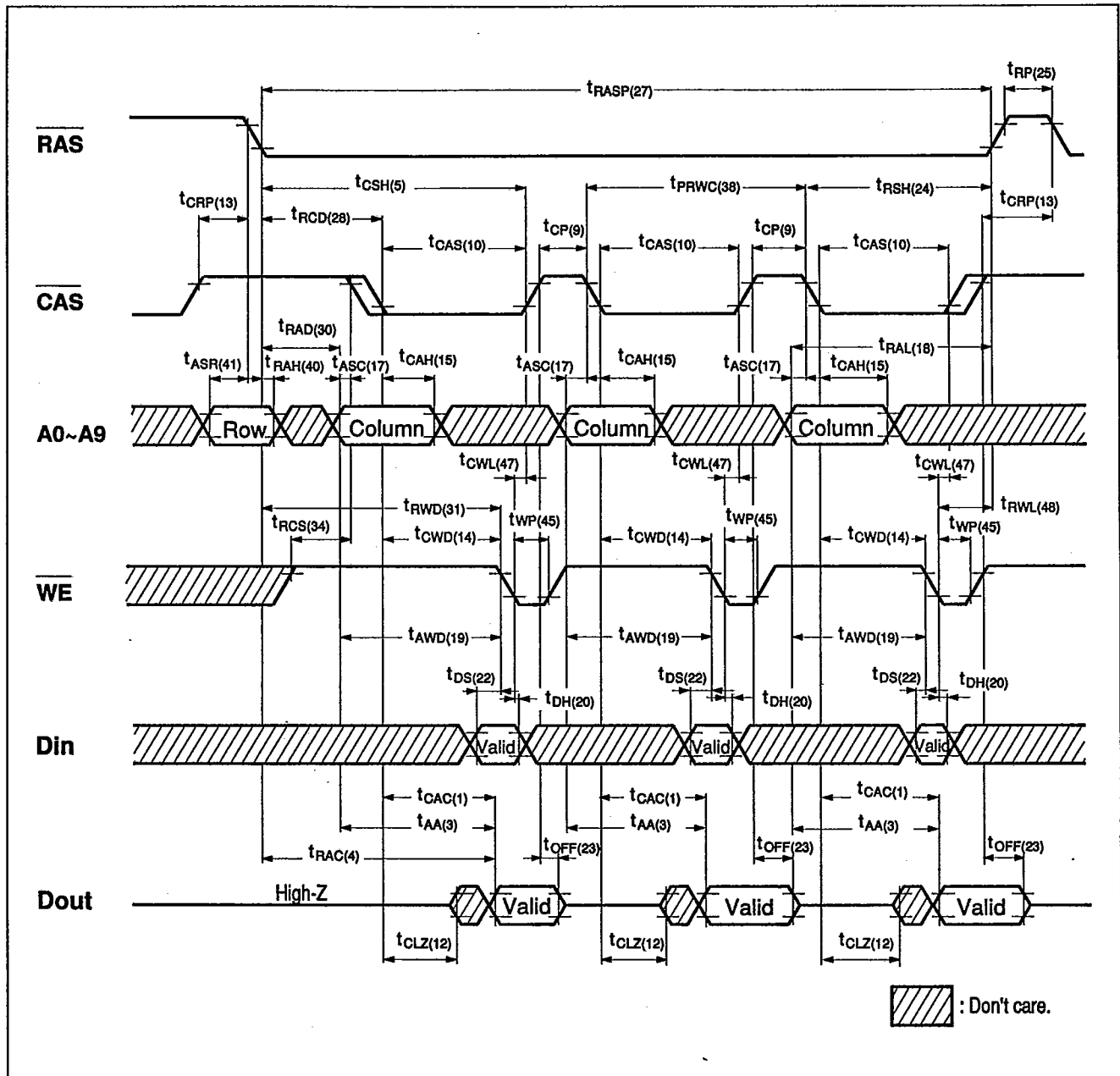
AAA1M300
CMOS 1M × 1 Dynamic RAM

FAST PAGE MODE READ CYCLE



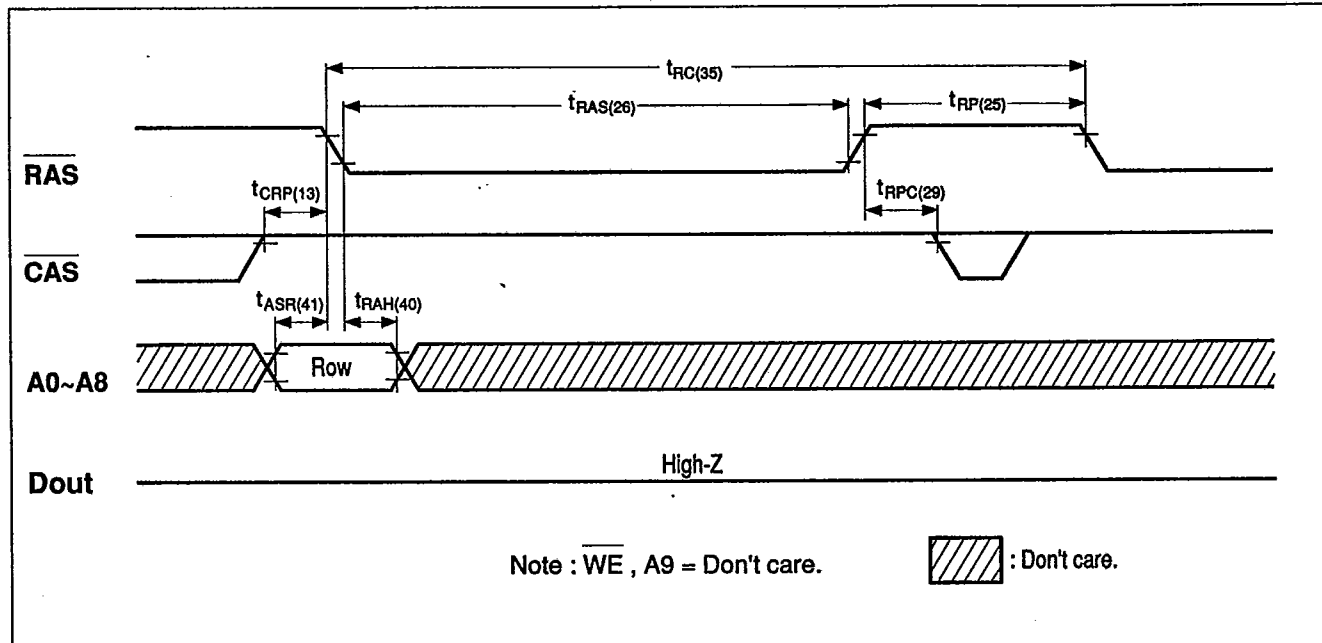
AAA1M300
CMOS 1M × 1 Dynamic RAM

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

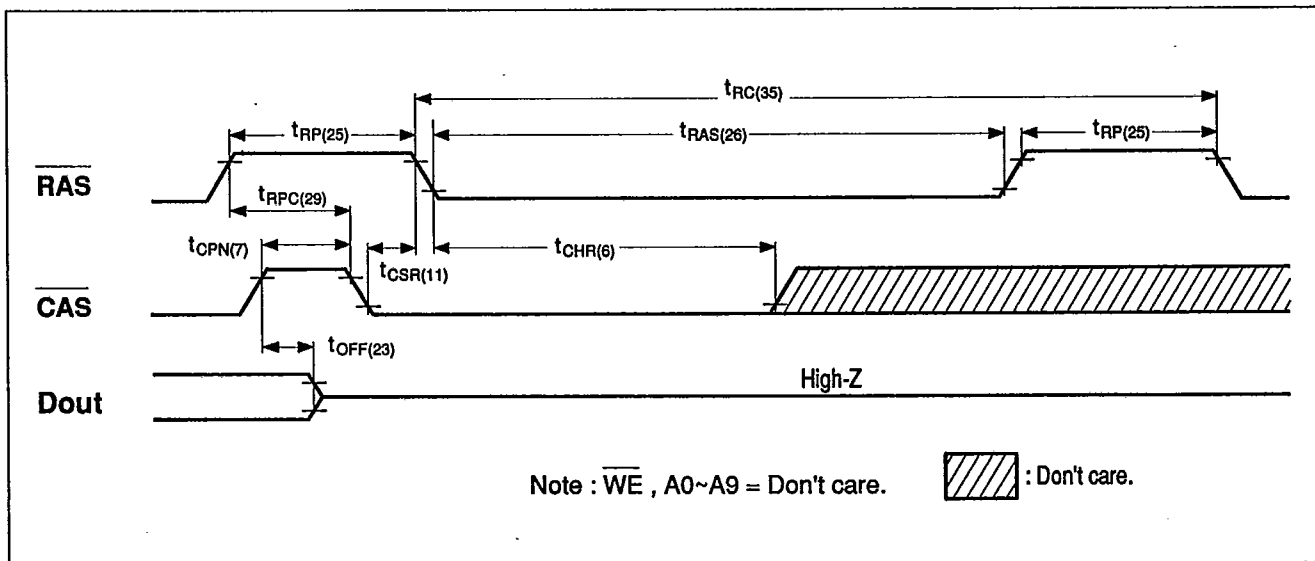


AAA1M300
CMOS 1M × 1 Dynamic RAM

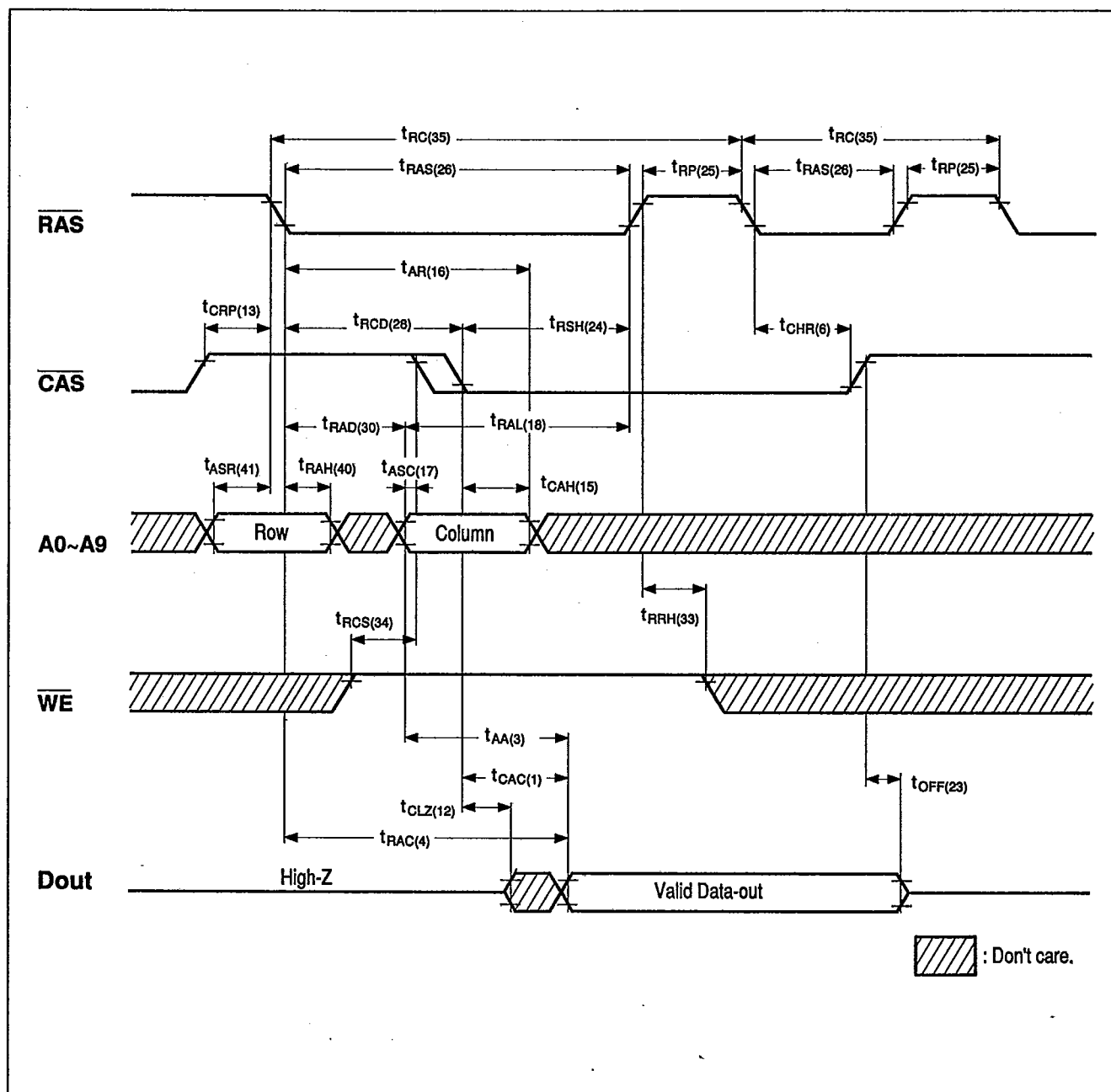
RAS ONLY REFRESH CYCLE



CAS BEFORE RAS REFRESH CYCLE

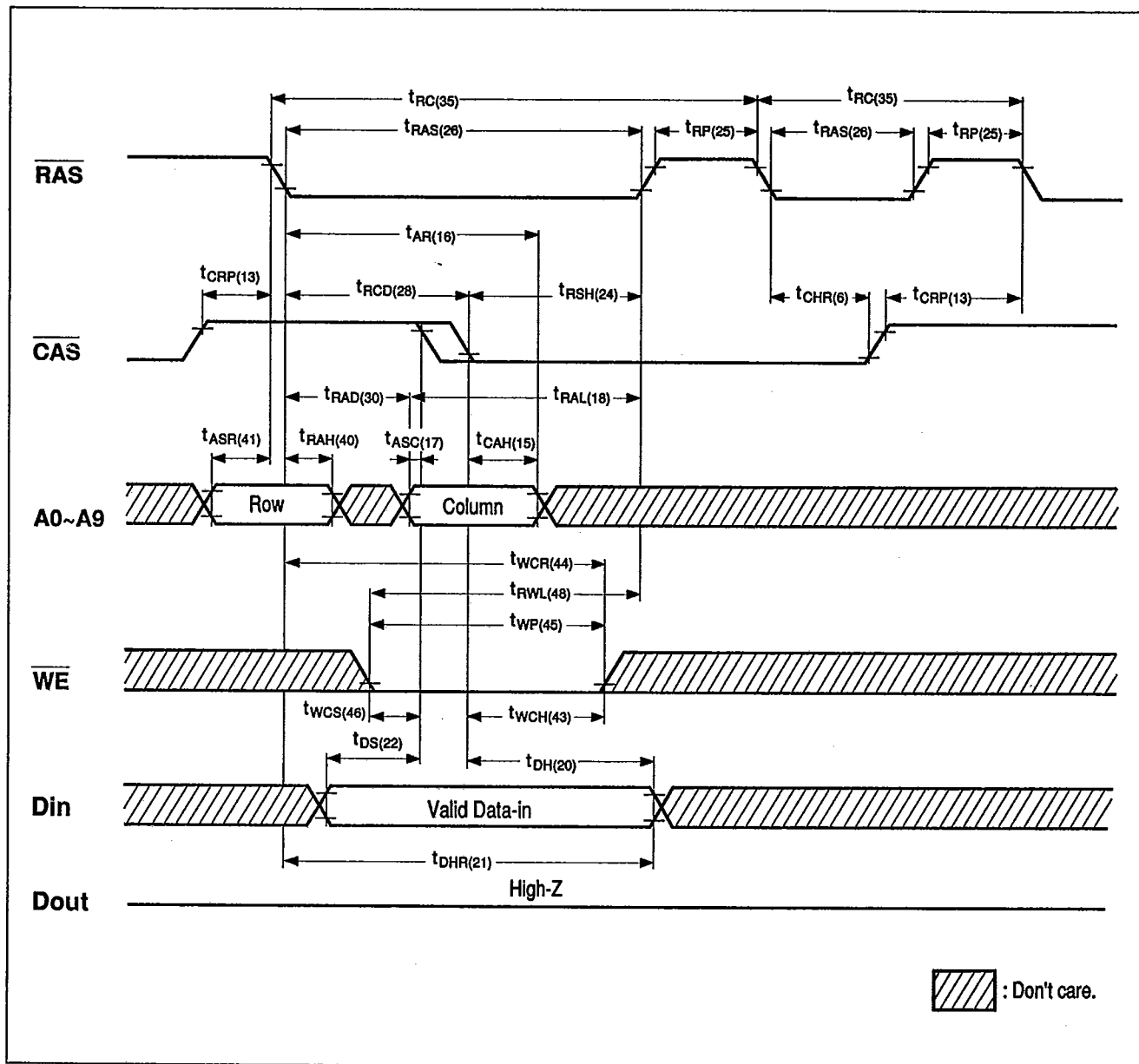


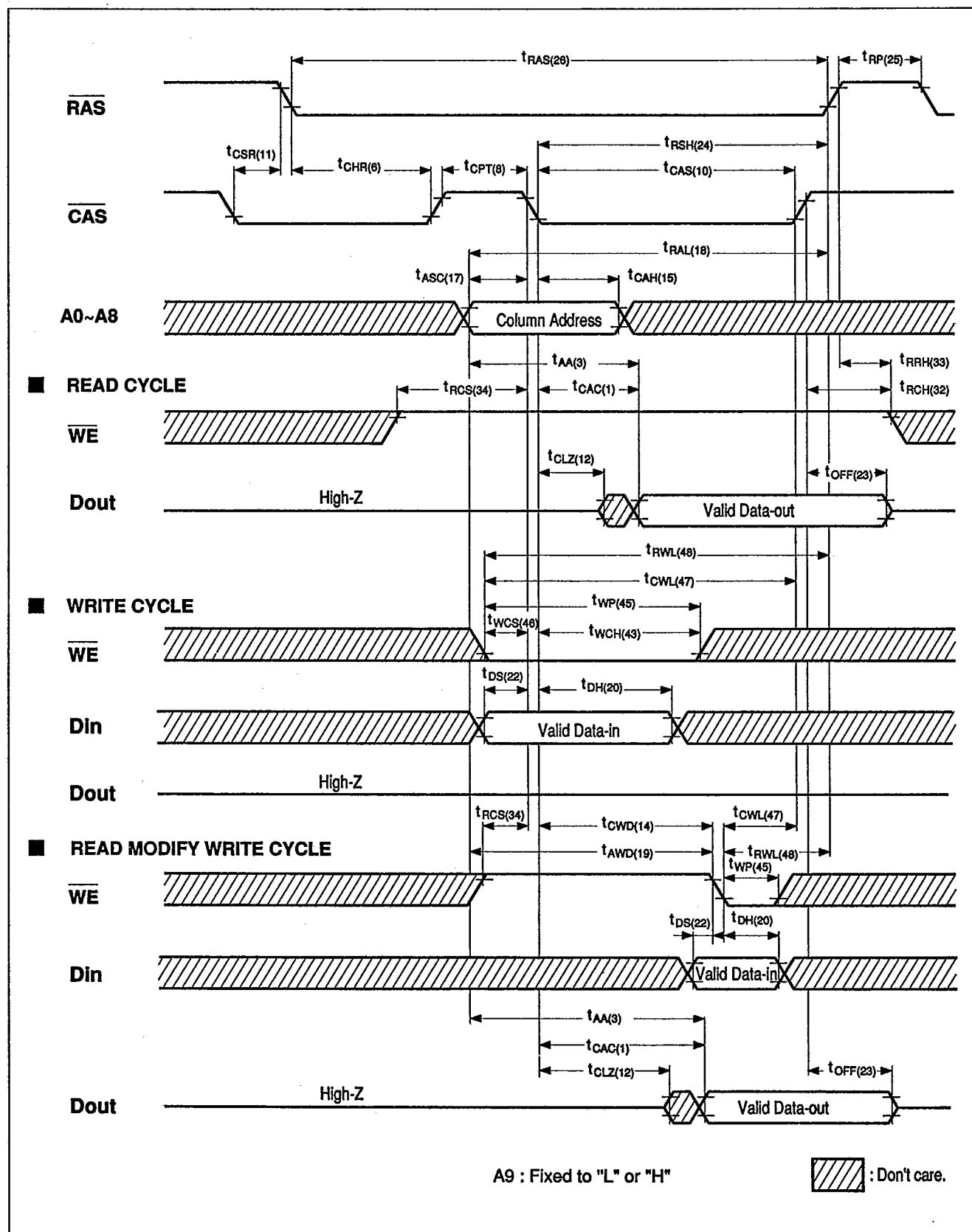
HIDDEN REFRESH CYCLE (READ)



AAA1M300
CMOS 1M × 1 Dynamic RAM

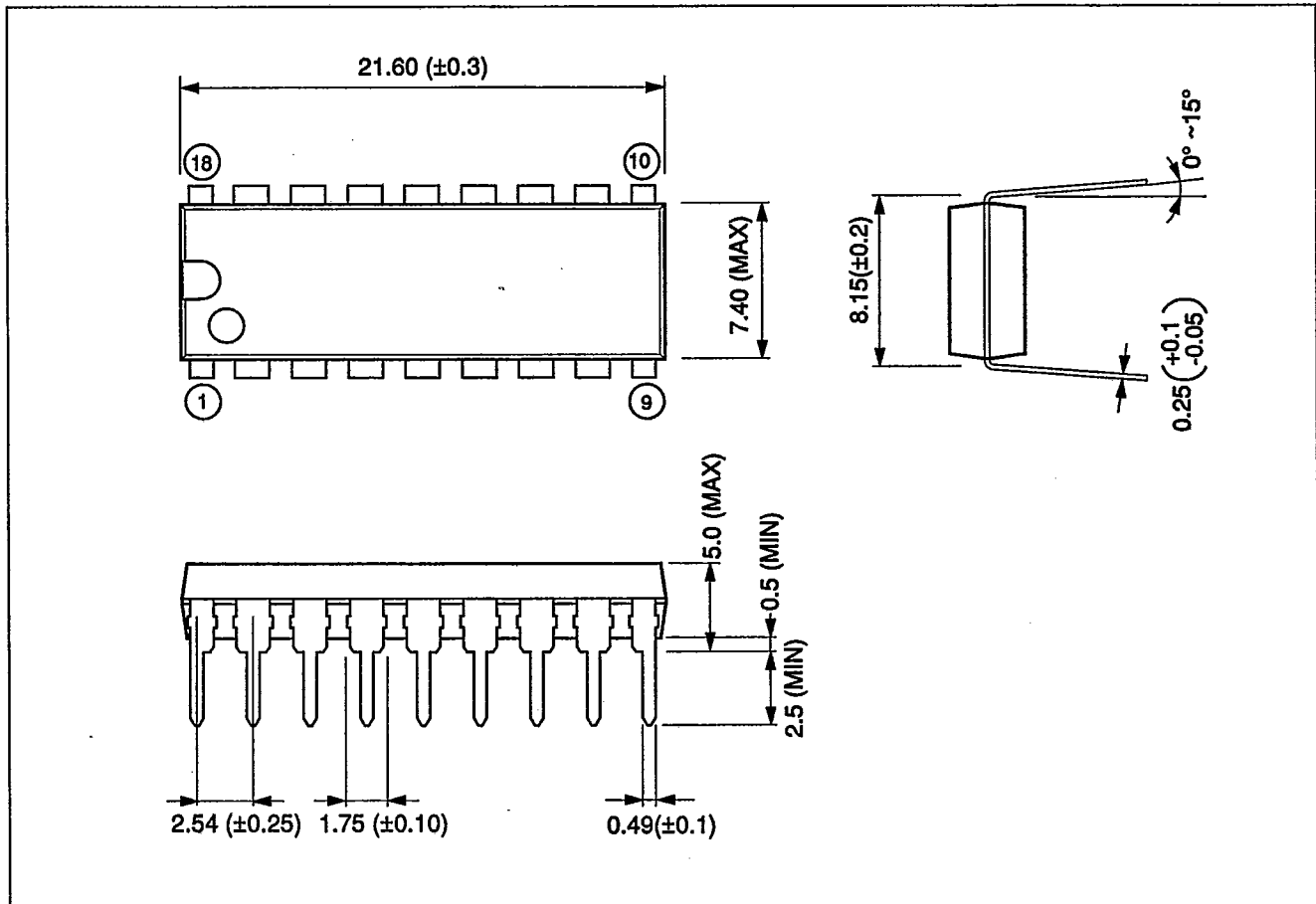
HIDDEN REFRESH CYCLE (WRITE)



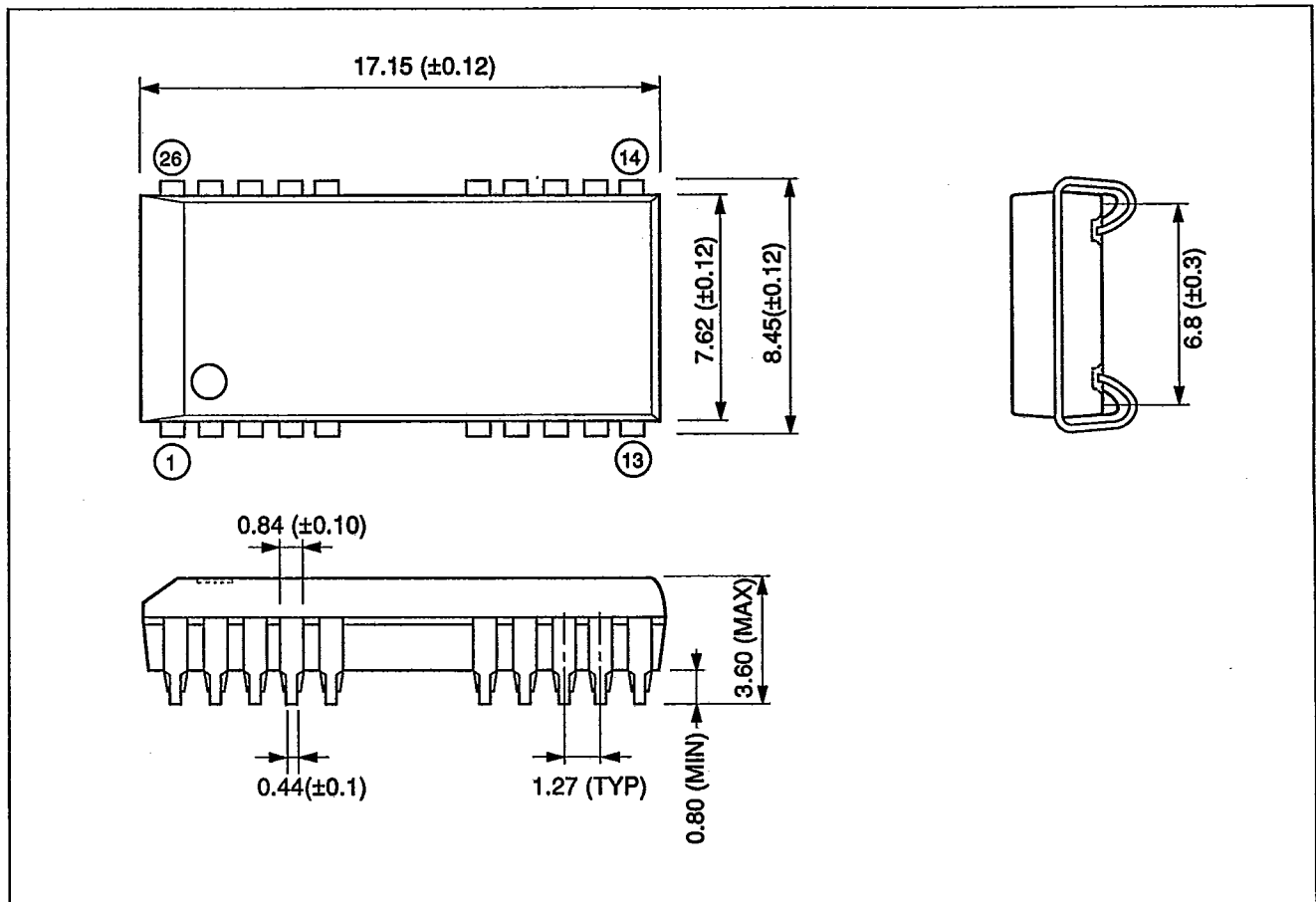
AAA1M300
CMOS 1M × 1 Dynamic RAM
CAS BEFORE RAS REFRESH COUNTER TEST CYCLE


AAA1M300
CMOS 1M × 1 Dynamic RAM

18 PIN PLASTIC DIP (300 mil) (Unit: mm)

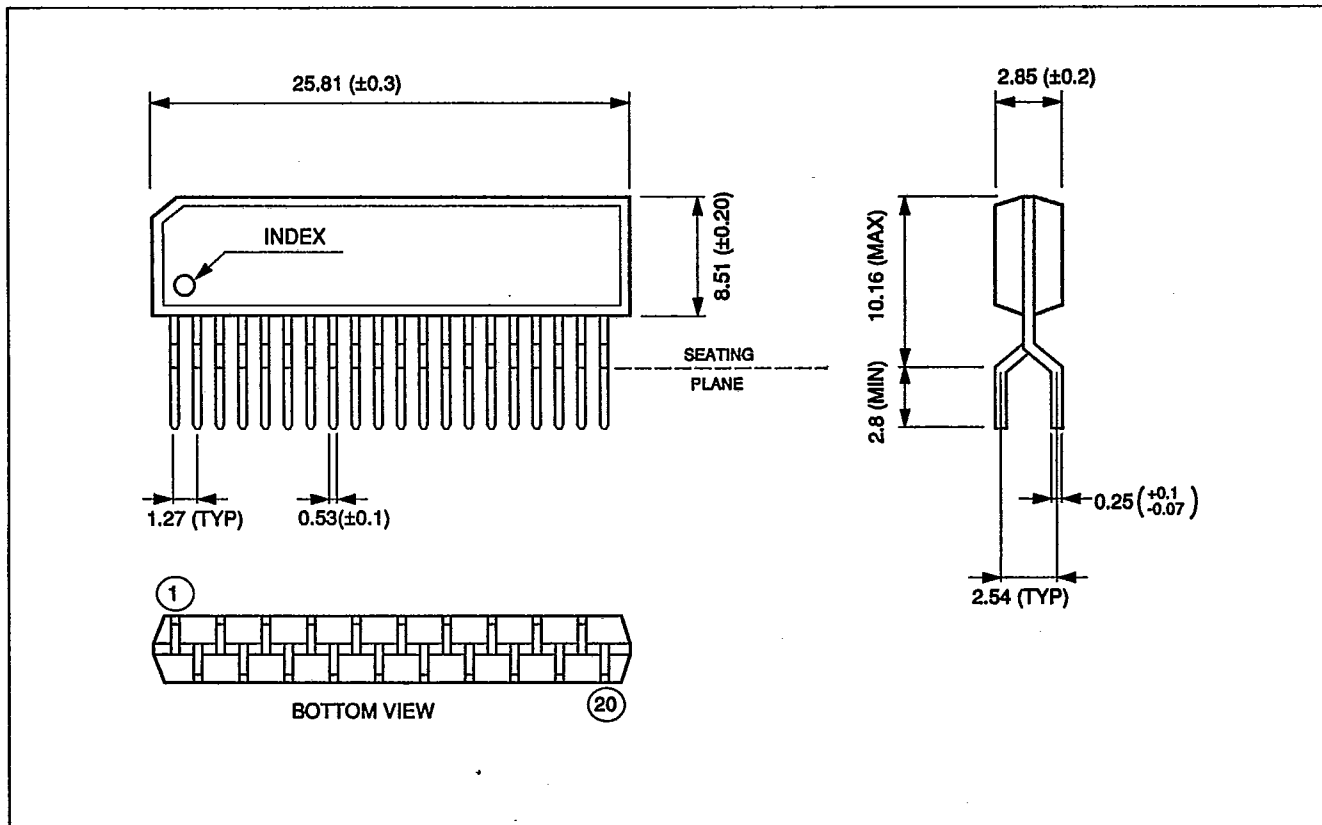


26 PIN PLASTIC SOJ (Unit: mm)



AAA1M300
CMOS 1M × 1 Dynamic RAM

20 PIN PLASTIC ZIP (Unit: mm)



ORDERING INFORMATION

