

# mos integrated circuit $\mu PD434008$

# 4M-BIT CMOS FAST STATIC RAM 512K-WORD BY 8 BITS

#### Description

The  $\mu$ PD434008 is a high speed, low power, 4 194 304 bits (524 288 words by 8 bits) CMOS static RAM. The  $\mu$ PD434008 is packed in 36-pin plastic SOJ.

#### **Features**

- 524 288 words by 8 bits organization
- Fast access time 20 ns (MAX.)
- OE input for easy application

#### **Ordering Information**

Part number	Package	Access time ns (MAX.)	Operating supply current mA (MAX.)	Standby supply current mA (MAX.)	Quality grade
μPD434008LE-20	36-pin plastic	20	190	10	Standard
μPD434008LE-25	SOJ (400 mil)	25	170	10	Standard

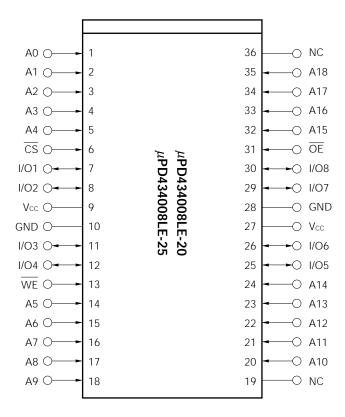
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice.



## Pin Configuration (Marking Side)

## 36-pin plastic SOJ (400 mil)



A0 – A18 : Address inputs I/O1 – I/O8 : Data inputs/outputs

CS : Chip Select

WE : Write Enable

OE : Output Enable

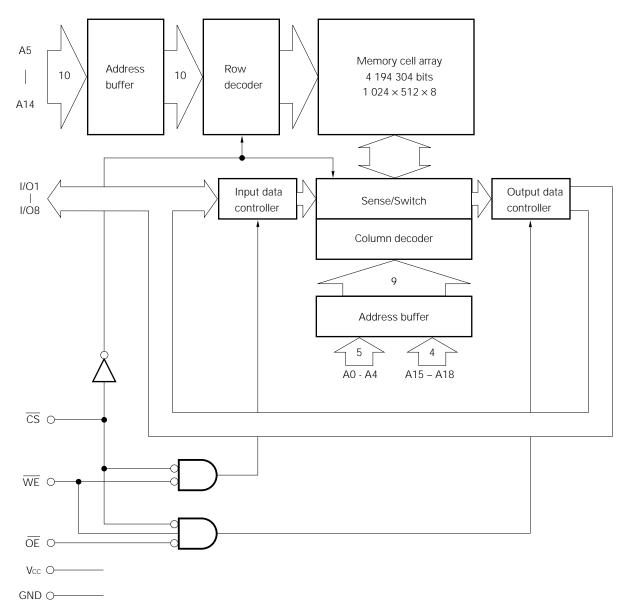
Vcc : Power supply

GND : Ground

NC : No connection







# Truth Table

CS	ŌĒ	WE	Mode	I/O	Supply current
Н	×	×	Not selected		lsв
L	Н	Н	Output disable	Hi-Z	
L	L	Н	Read	<b>D</b> оит	Icc
L	×	L	Write	Din	

Remark X : Don't care



#### **Electrical Characteristics**

## **Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Supply voltage	voltage Vcc		V
Input/Output voltage	VT	-0.5 Note to Vcc +0.3	V
Operating temperature Topt		0 to +70	°C
Storage temperature	Tstg	-55 to +125	°C

Note -2.0 V (MIN.) (Pulse width: 10 ns)

## **Recommended Operating Conditions**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
High level input voltage	VIH	2.2		Vcc +0.3	V
Low level input voltage	VIL	-0.5 <sup>Note</sup>		+0.8	V
Ambient temperature	Та	0		+70	°C

Note -2.0 V (MIN.) (Pulse width: 10 ns)

## DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test con	MIN.	TYP.	MAX.	Unit	
Input leakage current	lu	VIN = 0 V to Vcc		-2		+2	μΑ
Output leakage current	Іго	$\frac{V_{I/O}}{WE} = 0 \text{ V to Vcc, } \overline{CS} = V_{IH} \text{ or } \overline{OE} = V$		-2		+2	μΑ
Operating supply current	Icc	CS = V <sub>IL</sub> , I <sub>I/O</sub> = 0 mA,	μPD434008-20			190	mA
Operating supply current	ICC	Minimum cycle time	μPD434008-25			170	
	lsв	$\overline{CS} = V_{IH}$ , Minimum cycle time	μPD434008-20			60	
Standby cumply current			μPD434008-25			50	mA
Standby supply current	I <sub>SB1</sub>	$V_{CC} - 0.2 \text{ V} \stackrel{\leq}{=} \overline{CS},$ $V_{IN} \stackrel{\leq}{=} 0.2 \text{ V or } V_{CC} - 0.2 \text{ V} \stackrel{\leq}{=} V_{IN}$				10	MA
High level output voltage	Vон	Iон = -4.0 mA		2.4			V
Low level output voltage	Vol	IoL = 8 mA				0.4	V

Remark VIN: Input voltage

## Capacitance ( $T_a = +25$ °C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	CIN	$V_{IN} = 0 V$			6	pF
Input/Output capacitance	C1/0	V <sub>1/O</sub> = 0 V			10	pF

Remark 1. V<sub>IN</sub>: Input voltage

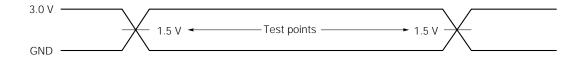
2. These parameters are periodically sampled and not 100 % tested.



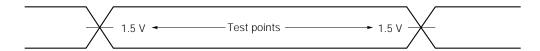
## AC Characteristics (Recommended operating conditions unless otherwise noted)

## **AC Test Conditions**

Input waveform (Rise/fall time ≤ 3 ns)

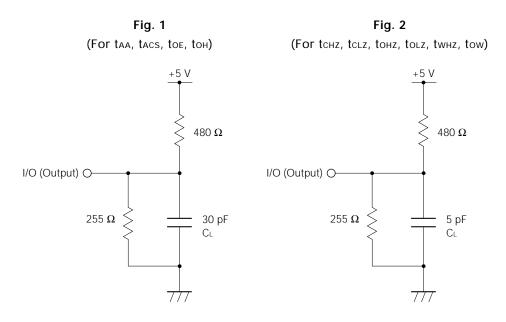


#### **Output waveform**



## **Output load**

AC Characteristics directed with the note should be measured with the output load shown in Fig. 1 or Fig. 2.



**Remark** C<sub>L</sub> includes capacitances of the probe and jig, and stray capacitances.



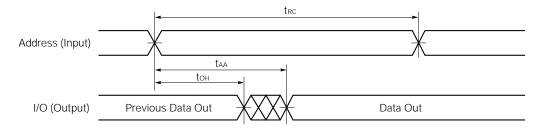
# Read Cycle

Parameter	Symbol	μPD434008LE-20		μPD434008LE-25		Unit	Condition	
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	Unit	Condition	
Read cycle time	trc	20		25		ns		
Address access time	taa		20		25	ns		
CS access time	tacs		20		25	ns	Note 1.	
OE access time	toe		10		12	ns	Note 1.	
Output hold from address change	tон	3		3		ns		
CS to output in low impedance	tcLz	3		3		ns		
OE to output in low impedance	tolz	0		0		ns	Note 2	
CS to output in high impedance	tснz		8		10	ns	Note 2.	
OE to output in high impedance	tонz		8		10	ns		

Note 1. See the output load shown in Fig. 1.

2. See the output load shown in Fig. 2.

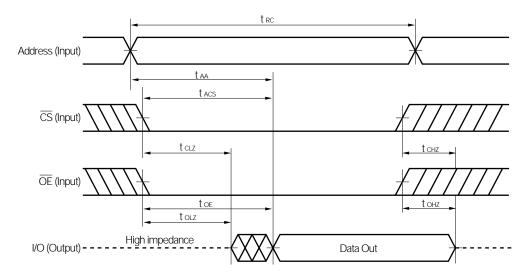
# Read Cycle Timing Chart 1 (Address Access)



**Remark 1.** In read cycle,  $\overline{\text{WE}}$  should be fixed to high level.

2.  $\overline{CS} = \overline{OE} = VIL$ 

## Read Cycle Timing Chart 2 (CS Access)



Caution Address valid prior to or coincident with  $\overline{\text{CS}}$  low level input.

Remark In read cycle, WE should be fixed to high level.

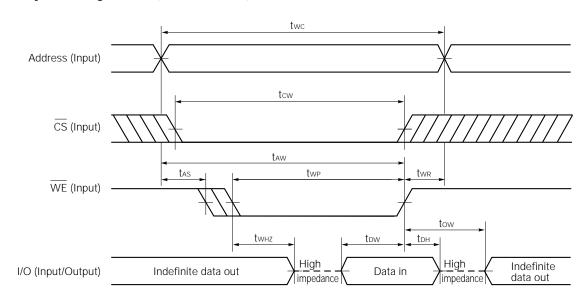


## Write Cycle

Parameter	Cumbal	μPD4340	μPD434008LE-20		μPD434008LE-25		Condition
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	Unit	Condition
Write cycle time	twc	20		25		ns	
CS to end of write	tcw	14		17		ns	
Address valid to end of write	taw	14		17		ns	
Write pulse width	twp	12		15		ns	
Data valid to end of write	tow	10		12		ns	
Data hold time	tон	0		0		ns	
Address setup time	tas	0		0		ns	
Write recovery time	twr	3		3		ns	
WE to output in high impedance	twнz		8		10	ns	Nete
Output active from end of write	tow	0		0		ns	Note

Note See the output load shown in Fig. 2.

## Write Cycle Timing Chart 1 (WE Controlled)

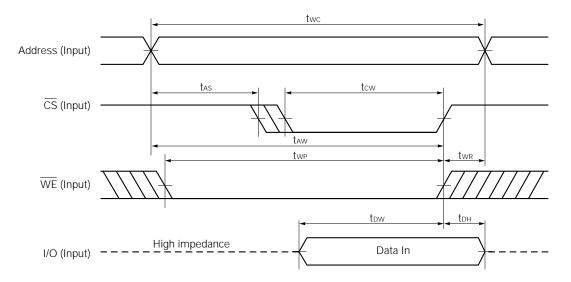


Caution  $\overline{\text{WE}}$  should be fixed to high level during address transition.

- **Remark 1.** Write operation is done during the overlap time of a low level  $\overline{CS}$  and a low level  $\overline{WE}$ .
  - 2. When  $\overline{WE}$  is at low level, I/O pins are always high impedance. When  $\overline{WE}$  is at high level, read operation is executed. Therefore  $\overline{OE}$  should be high level to make I/O pins high impedance.
  - 3. twR is measured between rising edge of  $\overline{CS}$  or  $\overline{WE}$ , whichever occurs first, and end of twc.
  - 4. twnz is measured at Vol + 200 mV and Von 200 mV with the output load shown in Fig. 2.
  - 5. tow is measured at  $\pm$  200 mV from steady state voltage with the output load shown in Fig. 2.



## **★** Write Cycle Timing Chart 2 (CS Controlled)



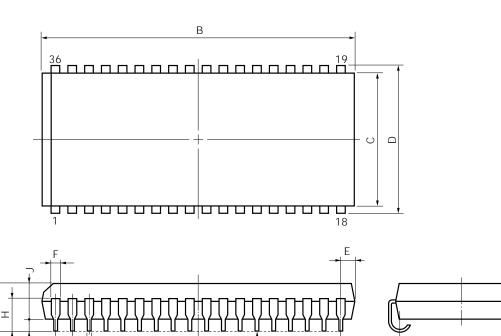
Caution  $\overline{\text{CS}}$  should be fixed to high level during address transition.

- **Remark 1.** Write operation is done during the overlap time of a low level  $\overline{CS}$  and a low level  $\overline{WE}$ .
  - 2. twR is measured between rising edge of  $\overline{CS}$  or  $\overline{WE}$ , whichever occurs first, and end of twc.
  - 3. twnz is measured at Vol + 200 mV and Von 200 mV with the output load shown in Fig. 2.



# Package Drawing

# 36 PIN PLASTIC SOJ (400 mil)



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#### NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

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P36LE-400A

ITEM	MILLIMETERS	INCHES
В	23.6±0.2	0.929±0.008
С	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.005±0.1	0.040+0.004
F	0.74	0.029
G	3.5±0.2	0.138±0.008
Н	2.545±0.2	0.100±0.008
1	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
М	0.40±0.10	0.016+0.004
N	0.12	0.005
Р	9.4±0.20	0.370±0.008
Q	0.1	0.004
Т	R 0.85	R 0.033
U	0.20 +0.10 -0.05	0.008+0.004

NEC  $\mu$ PD434008

## **★ RECOMMENDED SOLDERING CONDITIONS**

Please consult with our sales offices for soldering conditions of the  $\mu$ PD434008.

## TYPE OF SURFACE MOUNT DEVICE

 $\mu$ PD434008LE: 36-pin plastic SOJ (400 mil)



#### NOTES FOR CMOS DEVICES -

## 1) PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

## (2) HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

# (3) STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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