National Semiconductor

DM54190/DM74190, DM54191/DM74191 Synchronous Up/Down Counters with Mode Control

General Description

These circuits are synchronous, reversible, up/down counters. The 191 is a 4-bit binary counter and the 190 is a BCD counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement; which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

- Counts 8-4-2-1 BCD or binary
- Single down/up count control line
- Count enable control input
- Ripple clock output for cascading
- Asynchronously presettable with load control
- Parallel outputs
- Cascadable for n-bit applications
- Average propagation delay 20 ns
- Typical clock frequency 25 MHz
- Typical power dissipation 325 mW

Absolute Maximum Ratings (Note 1)

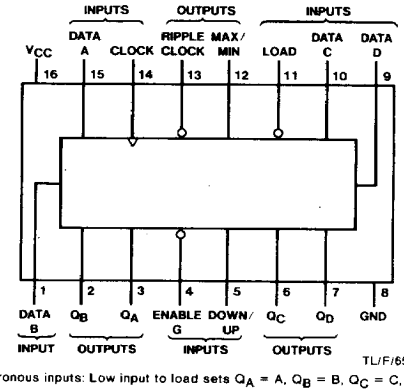
Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

6

Connection Diagram

Dual-In-Line Package



TL/F/6562-1

Asynchronous inputs: Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

54190 (J) **74190 (N)**
54191 (J) **74191 (N)**

Recommended Operating Conditions

Sym	Parameter		DM54190, 191			DM74190, 191			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		20	0		20	MHz
t_W	Pulse Width	Clock	25			25			ns
		Load	35			35			
t_{SU}	Data Setup Time		28			28			ns
t_H	Hold Time		0			0			ns
t_{REL}	Load Release Time		30			30			nS
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'190 and '191 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Enable			120	μA
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Enable			−4.8	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−65	mA
			DM74	−18		−65	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		65	99	mA
			DM74		65	105	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

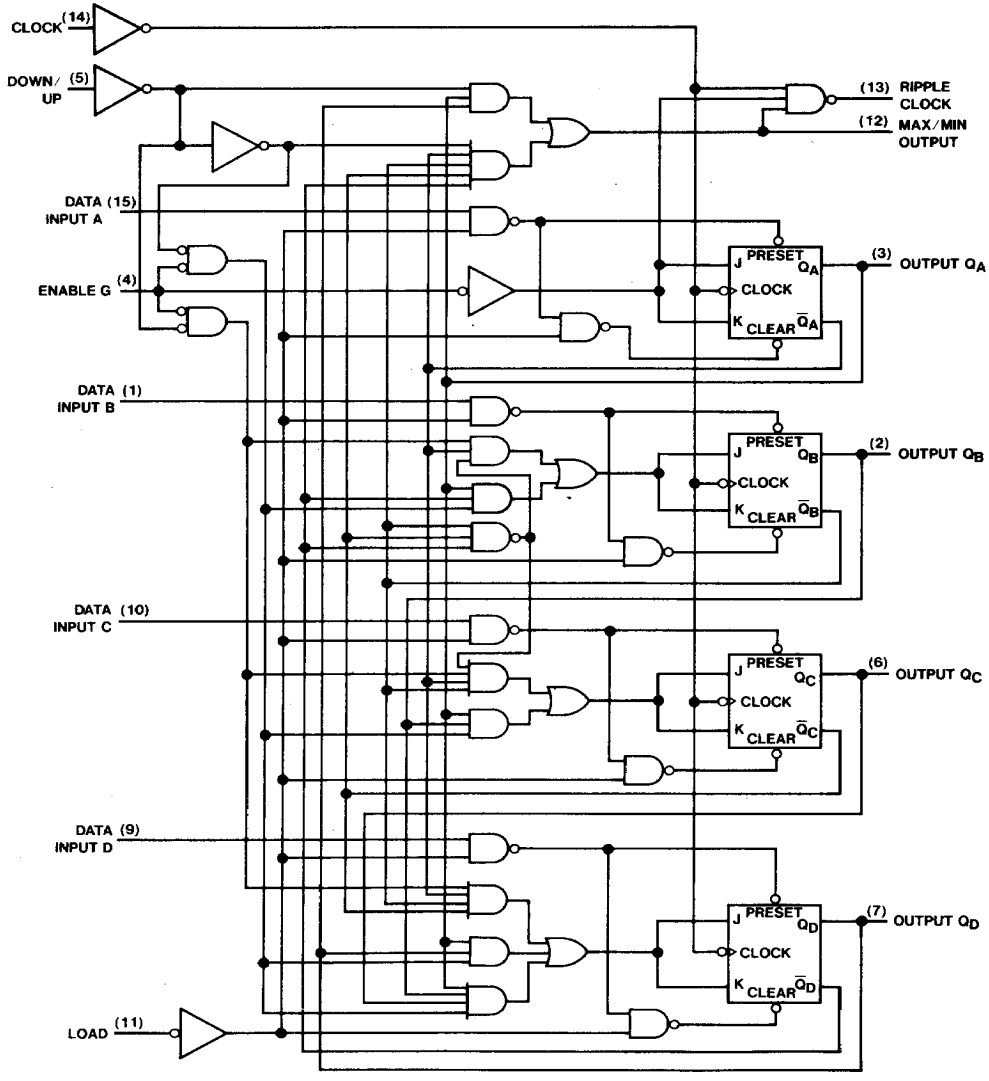
'190 and '191 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		20	25		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		22	33	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		48	70	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Any Q		14	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Any Q		46	70	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		13	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		16	24	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q		16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q		24	36	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Max/Min		28	42	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Max/Min		37	52	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Down/Up to Ripple Carry		30	45	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Down/Up to Ripple Carry		30	45	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Down/Up to Max/Min		21	33	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Down/Up to Max/Min		22	33	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Enable G to Ripple Carry			24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable G to Ripple Carry			24	ns

Logic Diagrams

190 Decade Counter

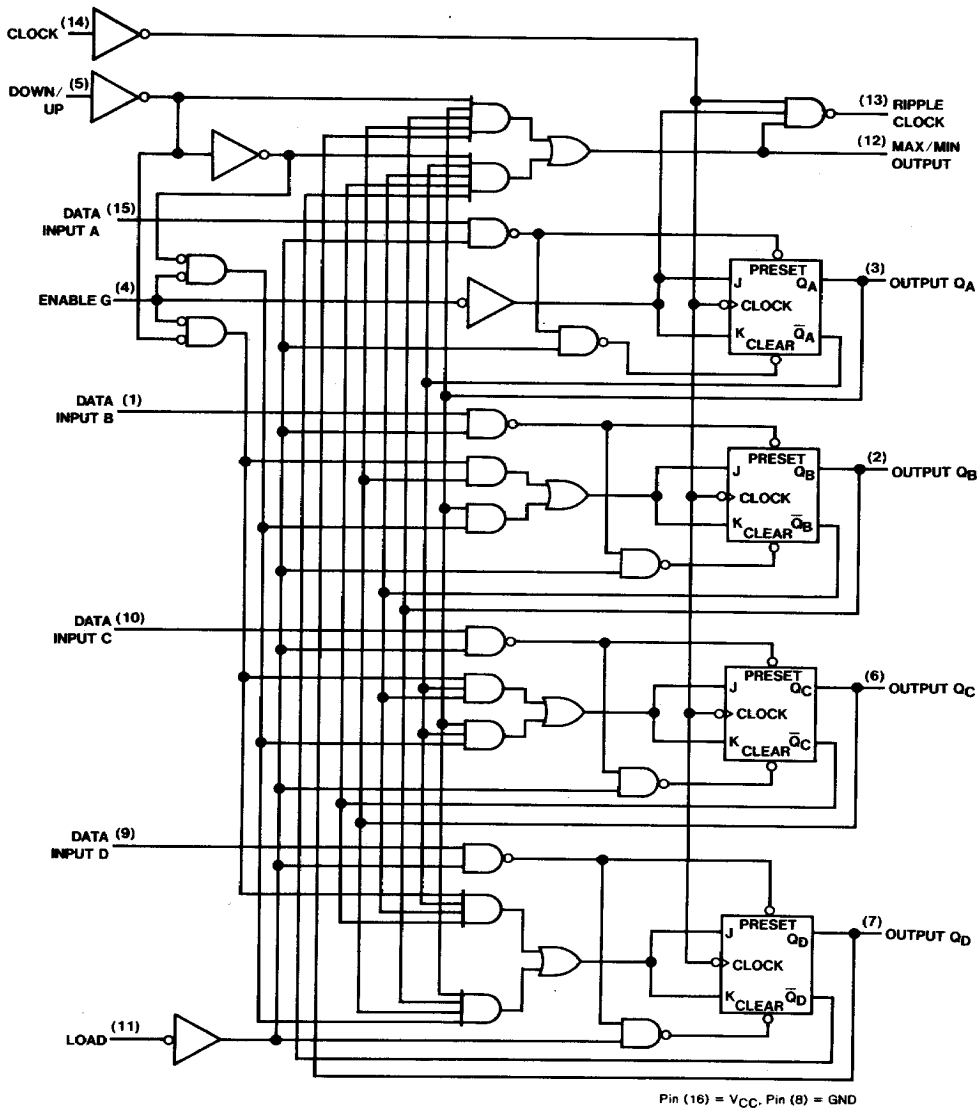


Pin (16) = V_{CC}, Pin (8) = GND

TL/F/6562-2

Logic Diagrams (Continued)

191 Binary Counter

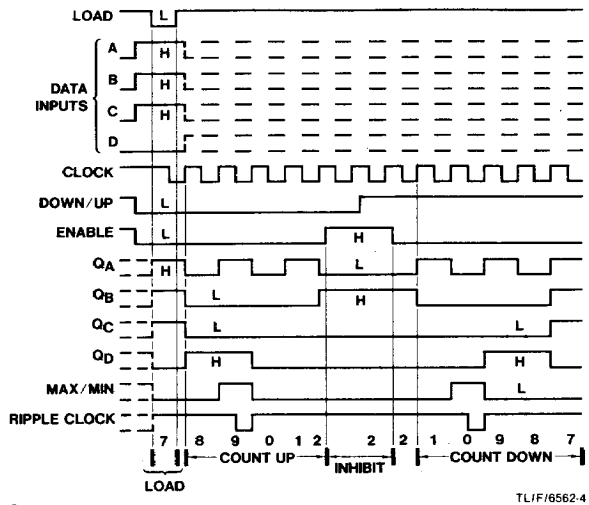


Pin (16) = V_{CC}, Pin (8) = GND

TL/F/6562-3

Timing Diagrams

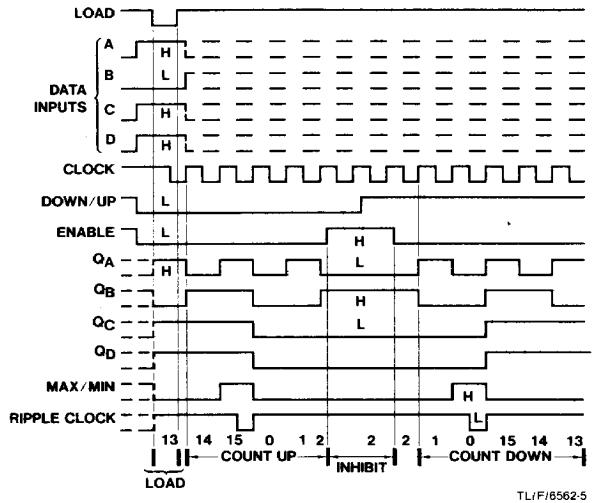
190 Decade Counter
Typical Load, Count, and Inhibit Sequences



TL/F/6562-4

Sequence:
(1) Load (preset) to BCD seven
(2) Count up to eight, nine, zero, one, and two
(3) Inhibit
(4) Count down to one, zero, nine, eight, and seven

191 Decade Counter
Typical Load, Count, and Inhibit Sequences



TL/F/6562-5

Sequence:
(1) Load (preset) to binary thirteen
(2) Count up to fourteen, fifteen, zero, one, and two
(3) Inhibit
(4) Count down to one, zero, fifteen, fourteen, and thirteen