DiskOnChip® Millennium Module 8MByte

M-Systems
Flash Disk Pioneers

Highlights

DiskOnChip Millennium Module is a member of M-Systems' family of DiskOnChip flash disk products. It is available in 8MByte (MB) capacity, 32-pin DIP form factor, and replaces M-Systems' DiskOnChip Millennium 8MB DIP product.

DiskOnChip Millennium Module features:

- Single-chip, plug and play flash disk
- Low power, single 3.3V or 5V power supply
- 8MByte capacity
- Simple, easy-to-integrate interface
- 8KByte memory window
- eXecute In Place (XIP) OS boot functionality
- Proprietary TrueFFS® technology for full hard disk emulation, high data reliability and maximum flash lifetime
- NAND-based flash technology
- Software tools for programming, duplicating, testing and debugging

Reliability

- On-the-fly Reed-Solomon Error Detection Code/Error Correction Code (EDC/ECC)
- Guaranteed data integrity, even after power failure
- Transparent bad block management

TrueFFS Software

- Full hard-disk read/write emulation for transparent file system management
- Patented methods to extend flash lifetime, including:
  - Dynamic virtual mapping
  - Dynamic and static wear leveling
- Support for all major OSs, including: VxWorks, Windows CE, Windows NT, Linux, Nucleus and QNX
- Operates with TrueFFS Software Development Kit (SDK) in OS-less environment

Hardware Compatibility

- 32-pin DIP, JEDEC standard EEPROM-compatible pinout
- Compatible with all major CPUs, including x86, StrongARM, XScale, Geode® SCxxxx, PowerPC™ MPC8xx, MediaGX, 68K, MIPS, SuperH™ SH-x
- 8-bit, 16-bit and 32-bit bus architecture support

Compatibility with Millennium DIP

- Hardware compatibility
  - Pinout
  - Timing
- Fully software compatible (no need to upgrade TrueFFS)
- Same socket on the target platform can be used when migrating from DiskOnChip Millennium 8MB DIP

Applications

- Embedded systems
- Internet access devices
- Internet set-top boxes, interactive TVs, web browsers
- WBT, thin clients, network computers
- Routers, switches, networking equipment
- Web phones, Car PCs, DVD, HPC
- Automotive computing
- Point of sale (POS) terminals, industrial PCs
- Medical equipment

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1. Introduction

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Section 4: TrueFFS technology, including power failure management

Section 5: Using DiskOnChip Millennium Module as a boot device

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Section 7: Environmental, electrical, timing and product specifications

Section 8: Information on ordering DiskOnChip Millennium Module

To contact M-Systems' worldwide offices for general information and technical support, please see the listing on the back cover, or visit M-Systems' website (www.m-sys.com).

2. Product Overview

2.1 Product Description

DiskOnChip Millennium Module, a member of M-Systems' DiskOnChip product family, is a single-chip, solid-state flash disk in a standard 32-pin DIP package that incorporates a disk controller with flash memory.

DiskOnChip Millennium Module is used in a wide range of products, such as set-top boxes, thin clients, thin servers, network computers, and portable computers. DiskOnChip Millennium Module has a simple SRAM-like interface for easy integration. Since DiskOnChip Millennium Module fits into a standard socket, no cables or extra space is required (unlike IDE drives). It is easy to use and reduces integration overhead. DiskOnChip Millennium Module is therefore a very attractive alternative to conventional hard and floppy disk drives.

M-Systems' patented TrueFFS software technology fully emulates a hard disk to manage the files stored on DiskOnChip Millennium Module. This transparent file system management enables read/write operations that are identical to a standard, sector-based hard disk. In addition, TrueFFS employs various patented methods, such as dynamic virtual mapping, dynamic and static wear-leveling, and automatic bad-block management to ensure high data reliability and to maximize flash lifetime. TrueFFS binary drivers are available for a wide range of popular OSs, including VxWorks, Windows CE, Windows NT, Linux, Nucleus and QNX. Customers developing for target platforms not supported by TrueFFS binary drivers can use the TrueFFS Software Development Kit (SDK). For customized boot solutions, M-Systems provides the DiskOnChip Boot Software Development Kit (BDK).

DiskOnChip Millennium Module is available in 8MB capacity, and is hardware and software compatible with DiskOnChip Millennium DIP 8MB. Only the mechanical dimensions differ slightly from DiskOnChip Millennium DIP 8MB. Please refer to Section 7.6 for further information on mechanical dimensions.

Note: The same socket on the target platform can be used when migrating from DiskOnChip Millennium 8MB DIP to DiskOnChip Millennium Module.

DiskOnChip Millennium Module is shipped as a plug-and-play device that is fully tested and formatted, and programmed with a DOS driver. Future driver, software or content upgrades, or formatting, can be made on-board or off-board using M-Systems' DiskOnChip utilities and accessories.

2.2 Pin Assignment

See Figure 1 for the DiskOnChip Millennium Module pinout.

Note: Pins marked NC are not connected internally.

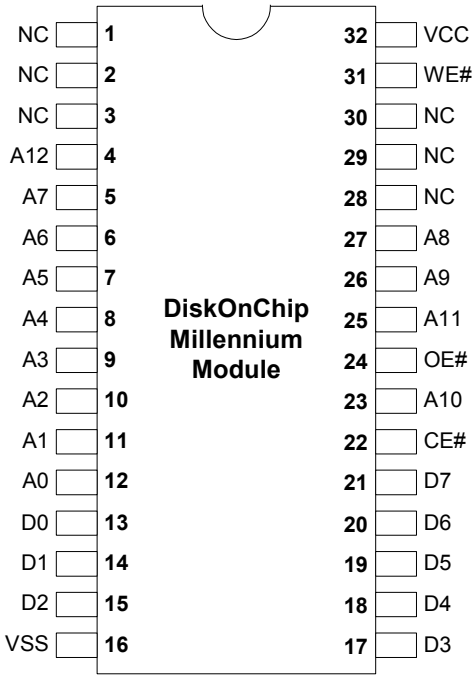

Figure 1: DiskOnChip Millennium Module Pin Diagram

2.3 System Interface

See Figure 2 for a simplified I/O diagram.

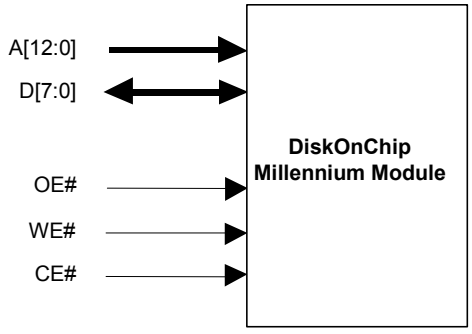

Figure 2: Simplified I/O Diagram

2.4 Signal Descriptions

See Table 1 for brief signal descriptions, presented in logic groups, based on the pin assignments in Figure 1.

Table 1: Signal Descriptions DiskOnChip Millennium Module

Signal	Pin No.	Input Type	Description	Signal Type
System Interface				
A[12:0]	4-12, 23, 25-27	ST	Address bus	Input
D[7:0]	13-15, 17-21	IN	Data bus	Input/ Output
CE#	22	ST	Chip Enable, active low	Input
OE#	24	ST	Output Enable, active low	Input
WE#	31	ST	Write Enable, active low	Input
Power				
VCC	32	-	Device supply. Requires a 10 nF and 0.1 µF capacitor.	Supply
VSS	16	-	Ground	Supply
Reserved				
NC	1, 2, 3, 28, 29, 30	-	Not Connected. These signals are not connected internally and may be left floating, or connected to VCC, VSS or any other logic signal.	

The following abbreviations are used:

IN Standard (non-Schmidt) input
ST Schmidt Trigger input

3. Theory of Operation

3.1 Major Functional Blocks

DiskOnChip Millennium Module consists of the following major functional blocks, as shown in Figure 3:

- **System Interface** for host interface.
- **Boot Block** that contains 512 bytes of boot code, usually required for recognition during the BIOS expansion search in PC architectures.
- **Reed-Solomon-based Error Detection and Error Correction Code (EDC/ECC)** for on-the-fly error handling.
- **Flash Control** block that contains registers responsible for transferring the address, data and control information between the TrueFFS driver and the flash media.

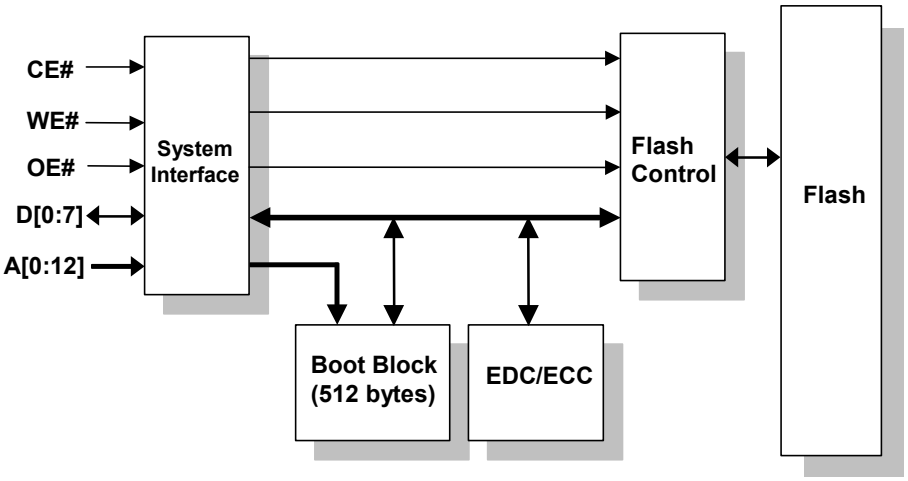

Figure 3: DiskOnChip Millennium Module Simplified Block Diagram

3.1.1 System Interface

The system interface block provides an easy-to-integrate SRAM/EEPROM-like interface to DiskOnChip Millennium Module, enabling it to interface with various CPU interfaces, such as a local bus, ISA bus, SRAM interface, EEPROM interface or any other compatible interface. In addition, the EEPROM-like interface enables direct access to the Programmable Boot Block to permit XIP functionality during system initialization.

A 13-bit wide address bus enables access to the DiskOnChip Millennium Module 8KB memory window (as shown in Figure 4). The Chip Enable (CE#), Write Enable (WE#) and Output Enable (OE#) signals trigger read and write cycles. A write cycle occurs while both the CE# and the WE# inputs are asserted. Similarly, a read cycle occurs while both the CE# and OE# inputs are asserted. Note that DiskOnChip Millennium Module does not require a clock signal. The CE#, WE# and OE# signals trigger the controller (e.g., system interface block, bus control and data pipeline) and flash access.

3.1.2 Boot Block with eXecute In Place (XIP) Capability

During boot-up, code must be executed directly from the flash media, rather than first copied to the host RAM and then executed from there. This direct XIP code execution functionality is essential for booting.

The first 2KB and last 2KB (out of a total of 8KB) of the DiskOnChip Millennium Module memory window each include a single programmable, fail-safe Programmable Boot Block of 512 bytes. These 512 bytes are aliased four times in each 2KB. The last 2KB window is aliased to the first 2KB window, thereby delivering a 512-byte boot block aliased a total of eight times.

The Programmable Boot Block can be used by the CPU to fetch and eXecute In Place (XIP) instructions at boot time. The boot block usually includes basic hardware initialization code and the IPL (Initial Program Loader), which loads the rest of the platform initialization code and the SPL (Secondary Program Loader). Loading the OS and executing the application follow these steps.

In PC architectures, the boot block is responsible for replying to the BIOS expansion search. After the BIOS identifies DiskOnChip Millennium Module as a valid BIOS expansion device, it executes the code stored in the Programmable Boot Block. The BIOS then loads the TrueFFS software from flash memory to the host memory, delivering full disk capabilities to the OS.

3.1.3 Error Detection Code/Error Correction Code (EDC/ECC)

NAND flash, being an imperfect memory, requires error handling. DiskOnChip Millennium Module implements Reed-Solomon Error Detection Code (EDC). A hardware-generated, 6-byte error detection signature is computed each time a page (512 bytes) is written to or read from DiskOnChip.

The TrueFFS driver implements complementary Error Correction Code (ECC). Unlike error detection, which is required on every cycle, error correction is relatively seldom required, hence implemented in software. The combination of DiskOnChip's built-in EDC mechanism and the TrueFFS driver ensures highly reliable error detection and correction, while providing maximum performance.

The following detection and correction capability is provided for each 512 bytes:

- Corrects up to two 10-bit symbols, including two random bit errors.
- Corrects single bursts up to 11 bits.
- Detects single bursts up to 31 bits and double bursts up to 11 bits.
- Detects up to 4 random bit errors.

3.1.4 Flash Control

The Flash Control block contains registers responsible for transferring the address, data and control information between the TrueFFS driver and the flash media. Additional registers are used to monitor the status of the flash media (ready/busy) and of the DiskOnChip controller.

3.2 Modes of Operation

DiskOnChip Millennium Module can operate in two modes:

- Normal mode: The device responds to every valid hardware cycle. While in this mode, all sections respond to valid read and write cycles.
- Reset mode: The device ignores all write cycles, and returns predetermined values for all read cycles.

Mode changes can occur due to any of the following events:

- A valid write sequence to the Control register
- Triggering the boot detector circuit, which enables automatic driver loading in a PC environment.

3.3 8KB Memory Window

The memory map of the DiskOnChip Millennium Module occupies a total address space of 8KB consisting of four 2KB sections, as depicted in Figure 4 and described below.

- Section 0: Programmable Boot Block
  This section includes data that is typically used for booting code from the CPU. The available size is 512 bytes, aliased 4 times in the 2KB section.
- Section 1: Flash Area Window
  Used as a window to the flash media for data to be written or read.
- Section 2: Control Registers
  Used to control the behavior of DiskOnChip Millennium Module and the flash media.
- Section 3: Programmable Boot Block
  This section includes data that is typically used for booting code from the CPU. The available size is 512 bytes, aliased four times in the 2KB section.

When in Reset mode, read cycles from sections 1 and 2 always return the value 00H to create a fixed and known checksum. When in Normal mode, these two sections are used for the internal registers. The 512 bytes of the Programmable Boot Block are aliased four times, in section 0 and section 3, to support systems that search for a checksum at the boot stage both from the top and bottom of memory. The addresses described here are relative to the absolute starting address of the 8KB memory window.

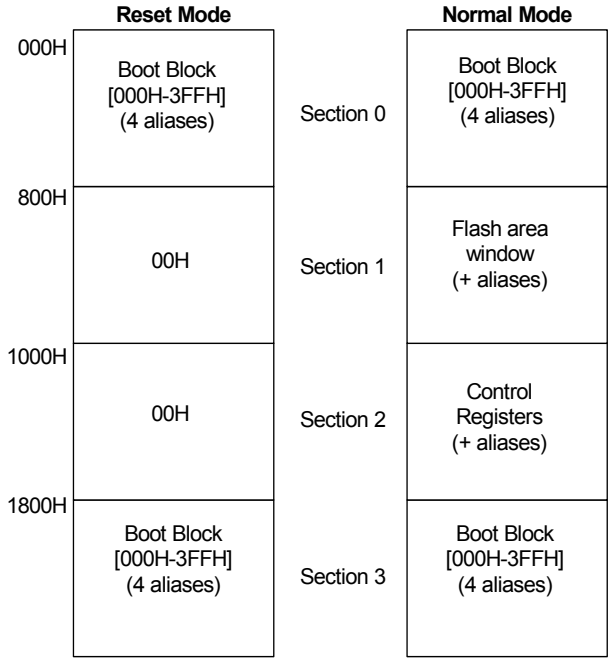

Figure 4: DiskOnChip Millennium Module Memory Map

4. TrueFFS Technology

4.1 General Description

M-Systems' patented TrueFFS technology was designed to maximize the benefits of flash memory while overcoming inherent flash limitations that would otherwise reduce its performance, reliability and lifetime. TrueFFS emulates a hard disk, making it completely transparent to the OS. In addition, since it operates under the OS file system layer (see Figure 5), it is completely transparent to the application.

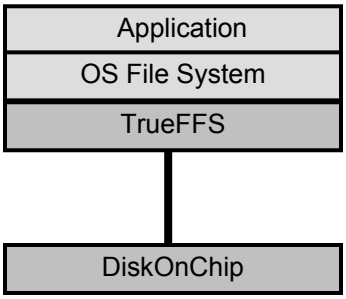

Figure 5: TrueFFS Location in System Hierarchy

TrueFFS technology support includes:

- Binary driver support for all major OSs
- TrueFFS Software Development Kit (TrueFFS SDK)
- Boot Software Development Kit (BDK)
- Support for all major CPUs, including 8, 16 and 32-bit bus architectures

TrueFFS technology features:

- Block device API
- Flash file system management
- Bad-block management
- Dynamic virtual mapping
- Dynamic and static wear-leveling
- Power failure management
- Implementation of Reed-Solomon EDC/ECC
- Performance optimization
- Compatibility with all DiskOnChip products

4.2 Built-in Operating System Support

The TrueFFS driver is integrated into all major OSs including: Windows CE, Windows NT, Symbian, Linux (various kernels), VxWorks, Nucleus, pSOS, QNX, DOS, and others. For a complete listing of all available drivers, please refer to M-Systems' website http://www.m-sys.com. It is advised to use the latest driver versions that can be downloaded from the DiskOnChip Millennium Module web page on the M-Systems site.

4.3 TrueFFS Software Development Kit (SDK)

The basic TrueFFS Software Development Kit (SDK) provides the source code of the TrueFFS driver. It can be used in an OS-less environment or when special customization of the driver is required for proprietary OSs.

When storing the OS image in a separate partition, TrueFFS SDK also incorporates in its source code the BDK, software that is required for this configuration (this package is also available separately). Please refer to the *DiskOnChip Boot Software Development Kit (BDK)* developer guide for further information on the usage of this software package.

4.4 File Management

TrueFFS accesses the flash memory within DiskOnChip Millennium Module through an 8KB window in the CPU memory space. It provides block device API by using standard file system calls, identical to those used by a mechanical hard disk, to enable reading from and writing to any sector on DiskOnChip. This makes it compatible with any file system and file system utilities, such as diagnostic tools and applications. When using the File Allocation Table (FAT) file system, the data stored on DiskOnChip uses FAT-16.

Note: DiskOnChip Millennium Module is shipped formatted and contains the FAT file system.

4.5 Bad Block Management

NAND flash, being an imperfect storage media, contains some bad blocks that cannot be used for storage because of their high error rates. TrueFFS automatically detects and maps bad blocks upon system initialization, ensuring that they are not used for storage. This management process is completely transparent to the user, who is unaware of the existence and location of bad blocks, while remaining confident of the integrity of data stored.

4.6 Wear-Leveling

Flash memory can be erased a limited number of times. This number is called the *erase cycle limit* or *write endurance limit* and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device. In DiskOnChip Millennium Module, the erase cycle limit of the flash is 1,000,000 erase cycles. This means that after approximately 1,000,000 erase cycles, the erase block begins to make storage errors at a rate significantly higher than the error rate that is typical to the flash.

In a typical application and especially if a file system is used, a specific page or pages are constantly updated (e.g., the page/s that contain the FAT, registry etc.). Without any special handling, these pages would wear out more rapidly than other pages, reducing the lifetime of the entire flash.

To overcome this inherent deficiency, TrueFFS uses M-Systems' patented wear-leveling algorithm. The wear-leveling algorithm ensures that consecutive writes of a specific sector are not written physically to the same page in the flash. This spreads flash media usage evenly across all pages, thereby maximizing flash lifetime. TrueFFS wear-leveling extends the flash lifetime 10 to 15 years beyond the lifetime of a typical application.

4.6.1 Dynamic Wear-Leveling

TrueFFS uses statistical allocation to perform dynamic wear-leveling on newly written data. This not only minimizes the number of erase cycles per block, it also minimizes the total number of erase cycles. Because a block erase is the most time-consuming operation, dynamic wear-leveling has a major impact on overall performance. This impact cannot be noticed during the first write to flash (since there is no need to erase blocks beforehand), but it is more and more noticeable as the flash media becomes full.

4.6.2 Static Wear-Leveling

Areas on the flash media may contain static files, characterized by blocks of data that remain unchanged for very long periods of time, or even for the whole device lifetime. If wear-leveling were only applied on newly written pages, static areas would never be cycled. This limited application of wear-leveling would lower life expectancy significantly in cases where flash memory contains large static areas. To overcome this problem, TrueFFS forces data transfer in static areas as well as in dynamic areas, thereby applying wear-leveling to the entire media.

4.7 Power Failure Management

TrueFFS uses algorithms based on “erase after write” instead of "erase before write" to ensure data integrity during normal operation and in the event of a power failure. Used areas are reclaimed for erasing and writing the flash management information into them only *after* an operation is complete. This procedure serves as a check on data integrity.

The “erase after write” algorithm is also used to update and store mapping information on the flash memory. This keeps the mapping information coherent even during power failures. The only mapping information held in RAM is a table pointing to the location of the actual mapping information. This table is reconstructed during power-up or after reset from the information stored in the flash memory.

To prevent data from being lost or corrupted, TrueFFS uses the following mechanisms:

- When writing, copying, or erasing the flash device, the data format remains valid at all intermediate stages. Previous data is never erased until the operation has been completed and the new data has been verified.
- A data sector cannot exist in a partially written state. Either the operation is successfully completed, in which case the new sector contents are valid, or the operation has not yet been completed or has failed, in which case the old sector contents remain valid.

4.8 Error Detection/Correction

TrueFFS implements a Reed-Solomon Error Correction Code (ECC) algorithm to ensure data reliability. Refer to Section 3.1.3 for further information on the EDC/ECC mechanism.

4.9 Special Features through I/O Control (IOCTL) Mechanism

In addition to standard storage device functionality, the TrueFFS driver provides extended functionality. This functionality goes beyond simple data storage capabilities to include features such as: format the media, read/write protect, binary partition(s) access, flash defragmentation and other options. This unique functionality is available in all TrueFFS-based drivers through the standard I/O control command of the native file system.

For further information, please refer to *Extended Functions of the TrueFFS Driver for DiskOnChip* developer guide, available on M-Systems’ website (www.m-sys.com).

4.10 Compatibility

The TrueFFS driver supports all released DiskOnChip products. Upgrading from one product to another requires no additional software integration.

Note: When migrating from DiskOnChip Millennium 8MB DIP, no software change is required.

When using different drivers (e.g. TrueFFS SDK, BDK, BIOS extension firmware, etc.) to access DiskOnChip Millennium Module, the user must verify that all software is based on the same code base version. It is also important to use only tools (e.g. DFORMAT, DINFO, GETIMAGE, etc.) derived from the same version as the firmware version and the TrueFFS drivers used in the application. Failure to do so may lead to unexpected results, such as lost or corrupted data. The driver and firmware version can be verified by the sign-on messages displayed, or by the version information stored in the driver or tool.

5. Boot Procedure in PC-Compatible Platforms

The DiskOnChip Millennium Module default firmware contains drivers to enable it to perform as the OS boot device under DOS. For other OSs, please refer to the TrueFFS driver *readme* file.

When used in PC-compatible platforms, DiskOnChip Millennium Module is connected to an 8KB memory window in the BIOS expansion memory range, typically located between 0C8000H to 0EFFFFH. During the boot process, the BIOS loads the TrueFFS firmware into the PC memory and installs DiskOnChip Millennium Module as a disk drive in the system. When the operating system is loaded, DiskOnChip Millennium Module is recognized as a standard disk. No external software is required to boot from DiskOnChip. Figure 6 illustrates the location of the DiskOnChip Millennium Module memory window in the PC memory map.

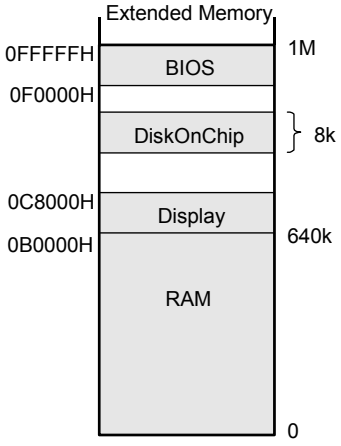

Figure 6: DiskOnChip Millennium Module Memory Window in PC Memory Map

After reset, the BIOS code first executes the Power On Self-Test (POST) and then searches for all expansion ROM devices. When DiskOnChip is found, the BIOS code executes from it the IPL (Initial Program Loader) code, located in the boot block. This code loads the TrueFFS driver into system memory, installs DiskOnChip Millennium Module as a disk in the system, and then returns control to the BIOS code. The operating system subsequently identifies DiskOnChip as an available disk. TrueFFS responds by emulating a hard disk.

From this point onward, DiskOnChip Millennium Module appears as a standard disk drive. It is assigned a drive letter and can be used by any application, without any modifications to either the BIOS set-up or the autoexec.bat/config.sys files. DiskOnChip Millennium Module can be used as the only disk in the system, with or without a floppy drive, and with or without hard disks.

The drive letter assigned depends on how DiskOnChip Millennium Module is used in the system, as follows:

- If DiskOnChip Millennium Module is used as the only disk in the system, the system boots directly from it and assigns drive C.
- If DiskOnChip Millennium Module is used with other disks in the system:
  - DiskOnChip Millennium Module can be configured as the last drive (the default configuration). The system assigns drive C to the hard disk and drive D to DiskOnChip Millennium Module.
  - Alternatively, DiskOnChip Millennium Module can be configured as the system's first drive. The system assigns drive D to the hard disk and drive C to DiskOnChip Millennium Module.
- If DiskOnChip Millennium Module is used as the OS boot device when configured as drive C, it must be formatted as a bootable device by copying the OS files onto it. This is done by using the SYS command when running DOS.

6. Design Considerations

6.1 Design Environment

DiskOnChip Millennium Module provides a complete design environment consisting of:

- Evaluation Boards (EVB) for enabling software integration and development with DiskOnChip Millennium Module, even before the target platform is available. EVBs for ISA and PCI buses are available for immediate plug and play usage.
- Programming solutions:
  - GANG programmer
  - Programming house
- TrueFFS Software Development Kit (SDK) and BDK
- DOS utilities:
  - DFORMAT
  - GETIMG/PUTIMG
  - DINFO
- Documentation:
  - Data sheet
  - Application notes
  - Technical notes
  - Articles
  - White papers

Please visit the M-Systems website (www.m-sys.com) for the most updated documentation, utilities and drivers.

6.2 System Interface

6.2.1 Standard Interface

DiskOnChip Millennium Module uses an SRAM-like interface that can easily be connected to any microprocessor bus. With a standard interface, it requires 13 address lines, 8 data lines and basic memory control signals (CE#, OE#, WE#), as shown in Figure 7. Typically, DiskOnChip Millennium Module can be mapped to any free 8KB memory space. In a PC-compatible platform, it is usually mapped into the BIOS expansion area. If the allocated memory window is larger than 8KB, an automatic anti-aliasing mechanism prevents the firmware from being loaded more than once during the ROM expansion search.

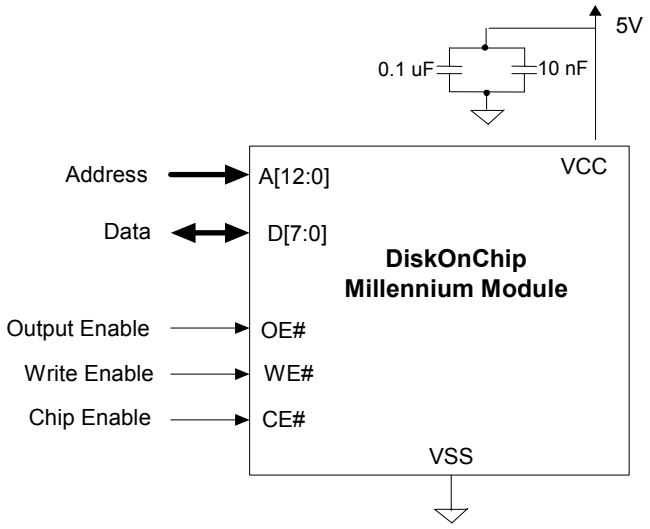

Figure 7: DiskOnChip Millennium Module System Interface

Notes: 1. The 0.1 µF and 10 nF low-inductance high-frequency capacitors must be attached to the device's VCC pin. These capacitors must be placed as close as possible to the package leads.

2. DiskOnChip Millennium Module is an edge-sensitive device. CE#, OE# and WE# should be properly terminated (according to board layout, serial parallel or both terminations) to avoid signal ringing.

6.2.2 Signal Connections

DiskOnChip Millennium Module uses standard SRAM-like control signals, which should be connected as follows:

- Address (A[12:0]) – To the host address bus.
- Data (D[7:0]) – To the host data bus.
- Write (WE#) and Output Enable (OE#) – To the host WR# and RD# signals, respectively.
- Chip Enable (CE#) – To the memory address decoder.

DiskOnChip Millennium Module derives its internal clock signal from the CE#, OE# and WE# inputs. Since access to DiskOnChip Millennium Module registers is volatile, much like a FIFO or UART, ensure that these signals have clean rising and falling edges, and are free from ringing that can be interpreted as multiple edges. PC board traces for these three signals must either be kept short or properly terminated to guarantee proper operation.

6.3 Platform-Specific Issues

The following section describes hardware design issues.

6.3.1 Wait State

Wait states can be implemented only when DiskOnChip Millennium Module is designed in a bus that supports a Wait state insertion, and supplies a WAIT signal.

6.3.2 Big and Little Endian Systems

PowerPC, ARM, and other RISC processors can use either Big or Little Endian systems. DiskOnChip uses the Little Endian system. Therefore, bits D[7:0] are its Least Significant Byte (LSB). Within the byte, bit D0 and bit D8 are the least significant bits. When connecting DiskOnChip Millennium Module to a device that supports the Big Endian system, make sure that the bytes of the CPU and DiskOnChip Millennium Module match.

Note: Certain processors, such as PowerPC, also change the bit ordering within the bytes. Failing to follow the designated order results in improper connection of DiskOnChip Millennium Module and prevents the TrueFFS driver from identifying DiskOnChip Millennium Module.

For further information on how to connect DiskOnChip Millennium Module to support CPUs that use the Big Endian system, refer to the application note for the relevant CPU.

6.3.3 Working with 8/16/32-Bit Systems

TrueFFS supports a wide range of OSs (see Section 4.2). The TrueFFS driver is set to work in 8-bit data access mode as the default. To support 16-bit/32-bit data access modes and their related memory window allocations, TrueFFS must be modified:

- For 16-bit address boundary shifts, shift the address lines by *one*, so that the host address line A1 connects to DiskOnChip Millennium Module address line A0, the host address line A2 connects to DiskOnChip Millennium Module line A1, and so on.
- For 32-bit address boundary shifts, shift the address lines by *two*, so that the host address line A2 connects to DiskOnChip Millennium Module address line A0, the host address line A3 connects to DiskOnChip 2000 line A1, and so on.

In Windows CE and Windows NT Embedded, these changes can be implemented through the registry entries. In all other cases, some minor customization is required in the driver. Please refer to the *readme* of each specific driver for further information.

6.4 Compatibility with DiskOnChip Millennium DIP 8MB

DiskOnChip Millennium Module is fully hardware and software compatible with DiskOnChip Millennium DIP 8MB. No software change is required, and the same TrueFFS version can be used. The same pinout is retained, and the timing specifications are identical. The only difference is in the mechanical dimensions (see Section 7.6 for the specifications).

7. Product Specifications

7.1 Environmental Specifications

7.1.1 Operating Temperature Ranges

Commercial Temperature Range: 0°C to 70°C

Storage Temperature Range: -50°C to +85°C

7.1.2 DiskOnChip Assembly

DiskOnChip Millennium Module is not hermetically sealed. Therefore, it must be assembled after the PCB goes through its final rinse. Assembling DiskOnChip Millennium Module prior to the final rinse phase may cause it to absorb moisture. Failure to adhere to these assembly instructions can lead to device failure not covered by M-Systems' warranty.

Note: DiskOnChip Millennium Module requires a DIP socket on the target platform. Due to its plastic shell and molding material, it cannot be soldered directly to the platform.

7.1.3 Humidity

10% to 90% relative, non-condensing.

7.1.4 Shock and Vibration

Table 2: Reliability Tests

Reliability Test	Test Conditions	Reference Standard
Vibration	100Hz~2000Hz, 15G peak, 3 cycles per axis (1hr.), 3 axes	STD-202F, Method 204D
Mechanical Shock	Half sine shock 50G, 11msec, +/-3 shock per axis, 3 axes	STD-202F, Method 213B

7.2 Endurance

DiskOnChip Millennium Module is based on NAND flash technology, which guarantees a minimum of 1,000,000 erase cycles. Due to the TrueFFS wear-leveling algorithm, the life span of all DiskOnChip products is significantly prolonged. M-Systems' website (www.m-sys.com) provides an online life-span calculator to facilitate application-specific endurance calculations.

7.3 Disk Capacity

Table 3: Disk Capacity (Bytes)

DOS 6.22 (TrueFFS Report)		DOS 6.22	
Formatted Capacity	**Sectors**	**Formatted Capacity**	**Sectors**
8,151,040	15,920	8,128,512	15,876

Note: DiskOnChip Millennium Module is shipped formatted and contains the FAT file system.

7.4 Electrical Specifications

7.4.1 Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings

Parameter	Symbol	Rating[1]	Unit	Notes
DC supply voltage	V_{CC}	-0.3 to 6.0	V	
Input pin voltage	V_{IN}	-0.3 [2] to 6.6	V	
Input pin current	I_{IN}	-10 to 10	mA	+25°C
Lead temperature	T_{LEAD}	260	°C	10 Sec

Notes: 1. Permanent device damage may occur if absolute maximum ratings are exceeded. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. The voltage on any pin may undershoot to -2.0V or overshoot to 8.6V for <20ns.

7.4.2 Capacitance

Table 5: Capacitance

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	V_{IN} =0V		5	12	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V		8	12	pF

7.4.3 DC Electrical Characteristics Over Operating Range

See Table 6 and Table 7 and for DC characteristics for VCC=3.3V or VCC=5V.

Table 6: DC Characteristics VCC=3.3V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	VCC		3.0	3.3	3.6	V
High-level Input Voltage	V_{IH}	VCC = 3.6V	2.1			V
Low-level Input Voltage	V_{IL}				0.7	V
Hysteresis	V_{HYS}	All inputs	0.4			V
High-level Output Voltage	V_{OH}	I_{OH} = I_{OHMAX}	2.4			V
Low-level Output Voltage	V_{OL}	I_{OL} = I_{OLMAX}			0.4	V
Maximum High Level Output Current	I_{OHMAX}	3.0 < VCC <3.6 D outputs	-5			mA
		VCC < 3.0V D outputs	-2			mA
Maximum Low Level Output Current	I_{OLMAX}	VCC > 3.3V	16			mA
		VCC < 4.5V D outputs	5			mA
Input Leakage Current	I_{ILK}				±10	µA
Active Supply Current	I_{CC}	Cycle Time = 100ns Outpus open VCC = 3.3V		16	30	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Standby Supply Current	I_{CCS}	CE# > VCC–0.2V All other inputs: Vin < 0.2V or Vin > VCC-0.2V			100	µA

Table 7: DC Characteristics VCC=5V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	VCC		4.5	5.0	5.5	V
High-level Input Voltage	V_{IH}	VCC = 5.5V	3.2			V
Low-level Input Voltage	V_{IL}				0.7	V
Hysteresis	V_{HYS}	All inputs	0.4			V
High-level Output Voltage	V_{OH}	$I_{OH} = I_{OHMAX}$	2.4			V
Low-level Output Voltage	V_{OL}	$I_{OL} = I_{OLMAX}$			0.4	V
Maximum High Level Output Current	I_{OHMAX}	VCC > 4.5V D outputs	-16			mA
		VCC < 4.5V D outputs	-5			mA
Maximum Low Level Output Current	I_{OLMAX}	VCC > 4.5V D outputs	16			mA
		VCC < 4.5V D outputs	5			mA
Input Leakage Current	I_{ILK}				±10	µA
Active Supply Current	I_{CC}	Cycle Time = 100ns Outpus open VCC = 5.0V		25	45	mA
Standby Supply Current	I_{CCS}	CE# > VCC–0.2V All other inputs: Vin < 0.2V or Vin > VCC-0.2V			100	µA

7.4.4 AC Operating Conditions

Environmental and timing specifications are based on the following conditions.

Table 8: AC Test Conditions

Parameter	VCCQ=2.7-3.6V
Ambient Temperature (TA)	-40°C to +85°C
Supply Voltage	5V ± 0.5V or 3.3V ± 0.3V
Input Pulse Levels	0.4V to 2.6V
Input Rise and Fall Times	5ns
Input Timing Levels	2.0V
Output Timing Levels	1.5V
Output Load	100pF

7.5 Timing Specifications

7.5.1 Read Cycle Timing

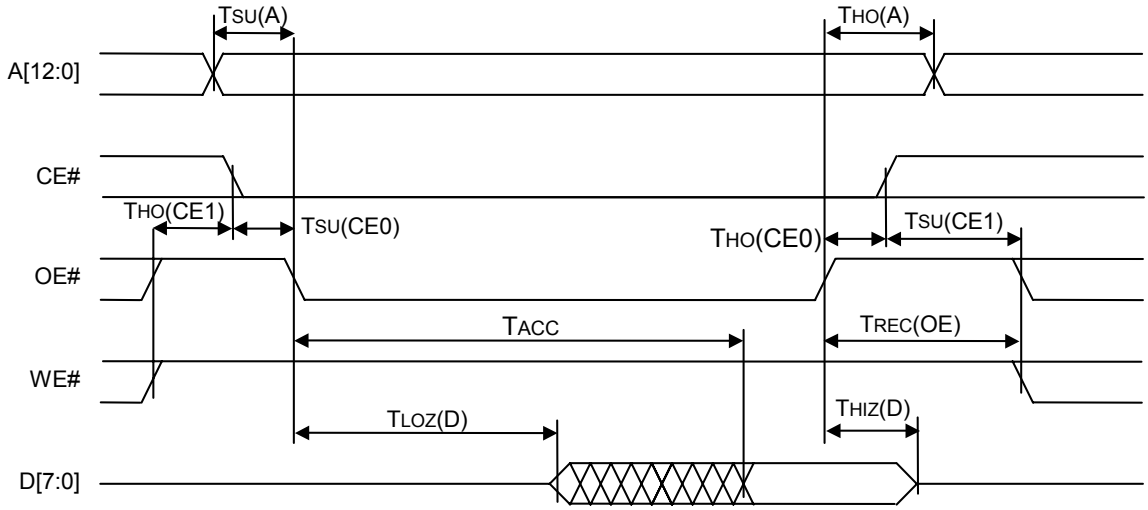

Figure 8: Read Cycle Timing

Table 9: Read Cycle Timing Parameter

Symbol	Description	3.3V		5V		Unit
		Min	Max	Min	Max	
Tsu(A)	Address to OE# ↓ setup time	0		0		ns
Tho(A)	OE# ↓ to Address hold time	0		0		ns
Tsu(CE0)	CE# ↓ to OE# ↓ setup time[1]	—		—		ns
Tho(CE0)	OE# ↑ to CE# ↑ hold time[2]	—		—		ns
Tho(CE1)	OE# or WE# ↑ to CE# ↓ hold time	8		7		ns
Tsu(CE1)	CE# ↑ to WE# ↓ or OE# ↓ setup time	8		7		ns
Trec(OE)	OE# negated to start of next cycle	11		10		ns
Tacc	Read access time (RAM)[3]		130		85	ns
	Read access time (all other addresses)[3]		100		65	ns
Tloz(D)	OE# ↓ to D driven	20		18		ns
Thiz(D)	OE# ↑ to D Hi-Z delay		20		17	ns

1. CE# may be asserted any time before or after OE# is asserted. If CE# is asserted after OE#, all timing relative to when OE# was asserted will be referenced to the time CE# was asserted.

2. CE# may be negated any time before or after OE# is negated. If CE# is negated before OE#, all timing relative to when OE# was negated will be referenced to the time CE# was negated.

3. The boot block is located at addresses 0000~07FFH and 1800H~1FFFH. Registers located at addresses 0800H~17FFH have a faster access time than the boot block. Access to the boot block is not required after the boot process has completed.

7.5.2 Write Cycle Timing Standard Interface

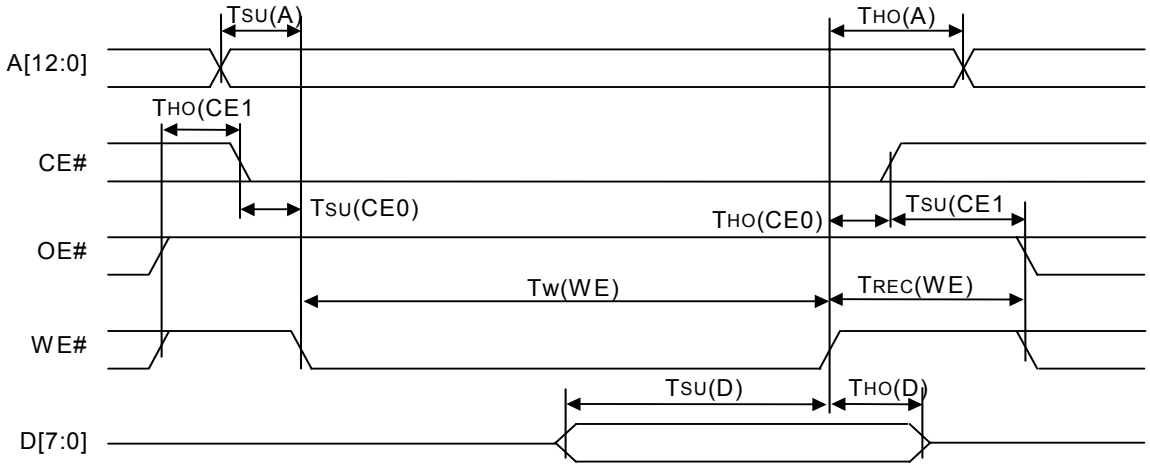

Figure 9: Write Cycle Timing

Table 10: Write Cycle Parameters

Symbol	Description	3.3V		5V		Unit
				Min	Max	
TSU (A)	Address to WE# ↓ setup time	0		0		ns
Tho(A)	WE# ↓ to Address hold time	0		0		ns
Tw(WE)	WE# asserted width	65		46		ns
Tsu (CE0)	CE# ↓ to WE# ↓ setup time[1]	--		--		ns
Tho (CE0)	WE# ↑ to CE# ↑ hold time[2]	--		--		ns
Tho (CE1)	OE# or WE# ↑ to CE# ↓ hold time	8		7		ns
Tsu (CE1)	CE# ↑ to WE# ↓ or OE# ↓ setup time	8		7		ns
Trec (WE)	WE# ↑ to start of next cycle	11		10		ns
Tsu(D)	D to WE# ↑ setup time	43		29		ns
Tho (D)	WE# ↑ to D hold time	0		0		

1. CE# may be asserted any time before or after WE# is asserted. If CE# is asserted after WE#, all timing relative to WE# asserted should be referenced to the time CE# was asserted.

2. CE# may be negated any time before or after WE# is negated. If CE# is negated before WE#, all timing relative to WE# negated will be referenced to the time CE# was negated.

7.5.3 Power-Up Timing

DiskOnChip Millennium Module generates an internal reset pulse on power-up, which is asserted for a maximum of 165 ms after VCC has reached the minimum operating voltage. When the reset condition is met, DiskOnChip Millennium Module initiates the download procedure from flash memory to the Programmable Boot Block.

Host systems accessing DiskOnChip Millennium Module for the first time must conform to the timing requirements shown in Figure 10.

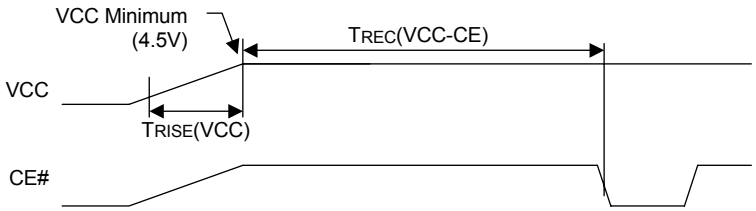

Figure 10: Reset Timing

It is illegal for the host to access DiskOnChip Millennium Module before the internal reset signal has been negated and the download process completed. Therefore, the host must delay TREC(VCC-CE) before the first access to DiskOnChip Millennium Module.

Table 11: Reset Timing Parameters

Symbol	Description	Min	Max	Unit
Trec(VCC-CE)	VCC stable to first access	165		mS
Trise(VCC)[1]	VCC rise time		44	mS

1. Specified as the first positive crossing above 0.5V to the final positive crossing above 3.0V or 4.5V.

7.6 Mechanical Dimensions

See Figure 11 and Table 12for the mechanical dimensions of DiskOnChip Millennium Module.

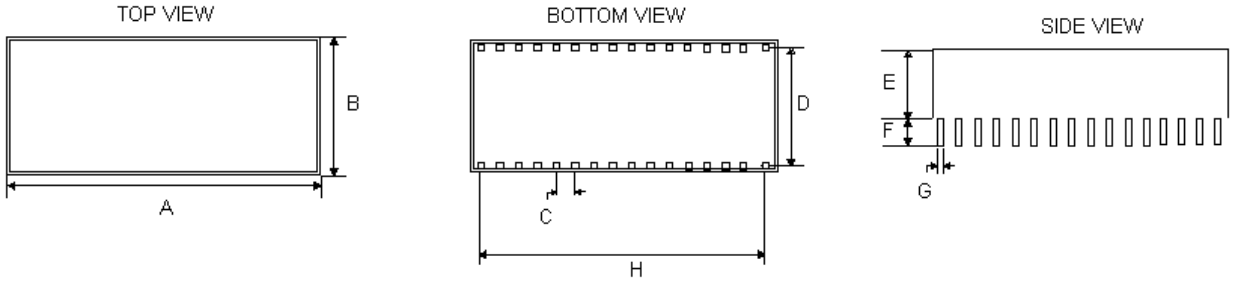

Figure 11: Mechanical Dimensions of DiskOnChip Millennium Module

Table 12: Mechanical Dimensions Parameters

	Millimeters (max.)
A	43.95
B	18.3
C	2.54
D	15.24
E	6.0
F	4.0
G	0.51
H	38.2

8. Ordering Information

MD2802-D08-V

MD:	M-Systems DiskOnChip
2802:	DiskOnChip Millennium Module
D08:	Capacity: 8MB
V	Supply Voltage
	Blank: 5V
	V3: 3.3V

How to Contact Us

Internet: http://www.m-sys.com

General Information: info@m-sys.com

Sales and Technical Information: techsupport@m-sys.com

USA
M-Systems Inc.
8371 Central Ave, Suite A
Newark CA 94560
Phone: +1-510-494-2090
Fax: +1-510-494-5545

China
M-Systems China Ltd.
25A International Business Commercial Bldg.
Nanhu Rd., Lou Hu District
Shenzhen, China 518001
Phone: +86-755-2519-4732
Fax: +86-755-2519-4729

Taiwan
M-Systems Asia Ltd.
Room B, 13 F, No. 133 Sec. 3
Min Sheng East Road
Taipei, Taiwan
R.O.C.
Tel: +886-2-8770-6226
Fax: +886-2-8770-6295

Europe & Israel
M-Systems Ltd.
7 Atir Yeda St.
Kfar Saba 44425, Israel
Tel: +972-9-764-5000
Fax: +972-3-548-8666

Japan
M-Systems Japan Inc.
Asahi Seimei Gotanda Bldg., 3F
Shinagawa-ku Tokyo, 141-0022
Phone: +81-3-5423-8101
Fax: +81-3-5423-8102