NEW FPM DRAM

# DRAM

# 1 MEG x 4 DRAM

## 5V, QUAD CAS PARITY, FAST PAGE MODE

### FEATURES

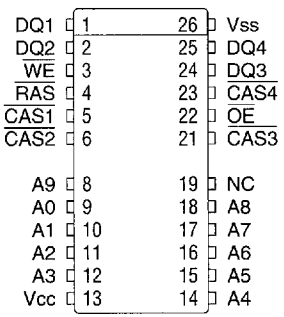
- Four independent $\overline{CAS}$ controls, allowing individual manipulation to each of the four data input/output ports (DQ1 through DQ4).
- Offers a single chip solution to byte-level parity for 36-bit words when using 1 Meg x 4 DRAMs for memory
- Emulates WRITE-PER-BIT at design-in level, with simplified timing constraints
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- 1,024-cycle refresh in 16ms
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN

### OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
- Packages
  - Plastic SOJ (300 mil) — DJ
- Part Number Example: MT4C4004JDJ-7

### PIN ASSIGNMENT (Top View)

**24/26-Pin SOJ**
**(DA-2)**




### KEY TIMING PARAMETERS

| SPEED | tRC | tRAC | tPC | tAA | tCAC | tRP |
|---|---|---|---|---|---|---|
| -6 | 110ns | 60ns | 35ns | 30ns | 15ns | 40ns |
| -7 | 130ns | 70ns | 40ns | 35ns | 20ns | 50ns |

### GENERAL DESCRIPTION

The MT4C4004J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. This 1 Meg x 4 DRAM is unique in that each $\overline{CAS}$ ($\overline{CAS1}$ through $\overline{CAS4}$) controls its corresponding data I/O port in conjunction with $\overline{OE}$ (that is, $\overline{CAS1}$ controls DQ1 I/O port, $\overline{CAS2}$ controls DQ2, $\overline{CAS3}$ controls DQ3 and $\overline{CAS4}$ controls DQ4).

The best way to view the Quad $\overline{CAS}$ function is to imagine the $\overline{CAS}$ inputs going into an OR gate to obtain an internally generated $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on a standard 1 Meg x 4 DRAM device. The key difference is that each $\overline{CAS}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$) on the Quad CAS DRAM.

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits, and the first $\overline{CAS}$ is used to latch the latter 10 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode.

During a WRITE cycle, data-in (Dx) is latched by the falling edge of $\overline{WE}$ or the first $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to the first $\overline{CAS}$ going LOW, the output pin(s) remain open until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output buffer, data-out (Q) is activated and retains the selected cell data until the trailing edge of its corresponding $\overline{CAS}$ occurs (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle ($\overline{OE}$ switching the device from a READ to a WRITE function). The four data inputs and four data outputs are routed through four pins using common I/O, with pin direction controlled by $\overline{WE}$ and $\overline{OE}$.

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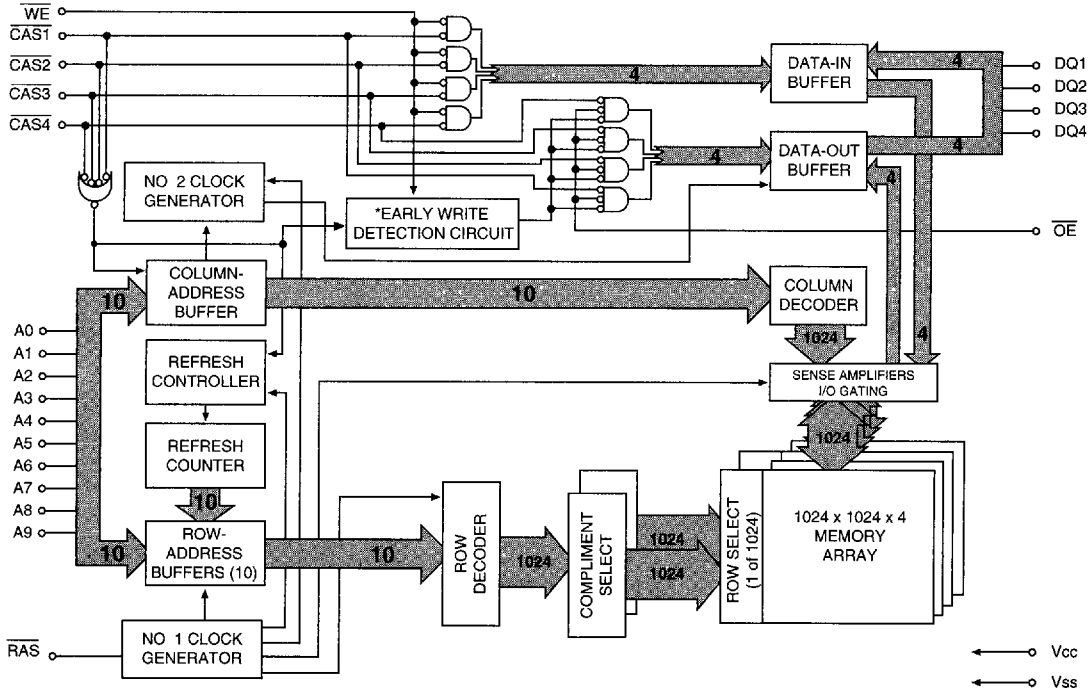
## GENERAL DESCRIPTION (continued)

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by the first $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and all four $\overline{CAS}$ controls HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

## FUNCTIONAL BLOCK DIAGRAM
QUAD CAS




***NOTE:** 1. $\overline{WE}$ LOW prior to first $\overline{CAS}$ LOW, EW detection circuit output is a 1.
2. First $\overline{CAS}$ LOW while $\overline{WE}$ HIGH, EW detection circuit output is a 0; ($\overline{OE}$ will now determine I/O).

## TRUTH TABLE

| FUNCTION | | RAS | CASx | CASy | WE | OE | ADDRESSES | | DQx |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | tR | tC | (DQy always High-Z) |
| Standby | | H | H→X | H→X | X | X | X | X | High-Z |
| READ | | L | L | H | H | L | ROW | COL | Data-Out |
| EARLY WRITE | | L | L | H | L | X | ROW | COL | Data-In |
| READ-WRITE | | L | L | H | H→L | L→H | ROW | COL | Data-Out, Data-In |
| FAST-PAGE-MODE | 1st Cycle | L | H→L | H | H | L | ROW | COL | Data-Out |
| READ | 2nd Cycle | L | H→L | H | H | L | n/a | COL | Data-Out |
| FAST-PAGE-MODE | 1st Cycle | L | H→L | H | L | X | ROW | COL | Data-In |
| EARLY-WRITE | 2nd Cycle | L | H→L | H | L | X | n/a | COL | Data-In |
| FAST-PAGE-MODE | 1st Cycle | L | H→L | H | H→L | L→H | ROW | COL | Data-Out, Data-In |
| READ-WRITE | 2nd Cycle | L | H→L | H | H→L | L→H | n/a | COL | Data-Out, Data-In |
| RAS-ONLY REFRESH | | L | H | H | X | X | ROW | n/a | High-Z |
| HIDDEN | READ | L→H→L | L | H | H | L | ROW | COL | Data-Out |
| REFRESH | WRITE | L→H→L | L | H | L | X | ROW | COL | Data-In |
| CBR REFRESH | | H→L | L | H | H | X | X | X | High-Z |

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## ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to $V_{SS}$ ..... -1V to +7V
Operating Temperature, $T_A$ (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation ..... 1W
Short Circuit Output Current ..... 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) ($V_{CC}$ = 5V ±10%)

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.5 | V | |
| Input High (Logic 1) Voltage, all inputs | $V_{IH}$ | 2.4 | $V_{CC}$+1 | V | |
| Input Low (Logic 0) Voltage, all inputs | $V_{IL}$ | -1.0 | 0.8 | V | |
| INPUT LEAKAGE CURRENT<br>Any input 0V ≤ $V_{IN}$ ≤ 6.5V<br>(All other pins not under test = 0V) | $I_I$ | -2 | 2 | µA | |
| OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ $V_{OUT}$ ≤ 5.5V) | $I_{OZ}$ | -10 | 10 | µA | |
| OUTPUT LEVELS<br>Output High Voltage ($I_{OUT}$ = -5mA) | $V_{OH}$ | 2.4 | | V | |
| Output Low Voltage ($I_{OUT}$ = 4.2mA) | $V_{OL}$ | | 0.4 | V | |

| | | MAX | | | |
|---|---|---|---|---|---|
| PARAMETER/CONDITION | SYMBOL | -6 | -7 | UNITS | NOTES |
| STANDBY CURRENT: (TTL)<br>($\overline{RAS}$ = $\overline{CAS}$ = $V_{IH}$) | $I_{CC1}$ | 2.5 | 2.5 | mA | |
| STANDBY CURRENT: (CMOS)<br>($\overline{RAS}$ = $\overline{CAS}$ = $V_{CC}$ -0.2V) | $I_{CC2}$ | 1 | 1 | 26 | |
| OPERATING CURRENT: Random READ/WRITE<br>Average power supply current<br>($\overline{RAS}$, $\overline{CAS}$, Single Address Cycling: $^tRC$= $^tRC$ [MIN]) | $I_{CC3}$ | 110 | 100 | mA | 3, 4, 39 |
| OPERATING CURRENT: FAST PAGE MODE<br>Average power supply current<br>($\overline{RAS}$ = $V_{IL}$; $\overline{CAS}$, Address Cycling: $^tPC$= $^tPC$ [MIN]) | $I_{CC4}$ | 80 | 70 | mA | 3, 4, 39 |
| REFRESH CURRENT: $\overline{RAS}$ ONLY<br>Average power supply current<br>($\overline{RAS}$ Cycling, $\overline{CAS}$ = $V_{IH}$: $^tRC$= $^tRC$ [MIN]) | $I_{CC5}$ | 110 | 100 | mA | 3, 39 |
| REFRESH CURRENT: CBR<br>Average power supply current<br>($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $^tRC$= $^tRC$ [MIN]) | $I_{CC6}$ | 110 | 100 | mA | 3, 5 |

## CAPACITANCE

| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance: A0-A9 | $C_{I1}$ | | 5 | pF | 2 |
| Input Capacitance: $\overline{RAS}$, $\overline{CAS}$1-4, $\overline{WE}$, $\overline{OE}$ | $C_{I2}$ | | 7 | pF | 2 |
| Input/Output Capacitance: DQ | $C_{IO}$ | | 7 | pF | 2 |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23, 25) ($V_{CC}$ = 5V ±10%)

| AC CHARACTERISTICS | | -6 | | -7 | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Access time from column-address | $^tAA$ | | 30 | | 35 | ns | |
| Column-address hold time (referenced to $\overline{RAS}$) | $^tAR$ | 45 | | 50 | | ns | |
| Column-address setup time | $^tASC$ | 0 | | 0 | | ns | 27 |
| Row-address setup time | $^tASR$ | 0 | | 0 | | ns | |
| Column-address to $\overline{WE}$ delay time | $^tAWD$ | 55 | | 65 | | ns | 21 |
| Access time from $\overline{CAS}$ | $^tCAC$ | | 15 | | 20 | ns | 15, 29 |
| Column-address hold time | $^tCAH$ | 10 | | 15 | | ns | 27 |
| $\overline{CAS}$ pulse width | $^tCAS$ | 15 | 10,000 | 20 | 10,000 | ns | 35 |
| $\overline{CAS}$ hold time (CBR REFRESH) | $^tCHR$ | 10 | | 10 | | ns | 5, 25, 28 |
| Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH | $^tCLCH$ | 10 | | 10 | | ns | 30 |
| $\overline{CAS}$ to output in Low-Z | $^tCLZ$ | 0 | | 0 | | ns | 29 |
| $\overline{CAS}$ precharge time | $^tCP$ | 10 | | 10 | | ns | 16, 32 |
| Access time from $\overline{CAS}$ precharge | $^tCPA$ | | 35 | | 40 | ns | 29 |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | $^tCRP$ | 10 | | 10 | | ns | 28 |
| $\overline{CAS}$ hold time | $^tCSH$ | 60 | | 70 | | ns | 28 |
| $\overline{CAS}$ setup time (CBR REFRESH) | $^tCSR$ | 10 | | 10 | | ns | 5, 25, 27 |
| $\overline{CAS}$ to $\overline{WE}$ delay time | $^tCWD$ | 40 | | 50 | | ns | 21, 27 |
| Write command to $\overline{CAS}$ lead time | $^tCWL$ | 15 | | 20 | | ns | 28 |
| Data-in hold time | $^tDH$ | 10 | | 15 | | ns | 22, 29 |
| Data-in hold time (referenced to $\overline{RAS}$) | $^tDHR$ | 45 | | 55 | | ns | |
| Data-in setup time | $^tDS$ | 0 | | 0 | | ns | 22, 29 |
| Output disable | $^tOD$ | | 15 | | 20 | ns | 38 |
| Output Enable | $^tOE$ | | 15 | | 20 | ns | 23 |
| $\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle | $^tOEH$ | 15 | | 20 | | ns | 37 |
| Output buffer turn-off delay | $^tOFF$ | 3 | 15 | 3 | 20 | ns | 20, 29, 38 |
| $\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle | $^tORD$ | 0 | | 0 | | ns | |
| FAST-PAGE-MODE READ or WRITE cycle time | $^tPC$ | 35 | | 40 | | ns | 31 |

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## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23, 25) ($V_{CC}$ = 5V ±10%)

| AC CHARACTERISTICS | | -6 | | -7 | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| FAST-PAGE-MODE READ-WRITE cycle time | $^tPRWC$ | 85 | | 100 | | ns | 31 |
| Access time from $\overline{RAS}$ | $^tRAC$ | | 60 | | 70 | ns | 14 |
| $\overline{RAS}$ to column-address delay time | $^tRAD$ | 15 | 30 | 15 | 35 | ns | 18 |
| Row-address hold time | $^tRAH$ | 10 | | 10 | | ns | |
| Column-address to $\overline{RAS}$ lead time | $^tRAL$ | 30 | | 35 | | ns | |
| $\overline{RAS}$ pulse width | $^tRAS$ | 60 | 10,000 | 70 | 10,000 | ns | |
| $\overline{RAS}$ pulse width (FAST PAGE MODE) | $^tRASP$ | 60 | 100,000 | 70 | 100,000 | ns | |
| Random READ or WRITE cycle time | $^tRC$ | 110 | | 130 | | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | $^tRCD$ | 20 | 45 | 20 | 50 | ns | 17, 27 |
| Read command hold time (referenced to $\overline{CAS}$) | $^tRCH$ | 0 | | 0 | | ns | 19, 28 |
| Read command setup time | $^tRCS$ | 0 | | 0 | | ns | 27 |
| Refresh period (1,024 cycles) | $^tREF$ | | 16 | | 16 | ms | |
| $\overline{RAS}$ precharge time | $^tRP$ | 40 | | 50 | | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ precharge time | $^tRPC$ | 0 | | 0 | | ns | |
| Read command hold time (referenced to $\overline{RAS}$) | $^tRRH$ | 0 | | 0 | | ns | 19 |
| $\overline{RAS}$ hold time | $^tRSH$ | 15 | | 20 | | ns | 36 |
| READ-WRITE cycle time | $^tRWC$ | 150 | | 180 | | ns | |
| $\overline{RAS}$ to $\overline{WE}$ delay time | $^tRWD$ | 90 | | 100 | | ns | 21 |
| Write command to $\overline{RAS}$ lead time | $^tRWL$ | 15 | | 20 | | ns | |
| Transition time (rise or fall) | $^tT$ | 3 | 50 | 3 | 50 | ns | |
| Write command hold time | $^tWCH$ | 10 | | 15 | | ns | 36 |
| Write command hold time (referenced to $\overline{RAS}$) | $^tWCR$ | 45 | | 55 | | ns | |
| $\overline{WE}$ command setup time | $^tWCS$ | 0 | | 0 | | ns | 21, 27 |
| Write command pulse width | $^tWP$ | 10 | | 15 | | ns | |
| $\overline{WE}$ hold time (CBR REFRESH) | $^tWRH$ | 10 | | 10 | | ns | |
| $\overline{WE}$ setup time (CBR REFRESH) | $^tWRP$ | 10 | | 10 | | ns | |

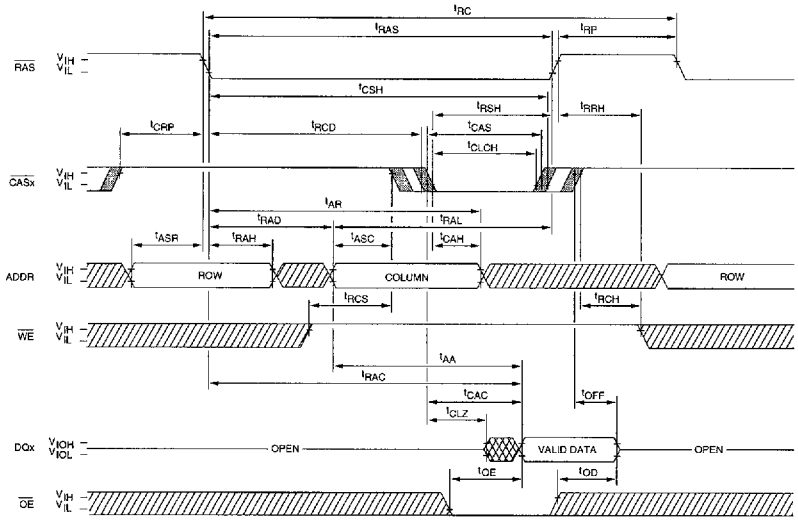
## NOTES

1. All voltages referenced to $V_{SS}$.
2. This parameter is sampled. $V_{CC}$ = 5V ±10%; f = 1 MHz.
3. $I_{CC}$ is dependent on cycle rates.
4. $I_{CC}$ is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial 100µs pause is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the $^tREF$ refresh requirement is exceeded.
8. AC characteristics assume $^tT$ = 5ns.
9. $V_{IH}$ (MIN) and $V_{IL}$ (MAX) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$)
10. In addition to meeting the transition rate specification, all input signals must transit between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
11. If $\overline{CAS}$x = $V_{IH}$, data output is High-Z.
12. If $\overline{CAS}$x = $V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If $^tRCD$ is greater than the maximum recommended value shown in this table, $^tRAC$ will increase by the amount that $^tRCD$ exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If at least one $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, all four $\overline{CAS}$ controls must be pulsed HIGH for $^tCP$.
17. Operation within the $^tRCD$ (MAX) limit ensures that $^tRAC$ (MAX) can be met. $^tRCD$ (MAX) is specified as a reference point only; if $^tRCD$ is greater than the specified $^tRCD$ (MAX) limit, then access time is controlled exclusively by $^tCAC$.
18. Operation within the $^tRAD$ (MAX) limit ensures that $^tRAC$ (MIN) and $^tCAC$ (MIN) can be met. $^tRAD$ (MAX) is specified as a reference point only; if $^tRAD$ is greater than the specified $^tRAD$ (MAX) limit, then access time is controlled exclusively by $^tAA$.
19. Either $^tRCH$ or $^tRRH$ must be satisfied for a READ cycle.
20. $^tOFF$ (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to $V_{OH}$ or $V_{OL}$. The 3ns minimum is a parameter guaranteed by design.
21. $^tWCS$, $^tRWD$, $^tAWD$ and $^tCWD$ are not restrictive operating parameters. $^tWCS$ applies to EARLY WRITE cycles. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE, and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. $^tWCS$, $^tRWD$, $^tAWD$ and $^tCWD$ are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$x leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, READ-WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. One to three $\overline{CAS}$ controls may be HIGH throughout any given $\overline{CAS}$ cycle, even though the timing waveforms show all $\overline{CAS}$ controls going LOW. If one goes LOW, it must meet all the timing requirements listed or the data for that I/O buffer may be invalid. At least one of the four $\overline{CAS}$ controls must be LOW for a valid $\overline{CAS}$ cycle to occur.
26. All other inputs at $V_{CC}$ -0.2V.
27. The first $\overline{CAS}$x edge to transition LOW.
28. The last $\overline{CAS}$x edge to transition HIGH.
29. Output parameters (DQx) are referenced to corresponding $\overline{CAS}$x input; DQ1 by $\overline{CAS1}$, DQ2 by $\overline{CAS2}$, etc.
30. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
31. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
32. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
33. First DQx controlled by the first $\overline{CAS}$x to go LOW.
34. Last DQx controlled by the last $\overline{CAS}$x to go HIGH.

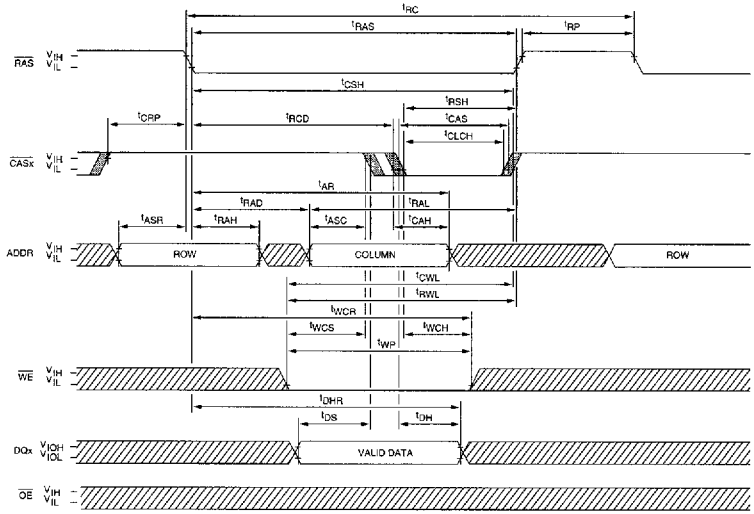
## NOTES (continued)

35. Each $\overline{CAS}$x must meet minimum pulse width.
36. Last $\overline{CAS}$x to go LOW.
37. LATE WRITE and READ-MODIFY-WRITE cycles must have both $^{t}$OD and $^{t}$OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{OE}$ is taken back LOW while $\overline{CAS}$ remains LOW, the DQs will remain open.
38. The DQs open during READ cycles once $^{t}$OD or $^{t}$OFF occur. If $\overline{CAS}$x goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$x stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. IF $\overline{OE}$ is brought back LOW ($\overline{CAS}$x still LOW), the DQs will provide the previously read data.
39. Column-address changed once each cycle.

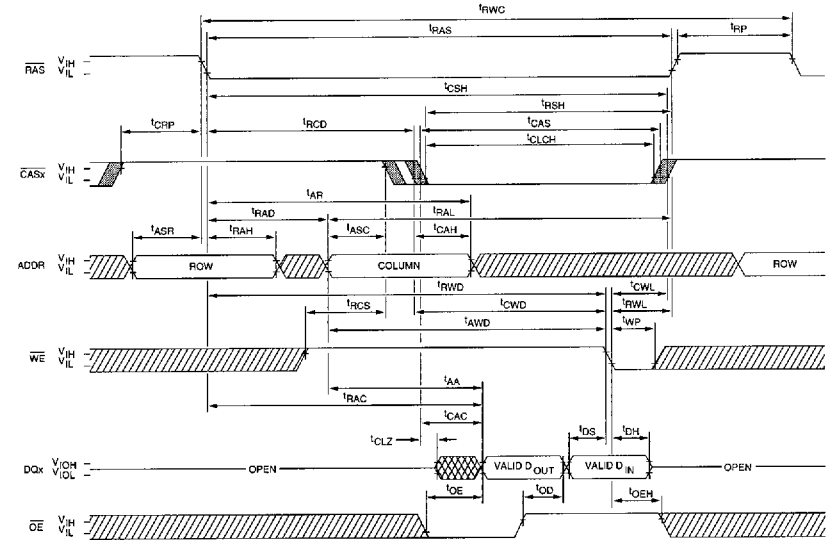
## READ CYCLE



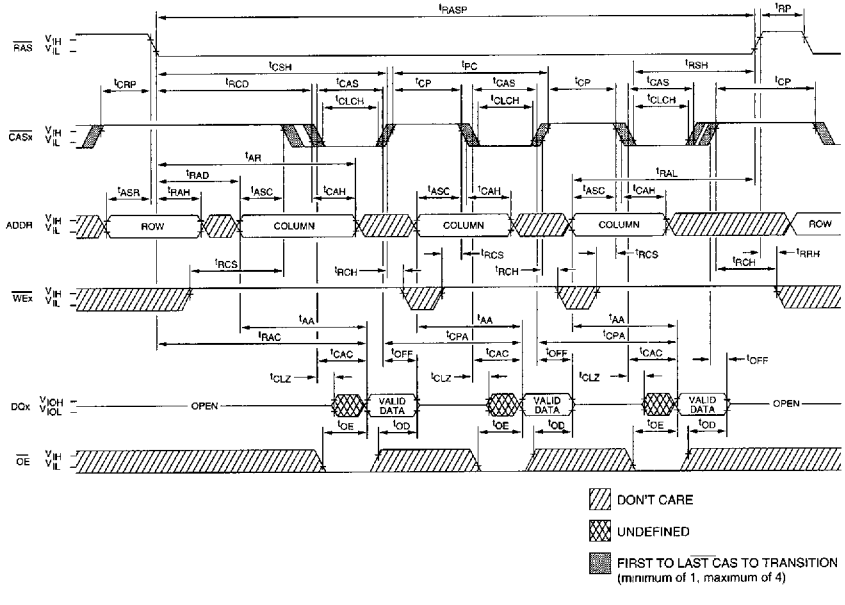

## EARLY WRITE CYCLE



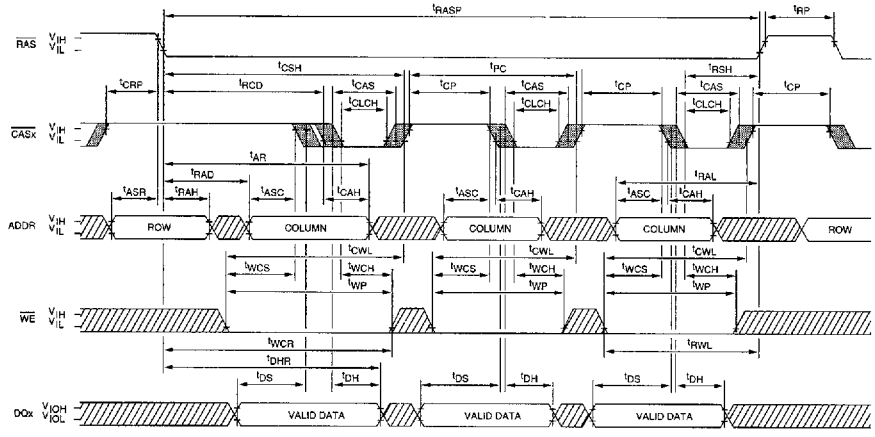
## READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE cycles)



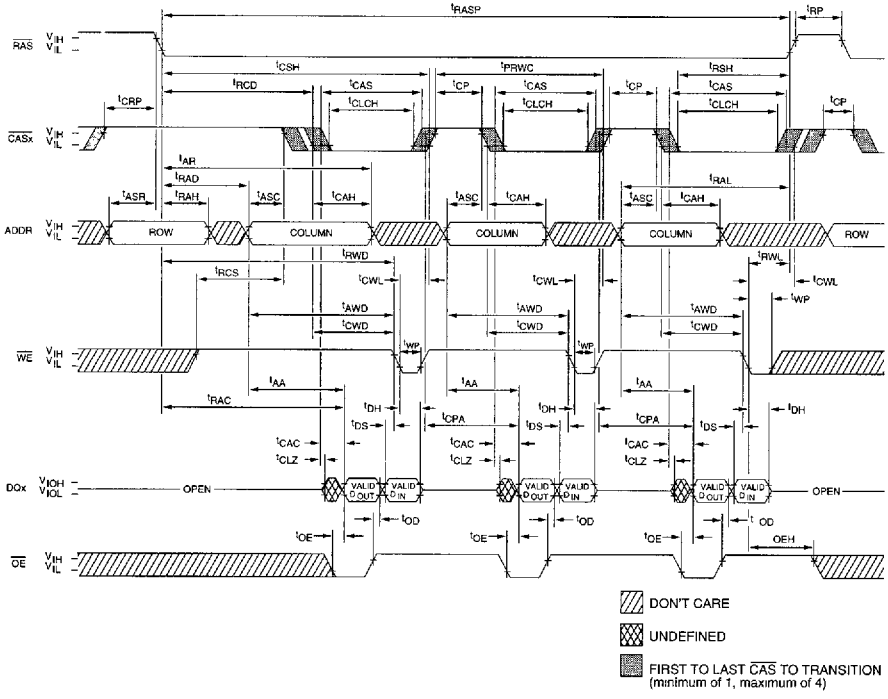

## FAST-PAGE-MODE READ CYCLE



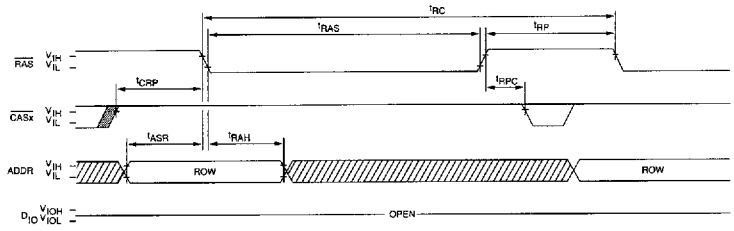
## FAST-PAGE-MODE EARLY-WRITE CYCLE



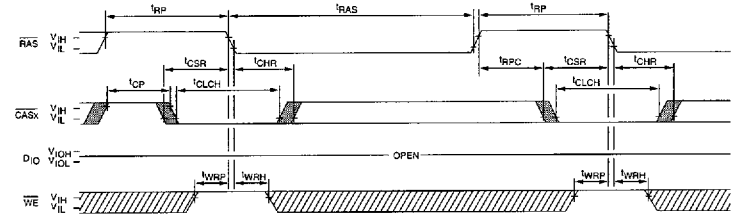

## FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE cycles)



## RAS-ONLY REFRESH CYCLE
(WE and OE = DON'T CARE)




## CBR REFRESH CYCLE [25]
(Addresses and OE = DON'T CARE)




## HIDDEN REFRESH CYCLE [24]
(WE = HIGH; OE = LOW)