REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Add LCC package. Convert to military drawing. Change load resistance in table I. Change code ident no. to 67268.	87-07-22	N. A. Hauck
D	Changes in accordance with NOR 5962-R180-92. --tvn	92-04-29	Monica L Poelking
E	Update to reflect latest changes in format and requirements. Editorial changes throughout. --les	04-01-29	Raymond Monnin
F	Update to reflect latest changes in format and requirements. Correction to marking paragraph 3.5. Editorial changes throughout. –les	05-03-22	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

REV											
SHEET											
REV											
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REV STATUS	REV	F	F	F	F	F	F	F	F	F	F
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10

PMIC N/A	PREPARED BY Joseph A. Kerbey	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY D. A. DiCenzo	
	APPROVED BY N. A. Hauck	MICROCIRCUIT, DIGITAL, LOW POWER SCHOTTKY TTL, AND GATE, BUS TRANSCEIVER WITH THREE-STATE OUTPUTS, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 81-05-19	
	REVISION LEVEL **F**	SIZE A · CAGE CODE **14933** · **80020**
		SHEET 1 OF 10

DSCC FORM 2233
APR 97

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

80020	01	C	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54LS242	Quadruple bus transceivers with three-state outputs inverted
02	54LS243	Quadruple bus transceivers with three-state outputs non-inverted

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	flat
2	CQCC1-N20	20	square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc at -18 mA to 5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	297 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases C and D	See MIL-STD-1835
Case 2	80% C/W
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.7 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input voltage	V_{IH}		1, 2, 3	All	2.0		V
Low level input voltage	V_{IL}		1, 2, 3	All		0.7	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA, T_C = +25°C	1	All		-1.5	V
High level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, V_{IL} = 0.7 V, I_{OH} = -3 mA	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, V_{IL} = 0.7 V, I_{OL} = 12 mA	1, 2, 3	All		0.4	V
Off-state output current, high level voltage applied	I_{OZH}	V_{CC} = 5.5 V, V_{IH} = 2.0 V, V_{IL} = 0.7 V, V_{OH} = 2.7 V	1, 2, 3	All		40	μA
Off-state output current, low level voltage applied	I_{OZL}	V_{CC} = 5.5 V, V_{IH} = 2.0 V, V_{IL} = 0.7 V, V_{OL} = 0.4 V	1, 2, 3	All		-200	μA
High level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 5.5 V	1, 2, 3	All		0.1	mA
High level input current, any input	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 2.7 V	1, 2, 3	All		20	μA
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	1, 2, 3	All		-200	μA
Output short circuit current 1/	I_{OS}	V_{CC} = 5.5 V	1, 2, 3	All	-40	-225	mA
Supply current	I_{CC}	V_{CC} = 5.5 V, Outputs high	1, 2, 3	All		38	mA
		Outputs low	1, 2, 3	01		50	mA
		Outputs low	1, 2, 3	02		54	mA
		All outputs disabled	1, 2, 3	01		50	mA
		All outputs disabled	1, 2, 3	02		54	mA
Functional tests		See 4.3.1c	7	All			
Propagation delay time	t_{PLH}	V_{CC} = 5.0 V, C_L = 45 pF ±10%, R_L = 110Ω ±5%	9, 10, 11	All		25	ns
	t_{PHL}		9, 10, 11	All		30	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Enable time	t_{PZL}	V_{CC} = 5.0 V, C_L = 45 pF ±10%, R_L = 110Ω ±5%	9, 10, 11	All		46	ns
	t_{PZH}		9, 10, 11	All		36	ns
Disable time	t_{PLZ}		9, 10, 11	All		39	ns
	t_{PHZ}		9, 10, 11	All		46	ns

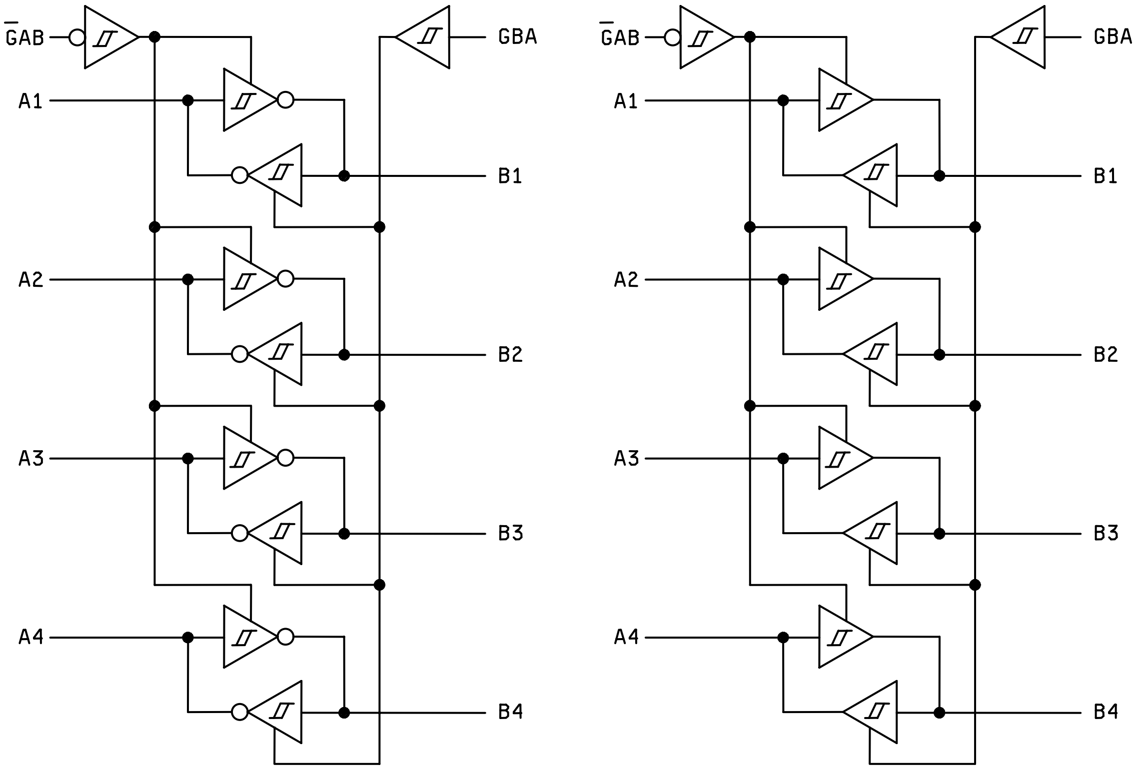
1/ Not more than one output should be shorted at a time, and the duration of the short circuit condition should not exceed one second.

Device types	01 and 02	
Case outlines	C, D	2
Terminal number	Terminal symbols	
1	$\overline{\text{G}}$ AB	NC
2	NC	$\overline{\text{G}}$ AB
3	A1	NC
4	A2	A1
5	A3	NC
6	A4	A2
7	GND	NC
8	B4	A3
9	B3	A4
10	B2	GND
11	B1	NC
12	NC	B4
13	GBA	B3
14	V_{CC}	B2
15	- - -	NC
16	- - -	B1
17	- - -	NC
18	- - -	NC
19	- - -	GBA
20	- - -	V_{CC}

FIGURE 1. Terminal connections.

INPUTS		DEVICE TYPE	
$\overline{\text{G}}$ AB	GBA	01	02
L	L	$\overline{\text{A}}$ to B	A to B
H	H	$\overline{\text{B}}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B (A = $\overline{\text{B}}$)	Latch A and B (A = B)

FIGURE 2. Truth table.


Device type 01

Device type 02

FIGURE 3. Logic diagram.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 9, 10**, 11**
Group C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-03-22

Approved sources of supply for SMD 80020 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Reference military specification PIN
8002001CA	3/ 3/ 3/	SNJ54LS242J SL54LS242/BCA 54LS242/BCAJC	M38510/32801BCA
8002001DA	3/ 3/ 3/	SNJ54LS242W SL54LS242/BDA 54LS242/BDAJC	M38510/32801BDA
80020012A	3/ 3/ 3/	SNJ54LS242FK SL54LS242/B2A 54LS242/B2AJC	M38510/32801B2A
80020012C	3/	SL54LS242/B2C	M38510/32801B2C
8002002CA	01295 3/ 3/	SNJ54LS243J SL54LS243/BCA 54LS243/BCAJC	M38510/32802BCA
8002002DA	01295 3/ 3/	SNJ54LS243W SL54LS243/BDA 54LS243/BDAJC	M38510/32802BDA
80020022A	3/ 3/ 3/	SNJ54LS243FK SL54LS243/B2A 54LS243/B2AJC	M38510/32802B2A
80020022C	3/	SL54LS243/B2C	M38510/32802B2C

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No current Source.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, Tx 75243 POC U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493