MOTOROLA

MCM6116

HCMOS
(COMPLEMENTARY MOS)

2,048 × 8 BIT
STATIC RANDOM
ACCESS MEMORY

16K BIT STATIC RANDOM ACCESS MEMORY

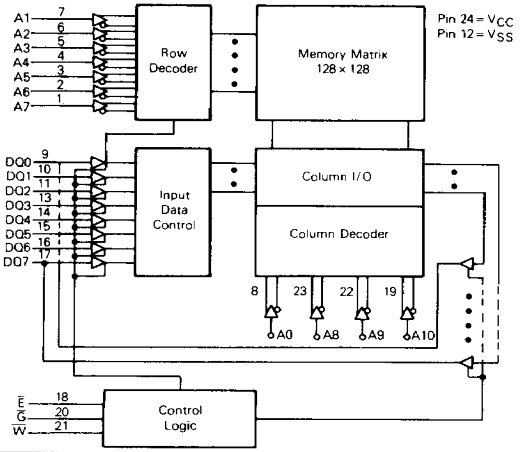
The MCM6116 is a 16,384-bit Static Random Access Memory organized as 2048 words by 8 bits, fabricated using Motorola's high-performance silicon-gate CMOS (HCMOS) technology. It uses a design approach which provides the simple timing features associated with fully static memories and the reduced power associated with CMOS memories. This means low standby power without the need for clocks, nor reduced data rates due to cycle times that exceed access time.

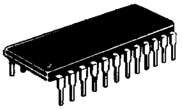
Chip Enable ($\overline{\text{E}}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after Chip Enable ($\overline{\text{E}}$) goes high, the part automatically reduces its power requirements and remains in this low-power standby as long as the Chip Enable ($\overline{\text{E}}$) remains high. The automatic power-down feature causes no performance degradation.

The MCM6116 is in a 24-pin dual-in-line package with the industry standard JEDEC approved pinout and is pinout compatible with the industry standard 16K EPROM/ROM.

- Single +5 V Supply
- 2048 Words by 8-Bit Operation
- HCMOS Technology
- Fully Static: No Clock or Timing Strobe Required
- Maximum Access Time: MCM6116-12 — 120 ns
  MCM6116-15 — 150 ns
  MCM6116-20 — 200 ns
- Power Dissipation: 70 mA Maximum (Active)
  15 mA Maximum (Standby-TTL Levels)
  2 mA Maximum (Standby)
- Low Power Version Also Available — MCM61L16
- Low Voltage Data Retention (MCM61L16 Only):
  50 μA Maximum

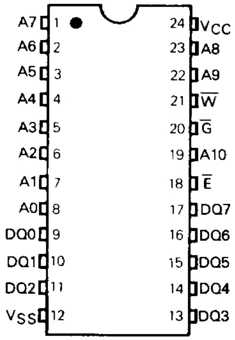
BLOCK DIAGRAM





P SUFFIX
PLASTIC PACKAGE
CASE 709

PIN ASSIGNMENTS



PIN NAMES	
A0-A10	Address Input
DQ0-DQ7	Data Input/Output
$\overline{\text{W}}$	Write Enable
$\overline{\text{G}}$	Output Enable
$\overline{\text{E}}$	Chip Enable
V_{CC}	Power (+5 V)
V_{SS}	Ground

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ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	−10 to +80	°C
Voltage on Any Pin With Respect to V_{SS}	−1.0 to +7.0	V
DC Output Current	20	mA
Power Dissipation	1.2	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature ranges unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−1.0*	–	0.8	V

*The device will withstand undershoots to the −1.0 volt level with a maximum pulse width of 50 ns at the −0.3 volt level. This is periodically sampled rather than 100% tested.

RECOMMENDED OPERATING CHARACTERISTICS

Parameter	Symbol	MCM6116			MCM61L16			Unit
		Min	Typ*	Max	Min	Typ*	Max	
Input Leakage Current ($V_{CC}=5.5$ V, V_{in} = GND to V_{CC})	$\lvert I_{LI} \rvert$	–	–	1	–	–	1	μA
Output Leakage Current ($\overline{E}=V_{IH}$ or $\overline{G}=V_{IH}$ $V_{I/O}$ = GND to V_{CC})	$\lvert I_{LO} \rvert$	–	–	1	–	–	1	μA
Operating Power Supply Current ($\overline{E}=V_{IL}$, $I_{I/O}=0$ mA)	I_{CC}	–	35	70	–	35	55	mA
Average Operating Current Minimum cycle, duty = 100%	I_{CC2}	–	35	70	–	35	55	mA
Standby Power Supply Current ($\overline{E}=V_{IH}$)	I_{SB}	–	5	15	–	5	12	mA
($\overline{E}\geq V_{CC}-0.2$ V, $V_{in}\geq V_{CC}-0.2$ V or $V_{in}\leq 0.2$ V)	I_{SB1}	–	20	2000	–	4	100	μA
Output Low Voltage ($I_{OL}=2.1$ mA)	V_{OL}	–	–	0.4	–	–	0.4	V
Output High Voltage ($I_{OH}=-1.0$ mA)**	V_{OH}	2.4	–	–	2.4	–	–	V

*$V_{CC}=5$ V, $T_A=25$°C

**Also, output voltages are compatible with Motorola's new high-speed CMOS logic family if the same power supply voltage is used.

CAPACITANCE (f = 1.0 MHz, $T_A=25$°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance except $\overline{E}$	C_{in}	3	5	pF
Input/Output Capacitance and $\overline{E}$ Input Capacitance	$C_{I/O}$	5	7	pF

MODE SELECTION

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	V_{CC} Current	DQ
Standby	H	X	X	I_{SB}, I_{SB1}	High Z
Read	L	L	H	I_{CC}	Q
Write Cycle (1)	L	H	L	I_{CC}	D
Write Cycle (2)	L	L	L	I_{CC}	D

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

Input Pulse Levels .... 0 Volt to 3.5 Volts
Input Rise and Fall Times .... 10 ns
Input and Output Timing Reference Levels .... 1.5 Volts
Output Load .... 1 TTL Gate and $C_L = 100$ pF

READ CYCLE

Parameter	Symbol	MCM6116-12 MCM61L16-12		MCM6116-15 MCM61L16-15		MCM6116-20 MCM61L16-20		Unit
		Min	Max	Min	Max	Min	Max	
Address Valid to Address Don't Care (Cycle Time when Chip Enable is Held Active)	t_{AVAX}	120	–	150	–	200	–	ns
Chip Enable Low to Chip Enable High	t_{ELEH}	120	–	150	–	200	–	ns
Address Valid to Output Valid (Access)	t_{AVQV}	–	120	–	150	–	200	ns
Chip Enable Low to Output Valid (Access)	t_{ELQV}	–	120	–	150	–	200	ns
Address Valid to Output Invalid	t_{AVQX}	10	–	15	–	15	–	ns
Chip Enable Low to Output Invalid	t_{ELQX}	10	–	15	–	15	–	ns
Chip Enable High to Output High Z	t_{EHQZ}	0	40	0	50	0	60	ns
Output Enable to Output Valid	t_{GLQV}	–	80	–	100	–	120	ns
Output Enable to Output Invalid	t_{GLQX}	10	–	15	–	15	–	ns
Output Enable to Output High Z	t_{GLQZ}	0	40	0	50	0	60	ns
Address Invalid to Output Invalid	t_{AXQX}	10	–	15	–	15	–	ns
Address Valid to Chip Enable Low (Address Setup)	t_{AVEL}	0	–	0	–	0	–	ns
Chip Enable to Power-Up Time	t_{PU}	0	–	0	–	0	–	ns
Chip Disable to Power-Down Time	t_{PD}	–	30	–	30	–	30	ns

WRITE CYCLE

Parameter	Symbol	MCM6116-12 MCM61L16-12		MCM6116-15 MCM61L16-15		MCM6116-20 MCM61L16-20		Unit
		Min	Max	Min	Max	Min	Max	
Chip Enable Low to Write High	t_{ELWH}	70	–	90	–	120	–	ns
Address Valid to Write High	t_{AVWH}	105	–	120	–	140	–	ns
Address Valid to Write Low (Address Setup)	t_{AVWL}	20	–	20	–	20	–	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	70	–	90	–	120	–	ns
Write High to Address Don't Care	t_{WHAX}	5	–	10	–	10	–	ns
Data Valid to Write High	t_{DVWH}	35	–	40	–	60	–	ns
Write High to Data Don't Care (Data Hold)	t_{WHDX}	5	–	10	–	10	–	ns
Write Low to Output High Z	t_{WLQZ}	0	50	0	60	0	60	ns
Write High to Output Valid	t_{WHQV}	5	–	10	–	10	–	ns
Output Disable to Output High Z	t_{GHQZ}	0	40	0	50	0	60	ns

TIMING PARAMETER ABBREVIATIONS

t X X X X
signal name from which interval is defined
transition direction for first signal
signal name to which interval is defined
transition direction for second signal

The transition definitions used in this data sheet are:
H = transition to high
L = transition to low
V = transition to valid
X = transition to invalid or don't care
Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

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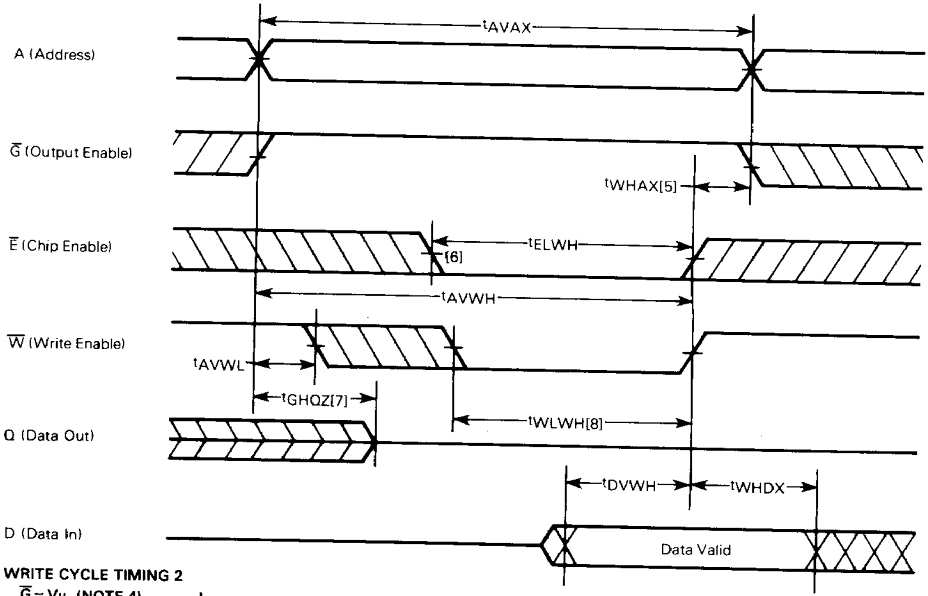
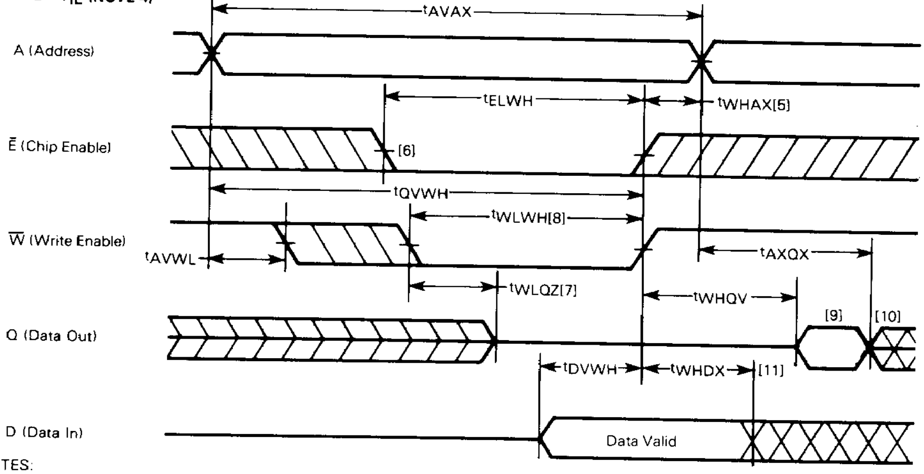
WRITE CYCLE TIMING 1 (NOTE 4)



WRITE CYCLE TIMING 2
$\overline{G}=V_{IL}$ (NOTE 4)



NOTES:

4. Write Enable ($\overline{W}$) must be high during all address transitions.
5. t_{WHAX} is measured from the earlier of Chip Enable ($\overline{E}$) or Write Enable ($\overline{W}$) going high to the end of write cycle.
6. If the Chip Enable ($\overline{E}$) low transition occurs simultaneously with the Write Enable ($\overline{W}$) low transitions or after the Write Enable ($\overline{W}$) transition, the output remains in a high impedance state.
7. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
8. A write occurs during the overlap of a low Chip Enable ($\overline{E}$) and a low Write Enable ($\overline{W}$).
9. Q (Data Out) is the same phase as write data of this write cycle.
10. Q (Data Out) is the read of the next address.
11. If Chip Enable ($\overline{E}$) is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

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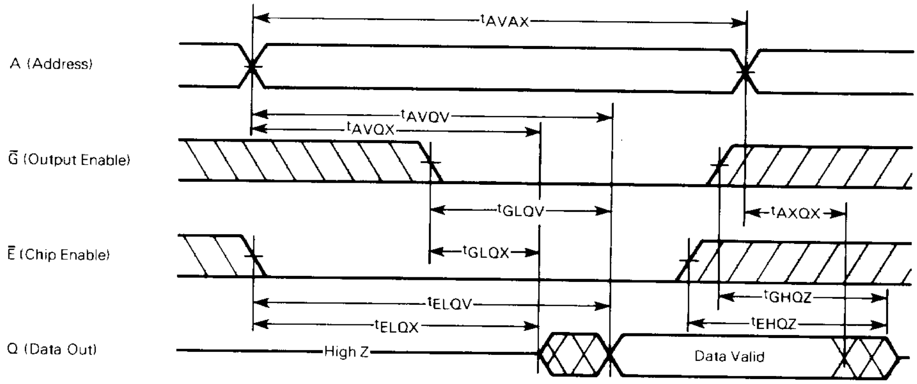
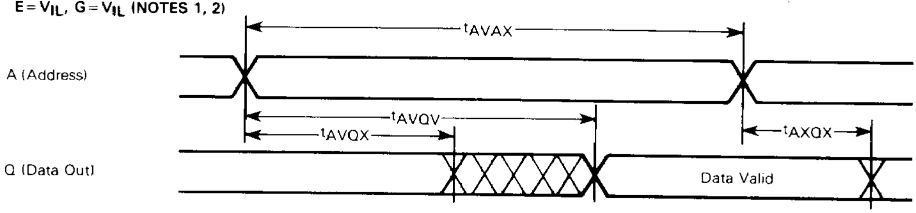
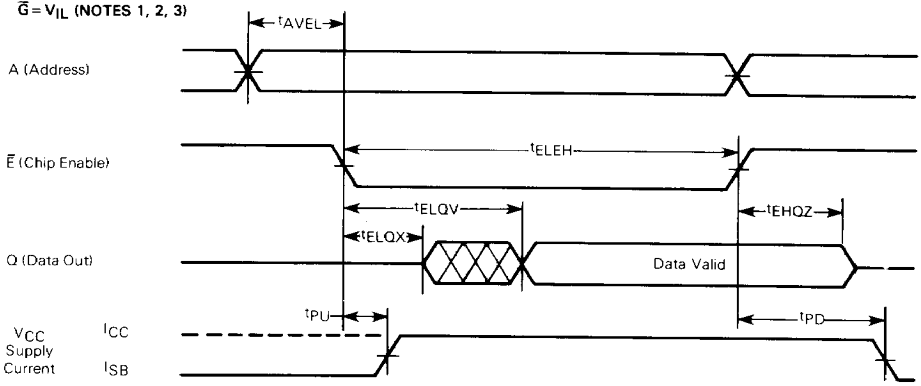
READ CYCLE TIMING 1 (NOTES 1 AND 2)



READ CYCLE TIMING 2
$\overline{E}=V_{IL}$, $\overline{G}=V_{IL}$ (NOTES 1, 2)



READ CYCLE TIMING 3
$\overline{G}=V_{IL}$ (NOTES 1, 2, 3)



NOTES:
1. Write Enable ($\overline{W}$) is High for Read Cycle.
2. When Chip Enable ($\overline{E}$) is Low, the address input must not be in the high impedance state.
3. Address Valid prior to or coincident with Chip Enable ($\overline{E}$) transition Low.

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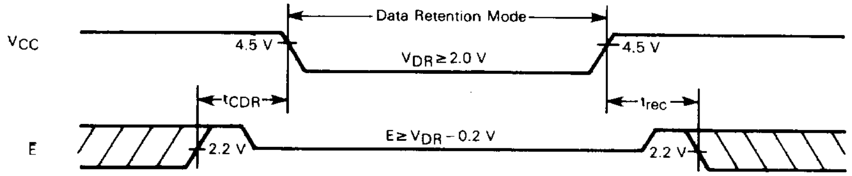
LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_A = 0$ to $+70°C$) (MCM61L16 Only)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention	$\overline{E} \geq V_{CC} - 0.2$ V $V_{in} \geq V_{CC} - 0.2$ V or $V_{in} \leq 0.2$ V	V_{DR}	2.0	–	–	V
Data Retention Current	$V_{CC} = 3.0$ V, $\overline{E} \geq 2.8$ V $V_{in} \geq 2.8$ V or $V_{in} \leq 0.2$ V	I_{CCDR}	–	–	50	µA
Chip Disable to Data Retention Time	See Retention Waveform	t_{CDR}	0	–	–	ns
Operation Recovery Time		t_{rec}	$^*t_{AVAX}$	–	–	ns

$^*t_{AVAX}$ = Read Cycle Time.

LOW V_{CC} DATA RETENTION WAVEFORM



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