MOTOROLA

MC75450

DUAL PERIPHERAL POSITIVE "AND" DRIVER

The MC75450 is a versatile device designed for use as a general-purpose dual interface circuit in MDTL and MTTL type systems. This device features two standard MTTL gates and two noncommitted, high-current, high-voltage NPN transistors. Typical applications include relay and lamp drivers, power drivers, MOS and memory drivers.

- MDTL and MTTL Compatibility
- 300 mA Output Current Drive Capability (each transistor)
- Separate Gate and Output Transistor for Maximum Design Flexibility
- High Output Breakdown Voltage: V_{CER} = 30 Volts minimum

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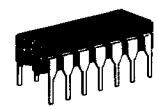
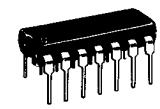
DUAL PERIPHERAL POSITIVE "AND" DRIVER

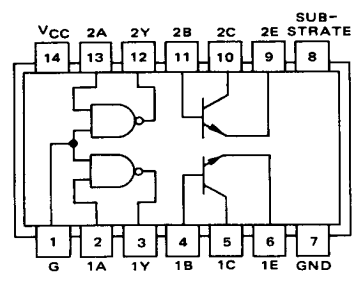
SILICON MONOLITHIC INTEGRATED CIRCUITS



L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)



P SUFFIX
PLASTIC PACKAGE
CASE 646



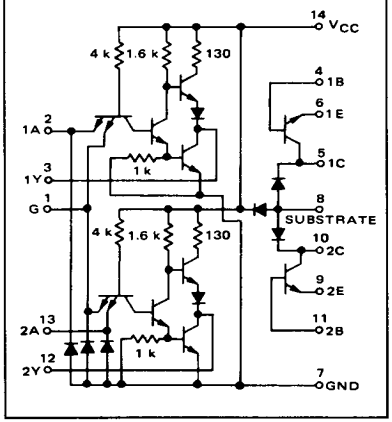
Positive Logic: $Y = \overline{AG}$ (gate only)
$C = AG$ (gate and transistor)

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage (See Note 1)	V_{CC}	+7.0	Vdc
Input Voltage (See Note 1)	V_{in}	5.5	Vdc
V_{CC}-to-Substrate Voltage		35	Vdc
Collector-to-Substrate Voltage		35	Vdc
Collector-Base Voltage	V_{CB}	35	Vdc
Collector-Emitter Voltage (See Note 2)	V_{CE}	30	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current (continuous) (See Note 3)		300	mA
Power Dissipation (Package Limitation) Plastic and Ceramic Dual In-Line Packages Derate above T_A = +25°C	P_D	 830 6.6	 mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 ohms.
3. Both halves of these dual circuits may conduct the rated current simultaneously.

CIRCUIT SCHEMATIC



RECOMMENDED OPERATING CONDITIONS (See Note 4)

Characteristic	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc

Note 4. The substrate, pin 8, must always be at the most negative device voltage for proper operation.

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic		Symbol	Test Fig.	Min	Typ*	Max	Unit
MTTL GATES							
High-Level Input Voltage		V_{IH}	1	2.0	–	–	Vdc
Low-Level Input Voltage		V_{IL}	2	–	–	0.8	Vdc
High-Level Output Voltage (V_{CC} = 4.5 V, V_{IL} = 0.8 V, I_{OH} = –400 μA)		V_{OH}	2	2.4	3.3	–	Vdc
Low-Level Output Voltage (V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OL} = 16 mA)		V_{OL}	1	–	0.22	0.4	Vdc
High-Level Input Current		I_{IH}	3				
(V_{CC} = 5.25 V, V_{in} = 2.4 V)	Input A			–	–	40	μA
	Input G			–	–	80	
(V_{CC} = 5.25 V, V_{in} = 5.5 V)	Input A			–	–	1.0	mA
	Input G			–	–	2.0	
Low-Level Input Current		I_{IL}	4				mA
(V_{CC} = 5.25 V, V_{in} = 0.4 V)	Input A			–	–	-1.6	
	Input G			–	–	-3.2	
Short-Circuit Output Current** (V_{CC} = 5.25 V)		I_{OS}	5	-18	–	-55	mA
Supply Current			6				mA
High-Level Output (V_{CC} = 5.25 V, V_{in} = 0)		I_{CCH}		–	2.0	4.0	
Low-Level Output (V_{CC} = 5.25 V, V_{in} = 5.0 V)		I_{CCL}		–	6.0	11	
Input Clamp Voltage (V_{CC} = 4.75 V, I_{in} = –12 mA)		V_{in}	4	–	–	-1.5	V

OUTPUT TRANSISTORS

Characteristic	Symbol	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage (I_C = 100 μA, I_E = 0)	V_{CBO}	35	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 100 μA, R_{BE} = 500 ohms)	V_{CER}	30	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μA, I_C = 0)	V_{EBO}	5.0	–	–	Vdc
Static Forward Transfer Ratio (See Note 5)	h_{FE}				
(V_{CE} = 3.0 V, I_C = 100 mA, T_A = +25°C)		25	–	–	
(V_{CE} = 3.0 V, I_C = 300 mA, T_A = +25°C)		30	–	–	
(V_{CE} = 3.0 V, I_C = 100 mA, T_A = 0°C)		20	–	–	
(V_{CE} = 3.0 V, I_C = 300 mA, T_A = 0°C)		25	–	–	
Base-Emitter Voltage (See Note 5)	V_{BE}				Vdc
(I_B = 10 mA, I_C = 100 mA)		–	0.85	1.0	
(I_B = 30 mA, I_C = 300 mA)		–	1.05	1.2	
Collector-Emitter Saturation Voltage (See Note 5)	$V_{CE(sat)}$				Vdc
(I_B = 10 mA, I_C = 100 mA)		–	0.25	0.4	
(I_B = 30 mA, I_C = 300 mA)		–	0.5	0.7	

Note 5. These parameters must be measured using pulse techniques; t_w = 300 μs, duty cycle ≤ 2%.
*All typical values at V_{CC} = 5.0 V, T_A = +25°C.
**Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
MTTL GATES						
Propagation Delay Time (C_L = 15 pF, R_L = 400 ohms)		7				ns
Low-to-High-Level Output	t_{PLH}		–	14	–	
High-to-Low-Level Output	t_{PHL}		–	6.0	–	
OUTPUT TRANSISTORS #						
Switching Times (I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = –40 mA, $V_{BE(off)}$ = –1.0 V, C_L = 15 pF, R_L = 50 ohms)		8				ns
Delay Time	t_d		–	9.0	–	
Rise Time	t_r		–	11	–	
Storage Time	t_s		–	14	–	
Fall Time	t_f		–	8.0	–	
GATES AND TRANSISTORS COMBINED #						
Propagation Delay Time (I_C = 200 mA, C_L = 15 pF, R_L = 50 ohms)		9				ns
Low-to-High-Level Output	t_{PLH}		–	21	–	
High-to-Low Level Output	t_{PHL}		–	16	–	
Transition Time # (I_C = 200 mA, C_L = 15 pF, R_L = 50 ohms)		9				ns
Low-to-High-Level Output	t_{TLH}		–	7.0	–	
High-to-Low-Level Output	t_{THL}		–	8.0	–	

#Voltage and current values are nominal; exact values vary slightly with transistors parameters.

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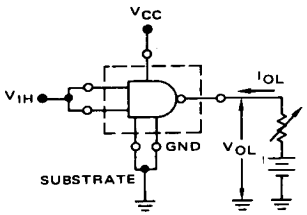
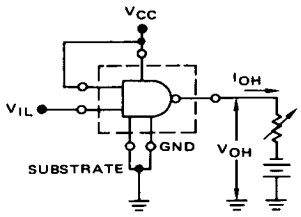
DC TEST CIRCUITS FOR MTTL GATES

FIGURE 1 – V_{IH}, V_{OL}



Both inputs are tested simultaneously.

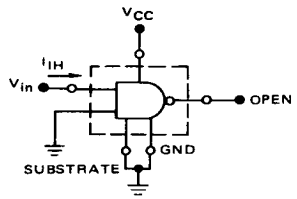
FIGURE 2 – V_{IL}, V_{OH}



Each input is tested separately.

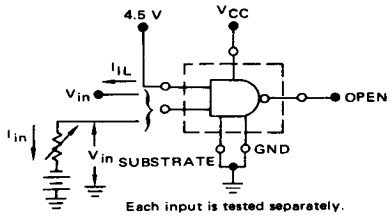
(Arrows indicate actual direction of current flow. Current into a terminal is a positive value.)

FIGURE 3 – I_{IH}



Each input is tested separately.

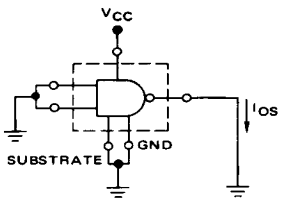
FIGURE 4 – I_{IL}, V_{in}



Each input is tested separately.

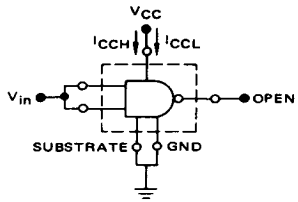
DC TEST CIRCUITS FOR MTTL GATES (continued)

FIGURE 5 – I_{OS}



Each gate is tested separately

FIGURE 6 – I_{CCH}, I_{CCL}



Both gates are tested simultaneously.

(Arrows indicate actual direction of current flow. Current into a terminal is a positive value.)

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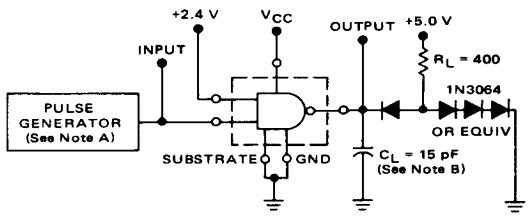
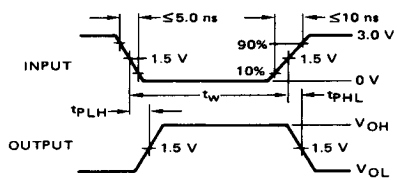
FIGURE 7 – PROPAGATION DELAY TIMES, EACH GATE



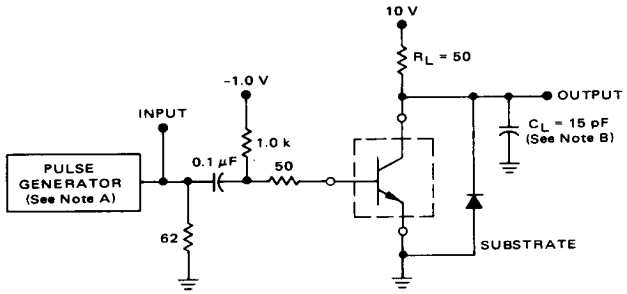
NOTES: A. The pulse generator has the following characteristics: $t_w = 0.5\ \mu s$, PRR = 1.0 MHz, $z_o \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS



TEST CIRCUITS (continued)

FIGURE 8 – SWITCHING TIMES, EACH TRANSISTOR



NOTES: A. The pulse generator has the following characteristics: t_w = 0.3 μs, duty cycle ≤ 1%, $z_o \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

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VOLTAGE WAVEFORMS

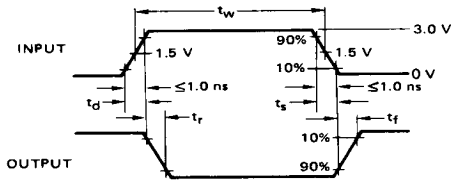
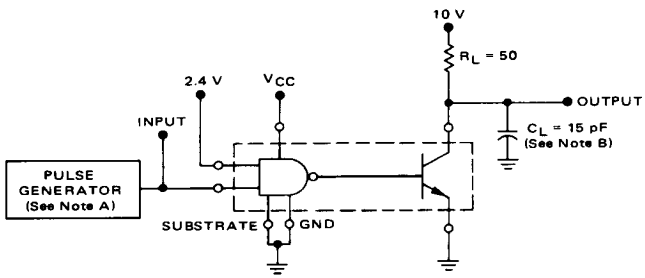


FIGURE 9 – SWITCHING TIMES, GATE AND TRANSISTOR



NOTES: A. The pulse generator has the following characteristics: t_w = 0.5 μs, PRR = 1.0 MHz, $z_o \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS