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MC68302

Integrated Multiprotocol Processor (IMP)

The IMP is a very large-scale integration (VLSI) device incorporating the main building blocks needed for the design of a wide variety of controllers. The device is especially suitable to applications in the communications industry. The IMP is the first device to offer the benefits of a closely coupled, industry-standard, MC68000/MC68008 microprocessor core and a flexible communications architecture. This multichannel communications device may be configured to support a number of popular industry interfaces, including those for the Integrated Services Digital Network (ISDN) basic rate and terminal adaptor applications. Through a combination of architectural and programmable features, concurrent operation of different protocols is easily achieved using the IMP. Data concentrators, line cards, bridges, and gateways are examples of suitable applications for this versatile device.

The IMP is a high-density complementary metal-oxide semiconductor (HCMOS) device consisting of an MC68000/MC68008 microprocessor core, a system integration block (SIB), and a communications processor (CP). The MC68302 block diagram is shown in Figure 1.

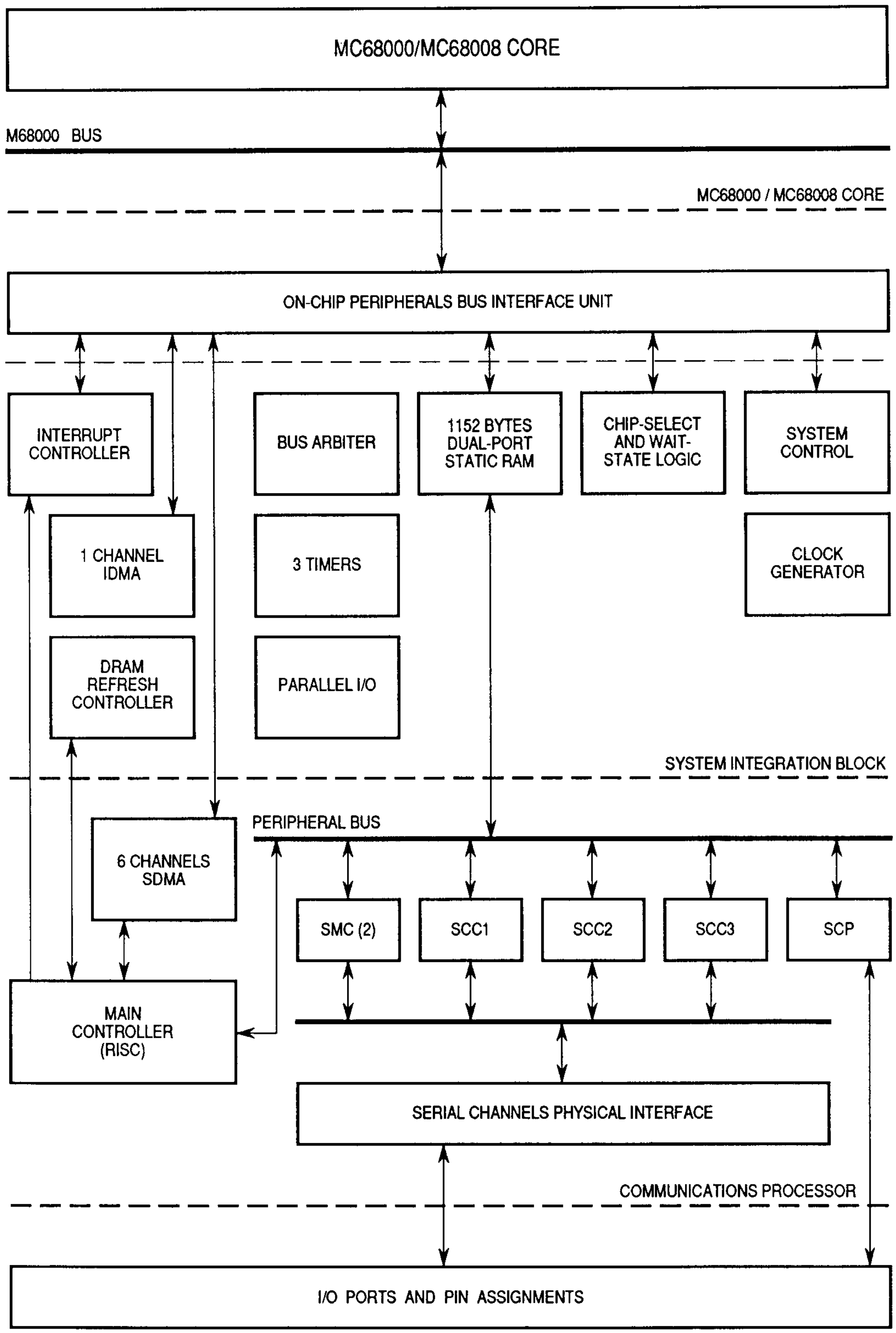


Figure 1. MC68302 Block Diagram

The features of the IMP are as follows:

- MC68000/MC68008 Microprocessor Core Supporting a 16- or 8-Bit M68000 Family
- SIB including:
  - Independent Direct Memory Access (IDMA) Controller
  - Interrupt Controller with Two Modes of Operation
  - Parallel Input/Output (I/O) Ports, Some with Interrupt Capability
  - On-Chip 1152 Bytes of Dual-Port Random-Access Memory (RAM)
  - Three Timers, Including a Watchdog Timer
  - Four Programmable Chip-Select Lines with Wait-State Logic
  - Programmable Address Mapping of Dual-Port RAM and IMP Registers
  - On-Chip Clock Generator with an Output Clock Signal
  - System Control
    - System Control Register
    - Bus Arbitration Logic with Low Interrupt Latency Support
    - Hardware Watchdog for Monitoring Bus Activity
    - Low Power (Standby) Modes
    - Disable CPU Logic (M68000)
    - Freeze Control for Debugging Selected On-Chip Peripherals
    - DRAM Refresh Controller
- CP including:
  - Main Controller (RISC Processor)
  - Three Full-Duplex Serial Communication Controllers (SCCs)
  - Six Serial Direct Memory Access (SDMA) Channels Dedicated to the Three SCCs
  - Flexible Physical Interface Accessible by SCCs for Interchip Digital Link (IDL), General Circuit Interface (GCI, see note), Pulse Code Modulation (PCM), and Nonmultiplexed Serial Interface (NMSI) Operation
  - Serial Communication Port (SCP) for Synchronous Communication
  - Serial Management Controllers (SMCs) for IDL and GCI Channels

NOTE

GCI is sometimes referred to as IOM2.

GENERAL DESCRIPTION

The MC68302 uses a microprocessor architecture which has peripheral devices connected to the system bus through a dual-port memory. Various parameters, counters, and all memory buffer descriptor tables reside in the dual-port RAM. The receive and transmit data buffers may be located in this on-chip RAM or in the off-chip system RAM (see Figure 2). Six DMA channels are dedicated to the six serial ports (receive and transmit for each of the three SCC channels). If an SCC channel's data is programmed to be located in the external RAM, the CP main controller (RISC processor) will program the corresponding DMA channel to perform the required accesses. If the data resides in the on-chip dual-port RAM, then the CP main controller accesses the RAM with one clock cycle access and no arbitration delays.

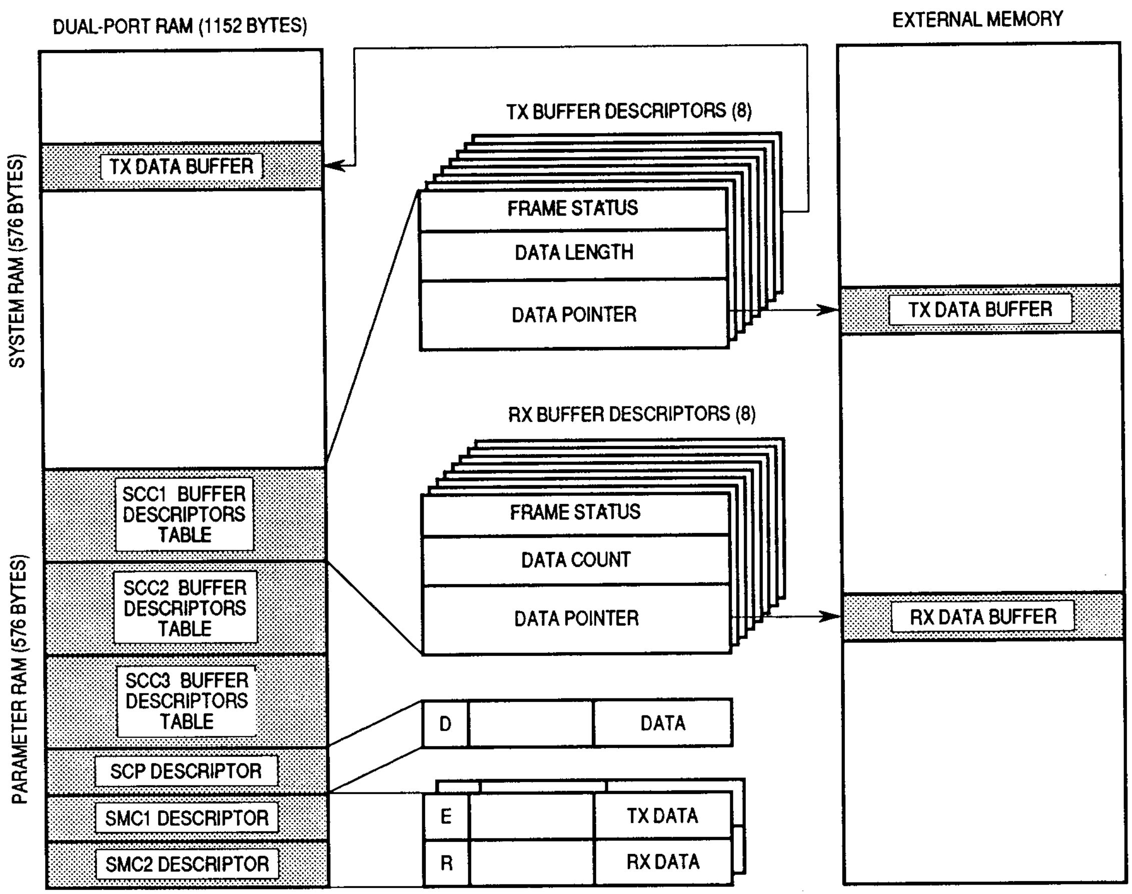


Figure 2. MC68302 Buffer Memory Structure

The buffer memory structure of the MC68302 can be configured by software to closely match I/O channel requirements. The interrupt structure is also programmable to relieve the on-chip MC68000/MC68008 core from bit manipulation functions for peripherals, allowing the processor to perform application software or protocol processing.

In some cases, the interface to equipment or proprietary networks may require the use of standard control and data signals. For these signals, the MC68302 can be programmed to use the NMSI mode. This mode is available for one, two, or all three SCC ports; remaining ports may then use one of the multiplexed interface modes: IDL, GCI, or PCM.

MC68000/MC68008 CORE OVERVIEW

The MC68302 allows operation either in the full MC68000 mode with a 16-bit data bus or in the MC68008 mode with an 8-bit data bus.

Refer to FR68K/D, *M68000 Family Reference*, and to M68000UM/AD, *M68000 8-/16-/32-Bit Microprocessors User's Manual Sixth Edition*, for information on the MC68000 and MC68008 microprocessors.

SYSTEM INTEGRATION BLOCK (SIB)

The MC68302 has an SIB which simplifies the task of hardware and software design. The IDMA controller eliminates the need for an external DMA controller on the system board. In addition, there is an interrupt controller that can be used in a dedicated mode to generate interrupt acknowledge signals without external logic. Similarly, the chip-select signals and wait-state logic eliminate the need to generate these signals externally.

The SIB includes the IDMA controller, interrupt controller, parallel I/O ports, dual-port RAM, three timers, chip-select logic, clock generator, and system control.

IDMA Controller

The MC68302 has one IDMA channel and six serial DMA channels which operate concurrently with other CPU operations. The IDMA can operate in different modes of data transfer as programmed by the user. The six serial DMA channels for the three full-duplex SCC channels are transparent to the user, implementing bus-cycle-stealing data transfers controlled by the MC68302's internal RISC controller. These six channels have priority over the separate IDMA channel.

The IDMA controller can transfer data between any combination of memory and I/O devices. In addition, data may be transferred in either byte or word quantities, and the source and destination addresses may be either odd or even. Every IDMA cycle requires between two and four bus cycles, depending on the address boundary and transfer size. If both the source and destination addresses are even, the IDMA fetches one word of data and then immediately deposits it. If either the source or destination block begins on an odd boundary, the transfer takes more bus cycles.

The IDMA features are as follows:

- Memory-Memory, Memory-Peripheral, or Peripheral-Memory Data Transfers
- Operation with Data Blocks Located at Even or Odd Addresses
- Packing and Unpacking of Operands
- Fast Transfer Rates: Up to 4 MBps at 16 MHz with No Wait States
- Full Support of All Bus Exceptions: Halt, Bus Error, and Retry
- Flexible Request Generation
- Two Address Pointer Registers and One Counter Register
- Three I/O Lines for Externally Requested Data Transfers
- Asynchronous Bus Structure with 24-Bit Address and 8-/16-Bit Data Bus

Interrupt Controller

The interrupt controller, which manages the priority of internal and external interrupt requests, generates a vector number during the CPU interrupt acknowledge cycle. Nested interrupts are fully supported.

The interrupt controller receives requests from internal sources (INRQ interrupts) such as the timers, the IDMA, the serial controllers, and the parallel I/O pins (port B). The interrupt controller allows the masking of each INRQ interrupt source. When multiple events within a peripheral can cause the interrupt, each of these events is also maskable.

The interrupt controller also receives external (EXRQ) requests. EXRQ interrupts are received by the IMP according to the operational mode selected. In the normal operational mode, EXRQ interrupts are encoded onto the $\overline{IPL}$ lines. In the dedicated operational mode, EXRQ interrupts are presented directly as $\overline{IRQ7}$, $\overline{IRQ6}$, and $\overline{IRQ1}$.

The interrupt controller block diagram is shown in Figure 3. The interrupt controller features are as follows:

- Two Operational Modes: Normal and Dedicated
- Eighteen Priority-Organized Interrupt Sources (Internal and External)
- Fully Nested Interrupt Environment
- Unique Vector Number for Each Internal/External Source
- Three Selectable Interrupt Request/Interrupt Acknowledge Pairs

Parallel I/O Ports

Port A and port B are two general-purpose I/O ports. Each pin in the 16-bit port A may be configured as a general-purpose I/O pin or as a dedicated peripheral interface pin. Port B has 12 pins. Eight pins may be configured as general-purpose pins or as dedicated peripheral interface pins, and four are general-purpose pins, each with interrupt capability.

Dual-Port RAM

The IMP has 1152 bytes of RAM configured as a dual-port memory. The RAM can be accessed by the internal RISC controller or one of three bus masters: the M68000 core, an external bus master, or the IDMA. All internal bus masters synchronously access the RAM with no wait states. External bus masters can access the RAM and registers synchronously or asynchronously.

The RAM is divided into two parts. There are 576 bytes used as a parameter RAM, which includes pointers, counters, and registers for the serial ports. The other 576 bytes may be used for system RAM, which may include data buffers, or may be used for other purposes such as a no-wait-state cache.

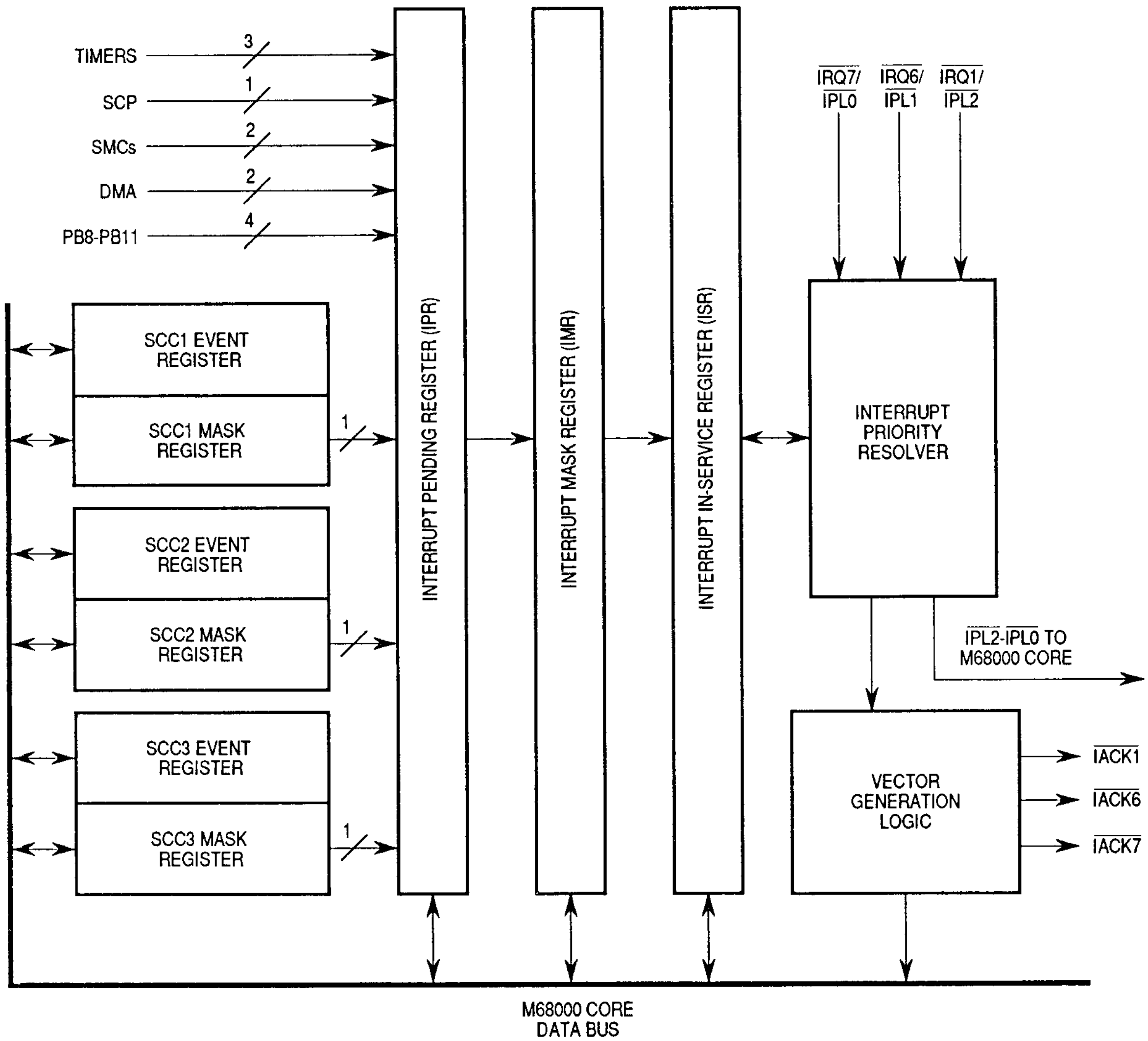


Figure 3. Interrupt Controller Block Diagram

TIMERS

There are three timer units. Two units are identical, general-purpose timers; the third unit can be used to implement a watchdog timer function.

The two general-purpose timers are implemented with a timer mode register (TMR), a timer capture register (TCR), a timer counter (TCN), a timer reference register (TRR), and a timer event register (TER). The TMR contains the prescaler value programmed by the user. The watchdog timer, which has a TRR and TCN, uses a fixed prescaler value.

The timer features are as follows:

- Two General-Purpose Timer Units:
  - Maximum Period of 16 Seconds (at 16.67 MHz)
  - 60-Nanosecond Resolution (at 16.67 MHz)
  - Programmable Sources for the Clock Input
  - Input Capture Capability
  - Output Compare with Programmable Mode for the Output Pin
  - Free Run and Restart Modes
- One Watchdog Timer with a 16-Bit Counter and a Reference Register
  - Maximum Period of 16 Seconds (at 16.67 MHz)
  - 0.5-Millisecond Resolution (at 16 MHz)
  - Output Signal ($\overline{\text{WDOG}}$)
  - Interrupt Capability

EXTERNAL CHIP-SELECT SIGNALS AND WAIT-STATE LOGIC

The MC68302 has a set of four programmable chip-select signals. Each chip select has an identical structure. For each memory area, an internally generated cycle-termination signal ($\overline{\text{DTACK}}$) may be defined with up to six wait states to avoid using board space for cycle-termination logic. The four signals may each support four different classes of memory, such as high-speed static RAM, slower dynamic RAM, EPROM, and nonvolatile RAM. The chip-select and wait-state generation logic is active for all potential bus masters.

CLOCK GENERATOR

The MC68302 has an on-chip clock generator which supplies internal and external high-speed clocks (up to 16.67 MHz). The clock circuitry uses three dedicated pins: EXTAL, XTAL, and CLKO.

SYSTEM CONTROL

The IMP system control consists of a system control register (SCR) containing bits for the following system control functions:

- System Status and Control Logic
- Bus Arbitration Logic with Low Interrupt Latency
- Hardware Watchdog
- Low Power (Standby) Modes
- Disable CPU Logic (M68000)
- Freeze Control for Debugging On-Chip Peripherals
- $\overline{\text{AS}}$ Control during Read-Modify-Write Cycles

System Control Register

The SCR is a 32-bit register that consists of system status and control bits, a bus arbiter control bit, hardware watchdog control bits, low power control bits, and freeze select bits. The eight most significant bits of the SCR report events recognized by the system control logic and set the corresponding bit in the SCR.

The low power modes are used, when no processing is required from the MC68000/MC68008 core, to reduce the system power consumption to its minimum value. The low power modes may be exited by an interrupt from an on-chip peripheral.

Disable CPU Logic (M68000)

This control allows an external processor direct connection to the bus and to the IMP's peripherals while the on-chip M68000 core is disabled. Entered during a system reset (RESET and HALT asserted together), this mode configures the IMP on-chip peripherals for use with other MC68302 units or other processors and is an effective configuration for systems needing more than three SCCs.

Freeze Control

This control is used to freeze the activity of selected peripherals and to debug systems. The IMP freezes its activity with no new interrupt requests, no memory accesses (internal or external), and no access of the serial channels.

The IDMA controller completes any bus cycle in progress and releases bus ownership. No further bus cycles will be started as long as $\overline{FRZ}$ remains asserted.

DRAM REFRESH CONTROLLER

The CP main (RISC) controller can optionally handle the dynamic RAM (DRAM) refresh task without any intervention from the M68000 core. The refresh request can be generated from an MC68302 timer, baud rate generator, or externally. The DRAM refresh controller performs a standard M68000-type read cycle at programmable address sequences, with user-provided RAS and CAS generation.

COMMUNICATIONS PROCESSOR

The CP in the MC68302 includes the main controller, six serial DMA channels, three SCCs, an SCP, and two SMCs.

Host software configures each communications channel, as required by the application, to include parameters, baud rates, physical channel interfaces desired, and interrupting conditions. Buffer structures are set up for receive and transmit channels. Up to eight frames may be received or transmitted without host software involvement. Selection of the interrupt interface is also set by register bits in the register space of the device.

Data is transmitted and received using the appropriate buffer descriptors and buffer data space for a given channel. The CP operates in a modified polling mode on each channel and buffer descriptor to identify buffers awaiting transmission and channels requiring servicing. The user sets a bit in the buffer descriptor of a transmit frame; when the CP polls and detects this bit, it will begin transmission. Generally, no other action is required to accomplish transmission.

Main Controller

The main controller is a microcoded RISC processor that services all the serial channels. The main controller transfers data between the serial channels and internal/external RAM, executes host commands, and generates interrupts to the interrupt controller.

Data is transferred from the serial channel to the dual-port RAM or to the external memory through the peripheral bus. If data is transferred between the SCC channels and external memory, the main controller uses up to six serial DMA channels for the transfer. The main controller also controls all character and address comparison and cyclic redundancy check (CRC) generation and checking.

The execution unit includes the arithmetic logic unit (ALU), which performs arithmetic and logic operations on the registers.

Serial Communication Controllers

The MC68302 has three independent SCCs. Each SCC can be configured to implement different protocols — for example, to perform a gateway function or to interface to an ISDN basic rate channel. To simplify programming, each protocol implementation uses identical data structures.

Five protocols are supported: high-level data link control (HDLC), binary synchronous communication (BISYNC), synchronous/asynchronous digital data communications message protocol (DDCMP), V.110, universal asynchronous receiver transmitter (UART), and a fully transparent mode. To aid system diagnostics, each SCC may be configured to operate in either an echo or loopback mode. In echo mode, the IMP retransmits any signals received; in loopback mode, the IMP locally receives signals originating from itself.

The clock pins (RCLK, TCLK) for each SCC can be programmed for either an external or internal source, with user-programmable baud rates available for each SCC channel.

Each SCC also supports the standard modem control signals: request to send ($\overline{RTS}$), clear to send ($\overline{CTS}$), and carrier detect ($\overline{CD}$). Other modem signals may be provided through the parallel I/O pins.

The SCC features are as follows:

- Programmable Baud Rate Generator Driven by the Internal or External Clock
- Data May Be Clocked by the Programmable Baud Rate Generator or Directly by an External Clock
- Provides Modem Signals $\overline{RTS}$, $\overline{CTS}$, and $\overline{CD}$
- Full-Duplex Operation
- Automatic Echo Mode

- Local Loopback Mode
- Baud Rate Generator Outputs Available Externally

The SCC HDLC mode key features are as follows:

- Flexible Data Buffers with Multiple Buffers per Frame Allowed
- Separate Interrupts for Frames and Buffers (Receive and Transmit)
- Four Address Comparison Registers with Mask
- Maintenance of Five 16-Bit Error Counters
- Flag/Abort/Idle Generation/Detection
- Zero Insertion/Deletion
- NRZ/NRZI Data Encoding
- 16-Bit or 32-Bit CRC-CCITT Generation/Checking
- Detection of Non-Octet Aligned Frames
- Detection of Frames That Are Too Long
- Programmable 0–15 FLAGS between Successive Frames
- Automatic Retransmission in Case of Collision

The SCC BISYNC mode key features are as follows:

- Flexible Data Buffers
- Eight Control Character Recognition Registers
- Automatic SYNC1 and SYNC2 Detection
- SYNC/DLE Stripping and Insertion
- CRC-16 and LRC Generation/Checking
- Parity (VRC) Generation/Checking
- Supports BISYNC Transparent Operation (Use of DLE Characters)
- Supports Promiscuous (Totally Transparent) Reception and Transmission
- Maintains Parity Error Counter
- External SYNC Support
- Reverse Data Mode

The SCC DDCMP mode key features are as follows:

- Synchronous or Asynchronous DDCMP Links Supported
- Flexible Data Buffers
- Four Address Comparison Registers with Mask
- Automatic Frame Synchronization
- Automatic Message Synchronization by Searching for SOH, ENQ, or DLE
- CRC-16 Generation/Checking
- NRZ/NRZI Data Encoding
- Maintenance of Four 16-Bit Error Counters

The SCC V.110 mode key features are as follows:

- Provides Synchronization and Reception of 80-Bit Frames
- Automatic Detection of Framing Errors
- Allows Transmission of the 80-Bit Frame

The SCC UART mode key features are as follows:

- Flexible Message-Oriented Data Buffers
- Multidrop Operation
- Receiver Wakeup on Idle Line or Address Mode
- Eight Control Character Comparison Registers
- Two Address Comparison Registers
- Four 16-Bit Error Counters
- Programmable Data Length (7–8 Bits)
- Programmable 1 or 2 Stop Bits with Fractional Stop Bits
- Even/Odd/Force/No Parity Generation
- Even/Odd/No Parity Check
- Frame Error, Noise Error, Break, and Idle Detection
- Transmits Idle and Break Sequences
- Freeze Transmission Option
- Maintenance of Four 16-Bit Error Counters
- Provides Asynchronous Link over which DDCMP May Be Used
- Flow Control Character Transmission Supported

Serial Communication Port

The SCP is a full-duplex, synchronous, character-oriented channel which provides a three-wire interface (TXD, RXD, and clock). The SCP consists of independent transmitter and receiver sections and a common SCP clock generator. The transmitter and receiver section use the same clock, which is derived from the main clock by an on-chip baud rate generator. The MC68302 is an SCP master, generating both the enable and the clock signals. The enable signals may be generated by the general-purpose I/O pins.

The SCP allows the MC68302 to communicate with a variety of serial devices for the exchange of status and control information using a subset of the Motorola serial peripheral interface (SPI). Such devices may include industry-standard CODECs (e.g., Motorola MC145474 S/T transceiver) and other microcontrollers and peripherals.

The SCP can be configured to operate in a local loopback mode, which is useful for diagnostic functions. The receiver and the transmitter operate normally in these modes.

The SCP features are as follows:

- Three-Wire Interface (SPTXD, SPRXD, and SPCLK)
- Full-Duplex Operation
- Clock Rate up to 4.96 MHz
- Programmable Baud Rate Generator
- Local Loopback Capability for Testing Purposes

Serial Management Controllers

The SMCs are two synchronous, full-duplex ports that may be configured to operate in either IDL or GCI mode to handle the maintenance and control portions of these interfaces. The SMC ports are not used in PCM or NMSI modes. The SMC features are as follows:

- Two Modes of Operation — IDL and GCI
- Local Loopback Capability for Testing Purposes
- Full-Duplex Operation
- SMC1 in GCI Mode Detects Collisions on the D Channel

Serial Channels Physical Interface

The serial channels physical interface connects the physical layer serial lines and the serial controllers (three SCCs and two SMCs). The interface implements both the routing and the time-division multiplexing for the full ISDN bandwidth. It supports four buses: IDL, GCI, PCM, and NMSI (a nonmultiplexed modem interface). The multiplexed modes (IDL, GCI, and PCM) also allow multiple channels (e.g., ISDN B channels) or user-defined subchannels to be assigned to a given SCC. The serial interface also supports two testing modes: echo and loopback.

For the IDL and GCI buses, support of management functions in the frame structure is provided by the SCP or SMCs, respectively. Refer to Figure 4 for the serial channels physical interface block diagram.

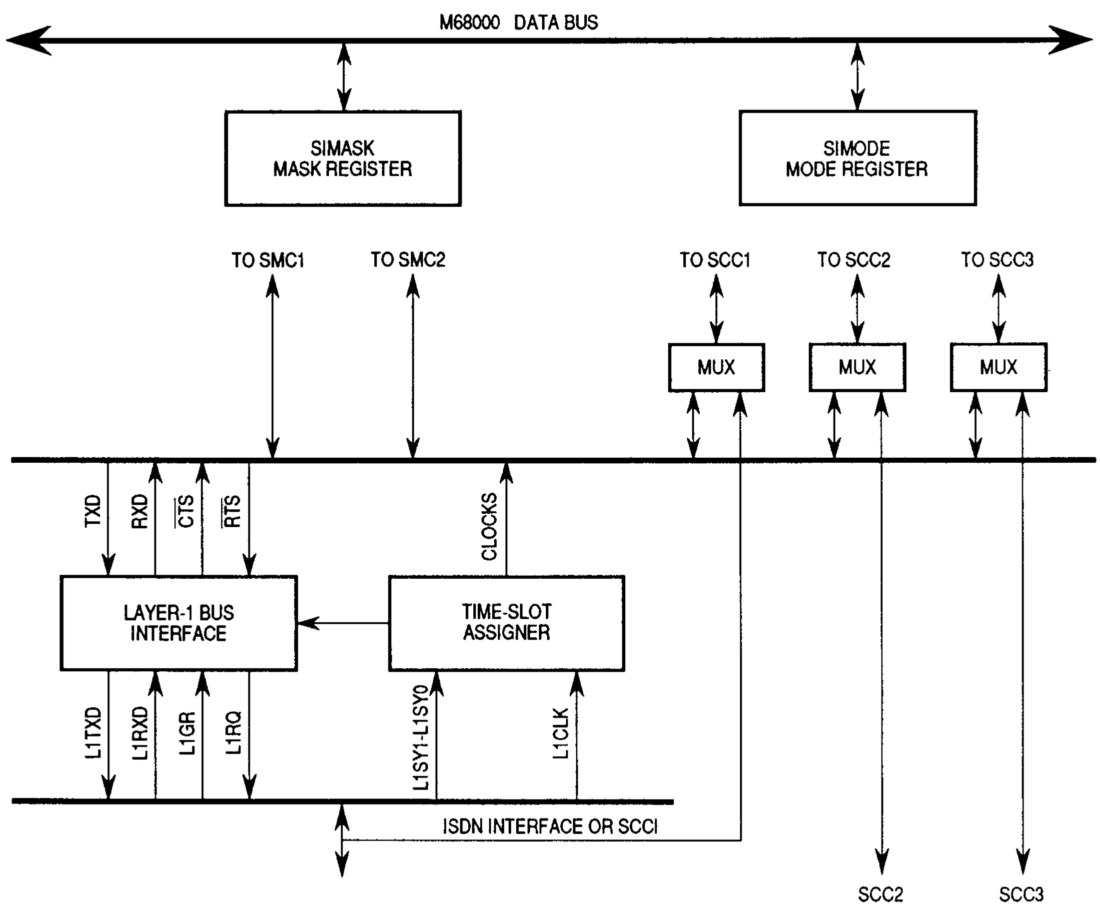


Figure 4. Serial Channels Physical Interface Block Diagram

SIGNAL DESCRIPTIONS

The input and output signals of the MC68302 are organized into functional groups as shown in Table 1 and Figure 5.

Table 1. Signal Definitions

Functional Group	Signals	Num.
Clocks	XTAL, EXTAL, CLKO	3
System Control	$\overline{RESET}$, $\overline{HALT}$, $\overline{BERR}$, BUSW, DISCPU	5
Address Bus	A23–A1	23
Data Bus	D15–D0	16
Bus Control	$\overline{AS}$, R/$\overline{W}$, $\overline{UDS}$/A0, $\overline{LDS}$/$\overline{DS}$, $\overline{DTACK}$	5
Bus Control	$\overline{RMC}$, IAC, $\overline{BCLR}$	3
Bus Arbitration	$\overline{BR}$, $\overline{BG}$, $\overline{BGACK}$	3
Interrupt Control	$\overline{IPL2}$–$\overline{IPL0}$, FC2–FC0, $\overline{AVEC}$	7
NMSI1/ISDN I/F	RXD, TXD, RCLK, TCLK, $\overline{CD}$, $\overline{CTS}$, $\overline{RTS}$, BRG1	8
NMSI2/PIO	RXD, TXD, RCLK, TCLK, $\overline{CD}$, $\overline{CTS}$, $\overline{RTS}$, SDS2	8
NMSI3/SCP/PIO	RXD, TXD, RCLK, TCLK, $\overline{CD}$, $\overline{CTS}$, $\overline{RTS}$, PA12	8
IDMA/PAIO	$\overline{DREQ}$, $\overline{DACK}$, $\overline{DONE}$	3
IACK/PBIO	$\overline{IACK7}$, $\overline{IACK6}$, $\overline{IACK1}$	3
Timer/PBIO	TIN2, TIN1, $\overline{TOUT2}$, $\overline{TOUT1}$, $\overline{WDOG}$	5
PBIO	PB11–PB8	4
Chip Select	$\overline{CS3}$–$\overline{CS0}$	4
Testing	$\overline{FRZ}$ (2 Spare)	3
V_{DD}		8
GND		13

Power Pins

There are eight power pins (V_{DD}).

Ground Pins

There are thirteen ground pins (GND).

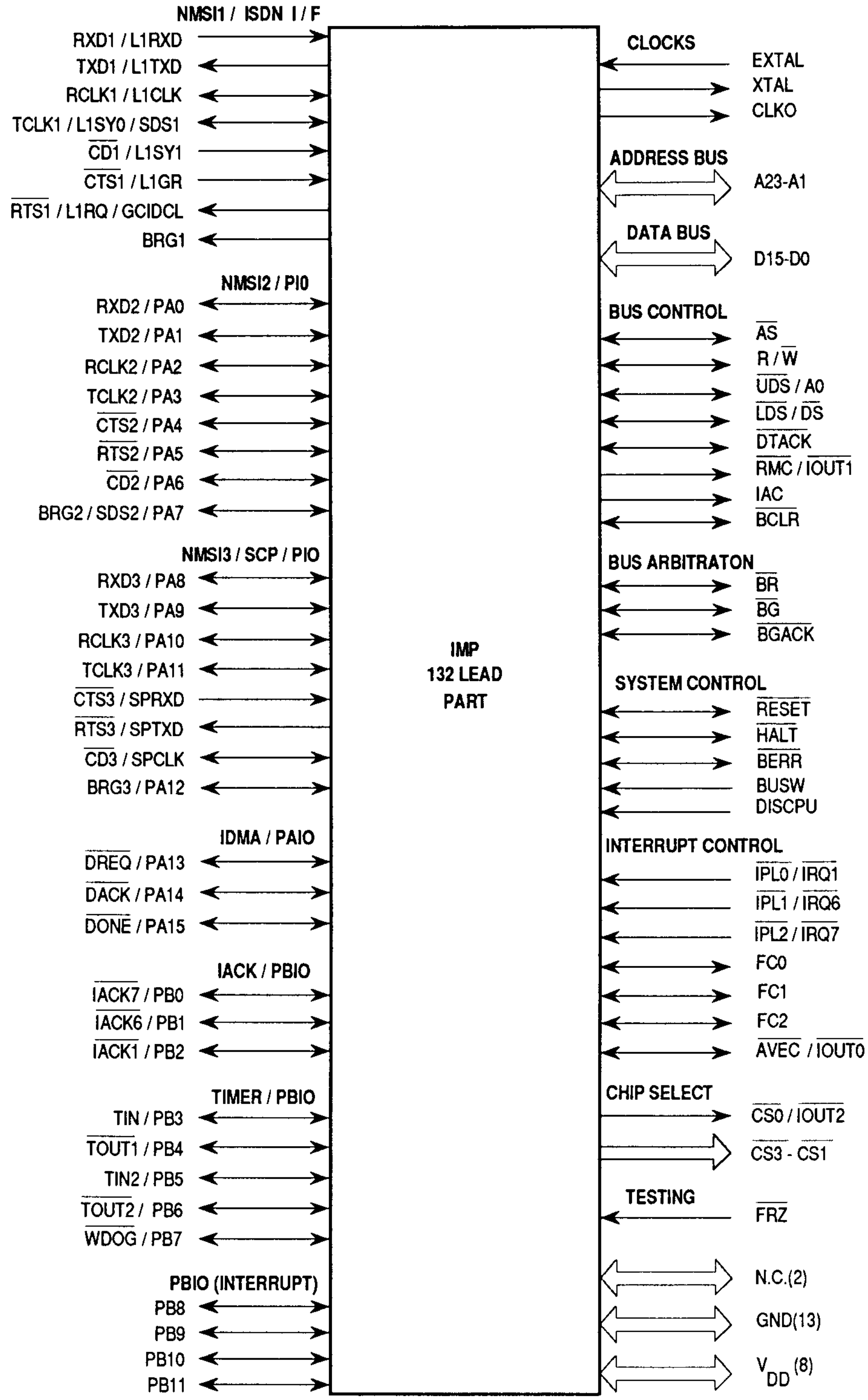


Figure 5. Functional Signal Groups

ELECTRICAL SPECIFICATIONS

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock (CLKO pin) and possibly to one or more other signals.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range MC68302 MC68302I	T_A	 0 to 70 0 to 85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{DD}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance for PGA	θ_{JA}	33	°C/W
Thermal Resistance for CQFP	θ_{JA}	46	°C/W

$T_J = T_A + (P_D \cdot \theta_{JA})$

$P_D = (V_{DD} \cdot I_{DD}) + P_{I/O}$

where:

$P_{I/O}$ is the power dissipation on pins.

For $T_A = 70°C$ and $P_D = 0.5$ W @ 12.5 MHz

$T_J = 88°C$

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = $I_{DD} \times V_{DD}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < 0.3 \cdot P_{INT}$ and can be neglected.

If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

POWER DISSIPATION

Characteristic	Symbol	Min	Max	Unit
Power Dissipation (Typical at 16.67 MHz) (See Note 1)	P_D	53	64	mA
Power Dissipation (Typical at 8 MHz) (See Note 1)	P_D	26	31	mA
Low Power Mode Dissipation (Typical at 16.67 MHz) (See Note 3)	LP_D	—	36	mA
Lowest Power Mode Dissipation (Typical at 16.67 MHz) (See Note 4)	LP_D	—	32	mA
Lowest Power Mode Dissipation (Typical at 50 kHz) (See Note 2)	LP_D	—	1	mA

NOTES:

1. The values shown are typical. The typical value varies as shown, based on how many IMP on-chip peripherals are enabled and the rate at which they are clocked.
2. The stated frequency must be externally applied to EXTAL only after the IMP has been placed in the lowest power mode with LPREC = 1. The M68000 core is not specified to operate at this frequency, but the rest of the IMP is. In this configuration, the user does not divide the clock internally using the LPCD4–LPCD0 bits in the system control register.
3. LPREC = 0. Divider = 2.
4. LPREC = 1. Divider = 1024.

DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input High Voltage (Except EXTAL)	V_{IH}	2.0	V_{DD}	V
Input Low Voltage (Except EXTAL)	V_{IL}	$V_{SS}-0.3$	0.8	V
Input High Voltage (EXTAL)	V_{CIH}	4.0	V_{DD}	V
Input Low Voltage (EXTAL)	V_{CIL}	$V_{SS}-0.3$	0.6	V
Input Leakage Current	I_{IN}	—	20	μA
Input Capacitance All Pins	C_{IN}	—	15	pF
Three-State Leakage Current (2.4/0.5 V)	I_{TSI}	—	20	μA
Open Drain Leakage Current (2.4 V)	I_{OD}	—	20	μA
Output High Voltage (I_{OH} = 400 μA)	V_{OH}	$V_{DD}-1.0$	—	V
Output Low Voltage	V_{OL}			V
(I_{OL} = 3.2 mA) A1–A23, PB0–PB11, FC0–FC3, $\overline{CS0}$–$\overline{CS3}$ IAC, $\overline{AVEC}$, $\overline{BG}$, RCLK1, RCLK2, RCLK3, TCLK1, TCLK2, TCLK3, $\overline{RTS1}$, $\overline{RTS2}$, $\overline{RTS3}$, $\overline{SDS2}$, PA12, RXD2, RXD3, $\overline{CTS2}$, $\overline{CD2}$, $\overline{CD3}$ $\overline{DREQ}$		—	0.5	
(I_{OL} = 5.3 mA) $\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$, R/$\overline{W}$, $\overline{BERR}$, $\overline{BGACK}$, $\overline{BCLR}$, $\overline{DTACK}$, DACK, $\overline{RMC}$, $\overline{RMC}$, D0–D15, $\overline{RESET}$		—	0.5	
(I_{OL} = 7.0 mA) TXD1, TXD2, TXD3		—	0.5	
(I_{OL} = 8.9 mA) $\overline{BR}$, $\overline{DONE}$, $\overline{HALT}$, ($\overline{BR}$ as output)		—	0.5	
(I_{OL} = 3.2 mA) CLKO		—	0.4	
Output Drive CLKO	O_{CLK}	—	50	pF
Output Drive ISDN I/F (GCI Mode)	O_{GCI}	—	150	pF
Output Drive All Other Pins	O_{ALL}	—	130	pF

DC ELECTRICAL CHARACTERISTICS — NMSI1 IN IDL MODE

Characteristic	Symbol	Min	Nom	Max	Unit	Condition
Power	V_{DD}	4.5	5.0	5.5	V	
Common	V_{SS}	0	0	0	V	
Temperature	T	0	25	70	°C	Operating Range
Input Pin Characteristics: L1CLK, L1SY1, L1RXD, L1GR						
Input Low Level Voltage	V_{IL}	−10%		+20%	V	(% of V_{DD})
Input High Level Voltage	V_{IH}	V_{DD} −20%		V_{DD} +10%	V	
Input Low Level Current	I_{IH}	—		±10	μA	$V_{in} = V_{SS}$
Input High Level Current	I_{IH}	—		±10	μA	$V_{in} = V_{DD}$
Output Pin Characteristics: L1TXD, SDS1–SDS2, L1RQ						
Output Low Level Voltage	V_{OL}	0		0.50	V	I_{OL} = 2.0 mA
Output High Level Voltage	V_{OH}	$V_{DD}-0.5$		V_{DD}	V	I_{OH} = 2.0 mA

AC ELECTRICAL SPECIFICATIONS — CLOCK TIMING

(see Figures 6, 7, 8, and 9)

Num.	Characteristic	Symbol	16.67 MHz		Unit
			Min	Max	
	Frequency of Operation	f	8	16.67	MHz
1	Clock Period (EXTAL)	t_{cyc}	60	125	ns
2, 3	Clock Pulse Width (EXTAL)	t_{CL}, t_{CH}	25	62.5	ns
4, 5	Clock Rise and Fall Times (EXTAL)	t_{Cr}, t_{Cf}	—	5	ns
5a	EXTAL to CLKO Delay (See Notes 1 and 2)	t_{CD}	2	11	ns

NOTE:

1. CLKO loading is 50 pF max.
2. CLKO skew from the rising and falling edges of EXTAL will not differ from each other by more than 1 ns, if the EXTAL rise time equals the EXTAL fall time.

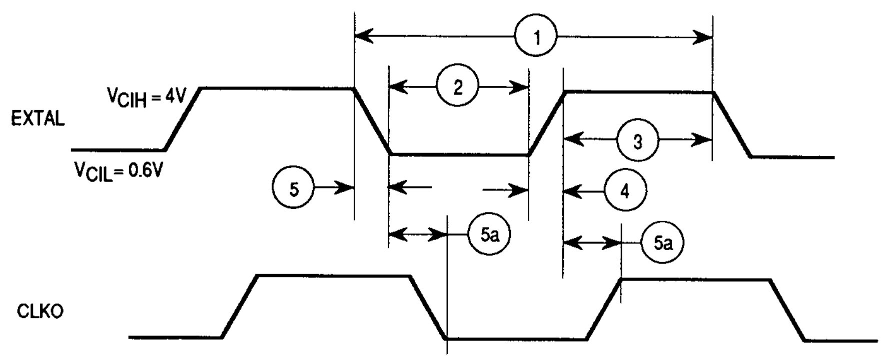


Figure 6. Clock Timing Diagram

AC ELECTRICAL SPECIFICATIONS — IMP BUS MASTER CYCLES

(see Figures 7, 8, and 9)

Num.	Characteristic	Symbol	16.67 MHz		Unit
			Min	Max	
6	Clock High to FC, Address Valid	$t_{CHFCADV}$	—	45	ns
7	Clock High to Address, Data Bus High Impedance (Maximum)	t_{CHADZ}	—	50	ns
8	Clock High to Address, FC Invalid (Minimum)	t_{CHAFI}	0	—	ns
9	Clock High to $\overline{AS}$, $\overline{DS}$ Asserted (see Note 1)	t_{CHSL}	3	30	ns
11	Address, FC Valid to $\overline{AS}$, $\overline{DS}$ Asserted (Read)/$\overline{AS}$ Asserted (Write) (see Note 2)	t_{AFCVSL}	15	—	ns
12	Clock Low to $\overline{AS}$, $\overline{DS}$ Negated (see Note 1)	t_{CLSH}	—	30	ns
13	$\overline{AS}$, $\overline{DS}$ Negated to Address, FC Invalid (see Note 2)	t_{SHAFI}	15	—	ns
14	$\overline{AS}$ (and $\overline{DS}$ Read) Width Asserted (see Note 2)	t_{SL}	120	—	ns
14A	$\overline{DS}$ Width Asserted, Write (see Note 2)	t_{DSL}	60	—	ns
15	$\overline{AS}$, $\overline{DS}$ Width Negated (see Note 2)	t_{SH}	60	—	ns
16	Clock High to Control Bus High Impedance	t_{CHCZ}	—	50	ns
17	$\overline{AS}$, $\overline{DS}$ Negated to R/$\overline{W}$ Invalid (see Note 2)	t_{SHRH}	15	—	ns
18	Clock High to R/$\overline{W}$ High (see Note 1)	t_{CHRH}	—	30	ns
20	Clock High to R/$\overline{W}$ Low (see Note 1)	t_{CHRL}	—	30	ns
20A	$\overline{AS}$ Asserted to R/$\overline{W}$ Low (Write) (see Notes 2 and 6)	t_{ASRV}	—	10	ns
21	Address FC Valid to R/$\overline{W}$ Low (Write) (see Note 2)	t_{AFCVRL}	15	—	ns
22	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write) (see Note 2)	t_{RLSL}	30	—	ns
23	Clock Low to Data-Out Valid	t_{CLDO}	—	30	ns
25	$\overline{AS}$, $\overline{DS}$, Negated to Data-Out Invalid (Write) (see Note 2)	t_{SHDOI}	15	—	ns
26	Data-Out Valid to $\overline{DS}$ Asserted (Write) (see Note 2)	t_{DOSL}	15	—	ns
27	Data-In Valid to Clock Low (Setup Time on Read) (see Note 5)	t_{DICL}	7	—	ns
28	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DTACK}$ Negated (Asynchronous Hold) (see Note 2)	t_{SHDAH}	0	110	ns
29	$\overline{AS}$, $\overline{DS}$ Negated to Data-In Invalid (Hold Time on Read)	t_{SHDII}	0	—	ns
30	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{BERR}$ Negated	t_{SHBEH}	0	—	ns
31	$\overline{DTACK}$ Asserted to Data-In Valid (Setup Time) (see Notes 2 and 5)	t_{DALDI}	—	50	ns
32	$\overline{HALT}$ and $\overline{RESET}$ Input Transition Time	t_{RHr}, t_{RHf}	—	150	ns
33	Clock High to $\overline{BG}$ Asserted	t_{CHGL}	—	30	ns
34	Clock High to $\overline{BG}$ Negated	t_{CHGH}	—	30	ns
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted	t_{BRLGL}	2.5	4.5	clks
36	$\overline{BR}$ Negated to $\overline{BG}$ Negated (see Note 7)	t_{BRHGH}	1.5	2.5	clks
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	t_{GALGH}	2.5	4.5	clks
37A	$\overline{BGACK}$ Asserted to $\overline{BR}$ Negated (see Note 8)	t_{GALBRH}	10	1.5	ns/clks
38	$\overline{BG}$ Asserted to Control, Address, Data Bus High Impedance ($\overline{AS}$ Negated)	t_{GLZ}	—	50	ns
39	$\overline{BG}$ Width Negated	t_{GH}	1.5	—	clks
44	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{AVEC}$ Negated	t_{SHVPH}	0	50	ns
46	$\overline{BGACK}$ Width Low	t_{GAL}	1.5	—	clks
47	Asynchronous Input Setup Time (see Note 5)	t_{ASI}	10	—	ns

—Continued

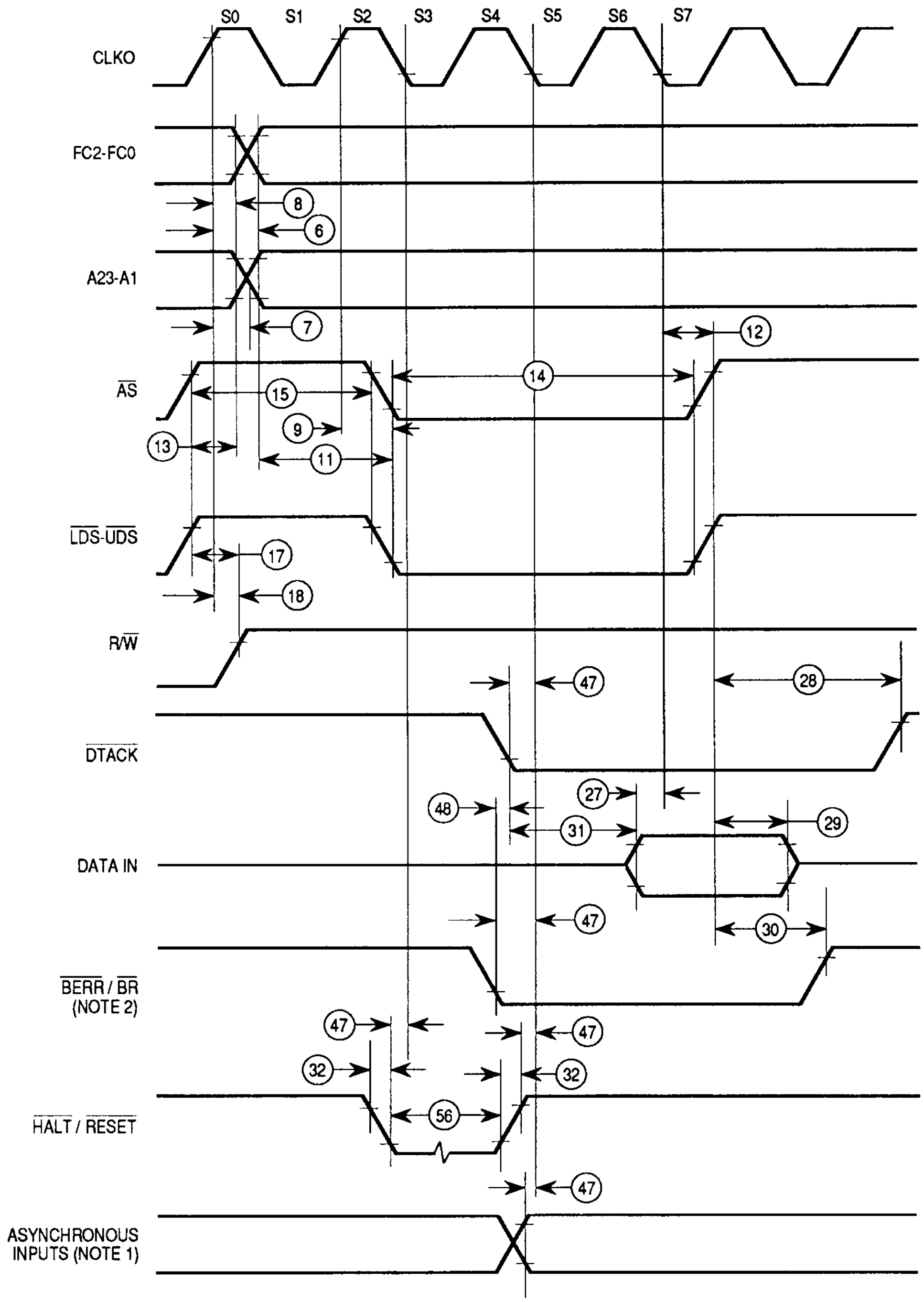
AC ELECTRICAL SPECIFICATIONS — IMP BUS MASTER CYCLES

(Continued) (see Figures 7, 8, and 9)

Num.	Characteristic	Symbol	16.67 MHz		Unit
			Min	Max	
48	$\overline{\text{BERR}}$ Asserted to $\overline{\text{DTACK}}$ Asserted (see Notes 2 and 3)	t_{BELDAL}	10	—	ns
53	Data-Out Hold from Clock High	t_{CHDOI}	0	—	ns
55	R/$\overline{\text{W}}$ Asserted to Data Bus Impedance Change	t_{RLDBD}	0	—	ns
56	$\overline{\text{HALT}}$/$\overline{\text{RESET}}$ Pulse Width (see Note 4)	t_{HRPW}	10	—	clks
57	$\overline{\text{BGACK}}$ Negated to $\overline{\text{AS}}$, $\overline{\text{DS}}$, R/$\overline{\text{W}}$ Driven	t_{GASD}	1.5	—	clks
57A	$\overline{\text{BGACK}}$ Negated to FC	t_{GAFD}	1	—	clks
58	$\overline{\text{BR}}$ Negated to $\overline{\text{AS}}$, $\overline{\text{DS}}$, R/$\overline{\text{W}}$ Driven (see Note 7)	t_{RHSD}	1.5	—	clks
58A	$\overline{\text{BR}}$ Negated to FC (see Note 7)	t_{RHFD}	1	—	clks
60	Clock High to $\overline{\text{BCLR}}$ Asserted	t_{CHBCL}	—	30	ns
61	Clock High to $\overline{\text{BCLR}}$ Negated (See Note 10)	t_{CHBCH}	—	30	ns
62	Clock Low (S0 Falling Edge during read) to $\overline{\text{RMC}}$ Asserted	t_{CLRML}	—	30	ns
63	Clock High (S7 Rising Edge during write) to $\overline{\text{RMC}}$ Negated	t_{CHRMH}	—	30	ns
64	$\overline{\text{RMC}}$ Negated to $\overline{\text{BG}}$ Asserted (see Note 9)	t_{RMHGL}	—	30	ns

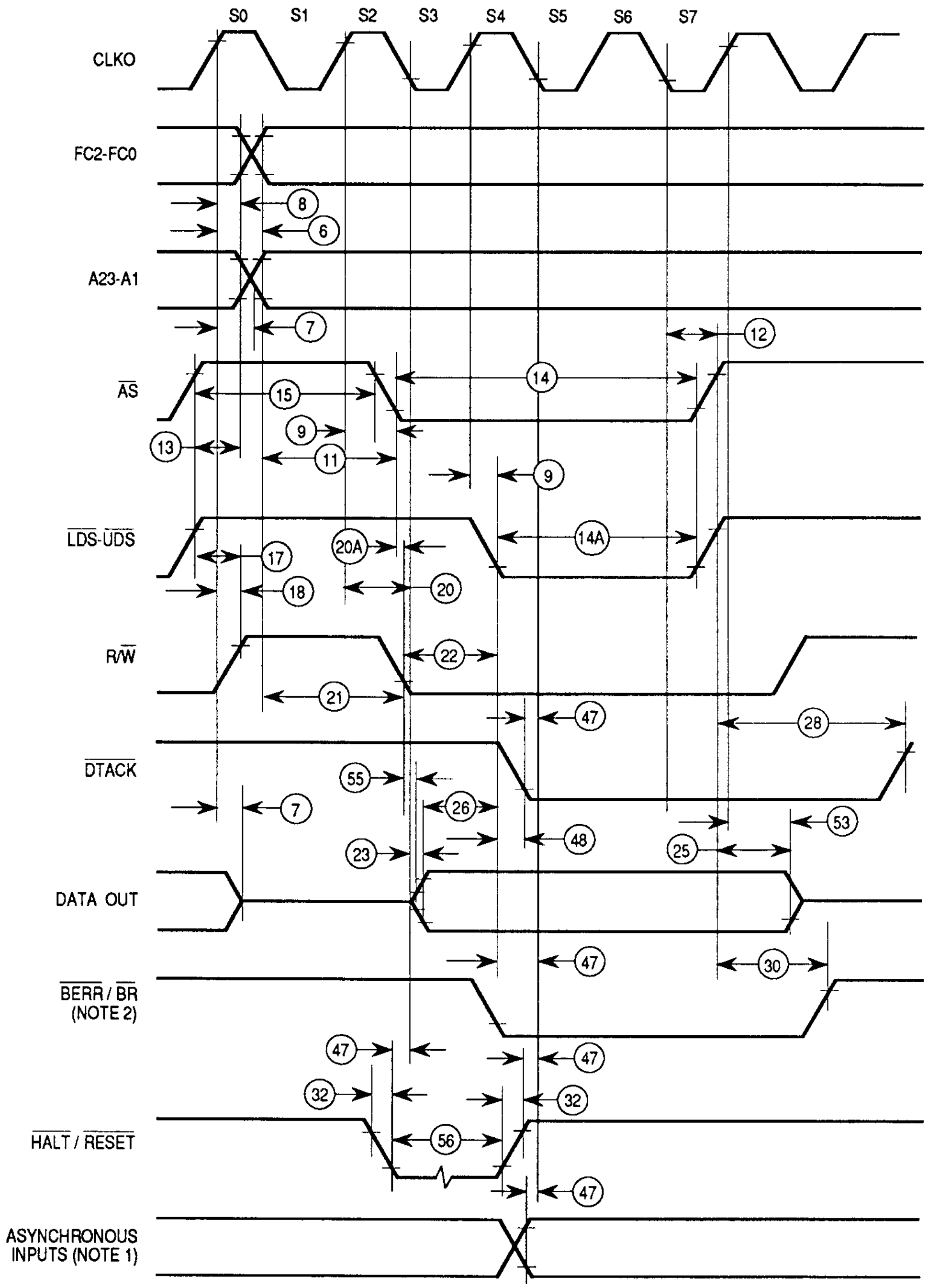
NOTES:

1. For loading capacitance of less than or equal to 50 picofarads, subtract 4 nanoseconds from the value given in the maximum columns.
2. Actual value depends on clock period.
3. If #47 is satisfied for both $\overline{\text{DTACK}}$ and $\overline{\text{BERR}}$, #48 may be ignored. In the absence of $\overline{\text{DTACK}}$, $\overline{\text{BERR}}$ is a synchronous input using the asynchronous input setup time (#47).
4. For powerup, the MC68302 must be held in the reset state for 100 milliseconds to allow stabilization of on-chip circuit. After the system is powered up #56 refers to the minimum pulse width required to reset the processor.
5. If the asynchronous input setup (#47) requirement is satisfied for $\overline{\text{DTACK}}$, the $\overline{\text{DTACK}}$ asserted to data setup time (#31) requirement can be ignored. The data must only satisfy the data-in to clock low setup time (#27) for the following clock cycle.
6. When $\overline{\text{AS}}$ and R/$\overline{\text{W}}$ are equally loaded (±20%), subtract 5 nanoseconds from the values given in these columns.
7. The MC68302 will negate $\overline{\text{BG}}$ and begin driving the bus if external arbitration logic negates $\overline{\text{BR}}$ before asserting $\overline{\text{BGACK}}$.
8. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, $\overline{\text{BG}}$ may be reasserted.
9. This specification is valid only when the RMCST bit is set in the SCR register.
10. Occurs on S0 of SDMA read/write access when the SDMA becomes bus master.



NOTES:
1. Setup time for the asynchronous inputs IPL2-IPL0 guarantees their recognition at the next falling edge of the clock.
2. BR need fall at this time only to insure being recognized at the end of the bus cycle.
3. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 vclt and 2.0 volts.

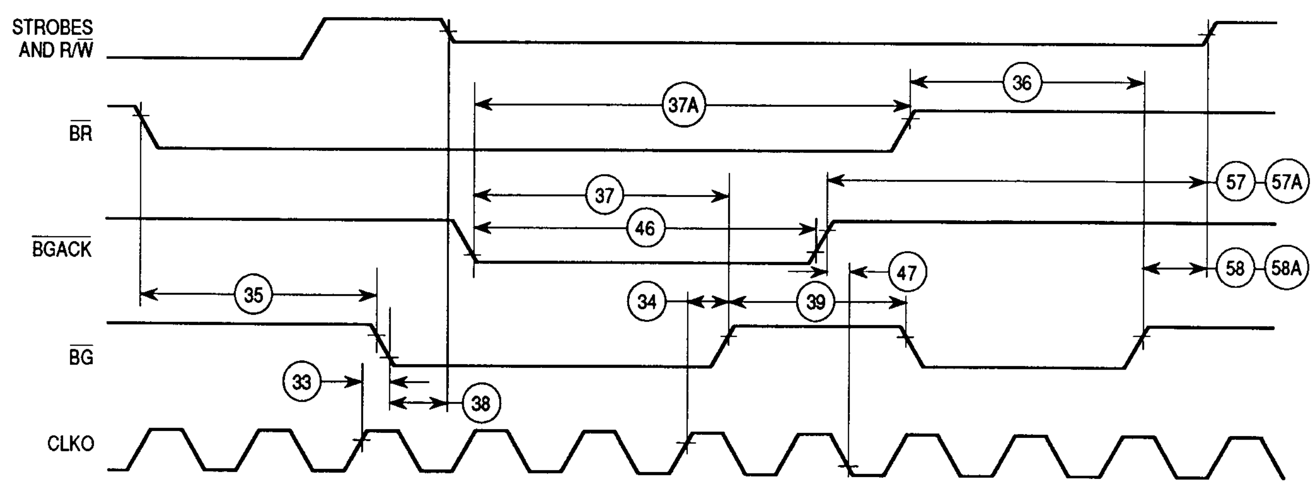
Figure 7. Read-Cycle Timing Diagram



NOTES:

1. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 volt and 2.0 volts.
2. Because of loading variations, R/W may be valid after AS even though both are initiated by the rising edge of S2 (specification #20A).

Figure 8. Write-Cycle Timing Diagram



NOTE: Setup time to the clock (#47) for the asynchronous inputs $\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, and $\overline{IPL2}$-$\overline{IPL0}$ guarantees their recognition at the next falling edge of the clock.

Figure 9. Bus Arbitration Timing Diagram

AC ELECTRICAL SPECIFICATIONS — DMA

(see Figure 10)

Num.	Characteristic	Symbol	16.67 MHz		Unit
			Min	Max	
80	DREQ Asynchronous Setup Time (see Note 1)	t_{REQASI}	15	—	ns
81	DREQ Width Low (see Note 2)	t_{REQL}	2	—	clk
82	DREQ Low to BR Low (see Notes 3 and 4)	$t_{REQLBRL}$	—	2	clk
83	Clock High to BR Low (see Notes 3 and 4)	t_{CHBRL}	—	30	ns
84	Clock High to BR High Impedance (see Notes 3 and 4)	t_{CHBRZ}	—	30	ns
85	BGACK Low to BR High Impedance (see Notes 3 and 4)	t_{BKLBRZ}	30	—	ns
86	Clock High to BGACK Low	t_{CHBKL}	—	30	ns
87	AS and BGACK High (the latest one) to BGACK Low (when BG is Asserted)	t_{ABHBKL}	1.5	2.5 +30	clk ns
88	BG Low to BGACK Low (No Other Bus Master) (see Notes 3 and 4)	t_{BGLBKL}	1.5	2.5 +30	clk ns
89	BR High Impedance to BG High (see Notes 3 and 4)	t_{BRHBGH}	0	—	ns
90	Clock on Which BGACK Low to Clock on Which AS Low	$t_{CLBKLAL}$	2	2	clk
91	Clock High to BGACK High	t_{CHBKH}	—	30	ns
92	Clock Low to BGACK High Impedance	t_{CLBKZ}	—	15	ns
93	Clock High to DACK Low	t_{CHACKL}	—	30	ns
94	Clock Low to DACK High	t_{CLACKH}	—	30	ns
95	Clock High to DONE Low (Output)	t_{CHDNL}	—	30	ns
96	Clock Low to DONE High Impedance	t_{CLDNZ}	—	30	ns
97	DONE Input Low to Clock High (Asynchronous Setup)	t_{DNLTCH}	15	—	ns

NOTES:
1. DREQ is sampled on the falling edge of CLK in cycle steal and burst modes.
2. If #80 is satified for DREQ, #81 may be ignored.
3. BR will not be asserted while AS, HALT, or BERR is asserted.
4. Specifications are for DISABLE CPU mode only.
5. DREQ, DACK, and DONE do not apply to the SDMA channels.
6. IDMA and SDMA read and write cycle timing is the same as that for the M68000 core.

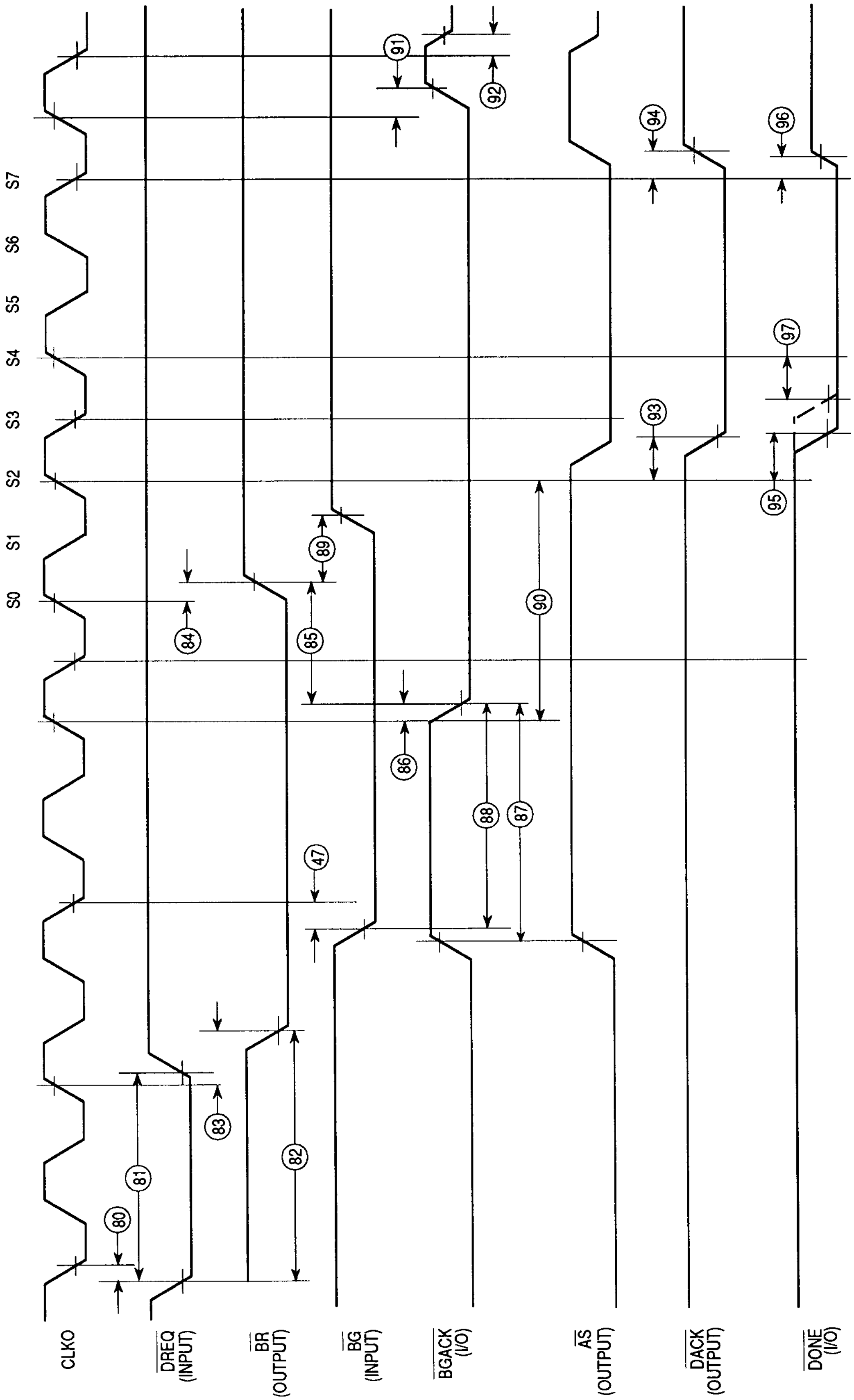


Figure 10. DMA Timing Diagram

AC ELECTRICAL SPECIFICATIONS — EXTERNAL MASTER INTERNAL ASYNCHRONOUS READ/WRITE CYCLES

(see Figures 11 and 12)

Num.	Characteristic	Symbol	16.67 MHz		Unit
			Min	Max	
100	R/$\overline{\text{W}}$ Valid to $\overline{\text{DS}}$ Low	t_{RWVDSL}	0	—	ns
101	$\overline{\text{DS}}$ Low to Data In Valid	t_{DSLDIV}	—	30	ns
102	$\overline{\text{DTACK}}$ Low to Data In Hold Time	t_{DKLDH}	0	—	ns
103	$\overline{\text{AS}}$ Valid to $\overline{\text{DS}}$ Low	t_{ASVDSL}	0	—	ns
104	$\overline{\text{DTACK}}$ Low to $\overline{\text{DS}}$ High	t_{DKLDSH}	0	—	ns
105	$\overline{\text{DS}}$ High to $\overline{\text{DTACK}}$ High	t_{DSHDKH}	—	45	ns
106	$\overline{\text{DS}}$ Inactive to $\overline{\text{AS}}$ Inactive	t_{DSIASI}	0	—	ns
107	$\overline{\text{DS}}$ High to R/$\overline{\text{W}}$ High	t_{DSHRWH}	0	—	ns
108	$\overline{\text{DS}}$ High to Data High Impedance	t_{DSHDZ}	—	45	ns
108A	$\overline{\text{DS}}$ High to Data Out Hold Time	t_{DSHDH}	0	—	ns
109	$\overline{\text{DS}}$ High to Data In Hold Time (see Note)	t_{DSHDOH}	0	—	ns
109A	Data Out Valid to $\overline{\text{DTACK}}$ Low	t_{DOVDKL}	15	—	ns

NOTE: If $\overline{\text{AS}}$ is negated before $\overline{\text{DS}}$, the data bus could be three-stated (spec 126) before $\overline{\text{DS}}$ is negated.

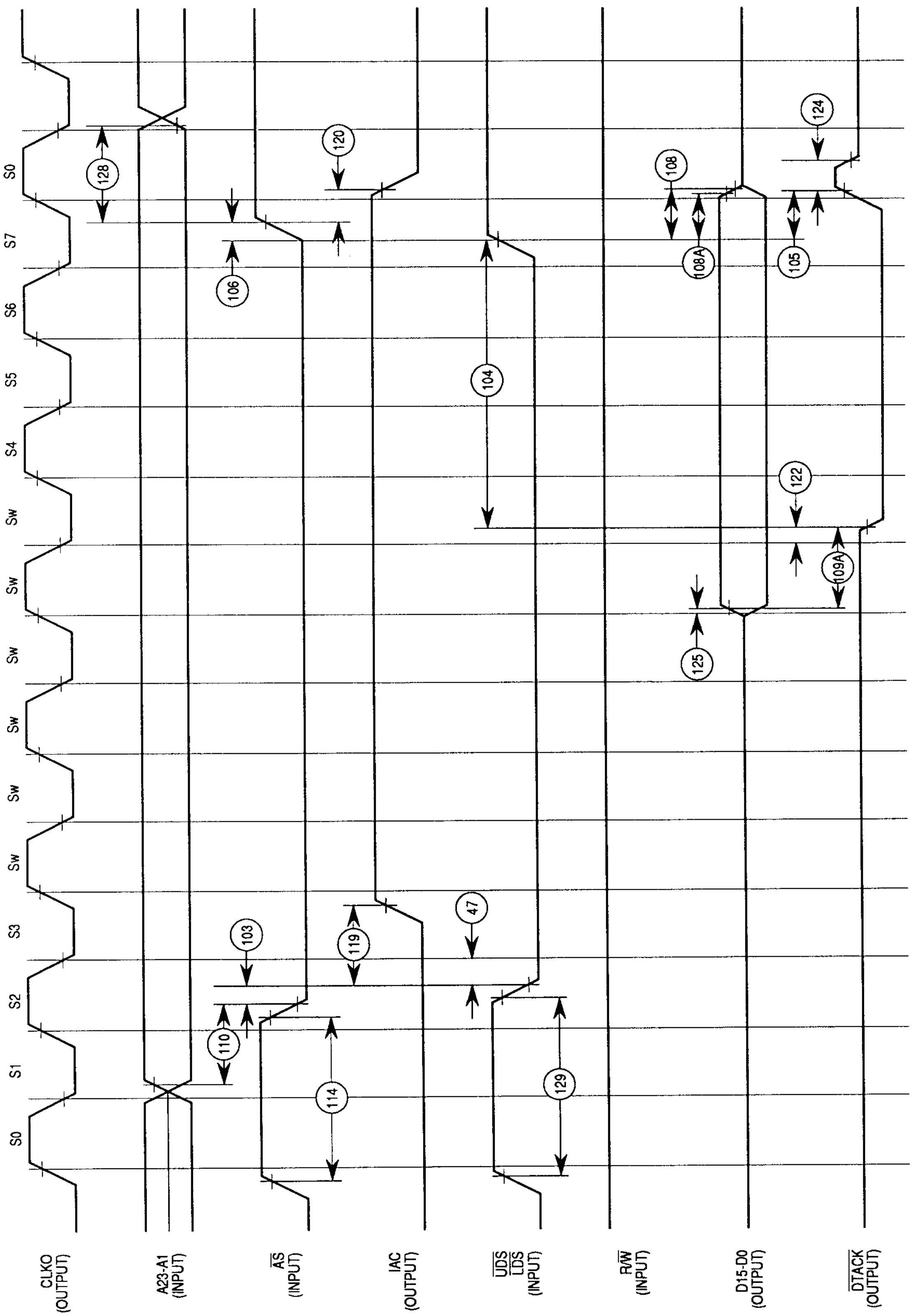


Figure 11. External Master Internal Asynchronous Read Cycle Timing Diagram

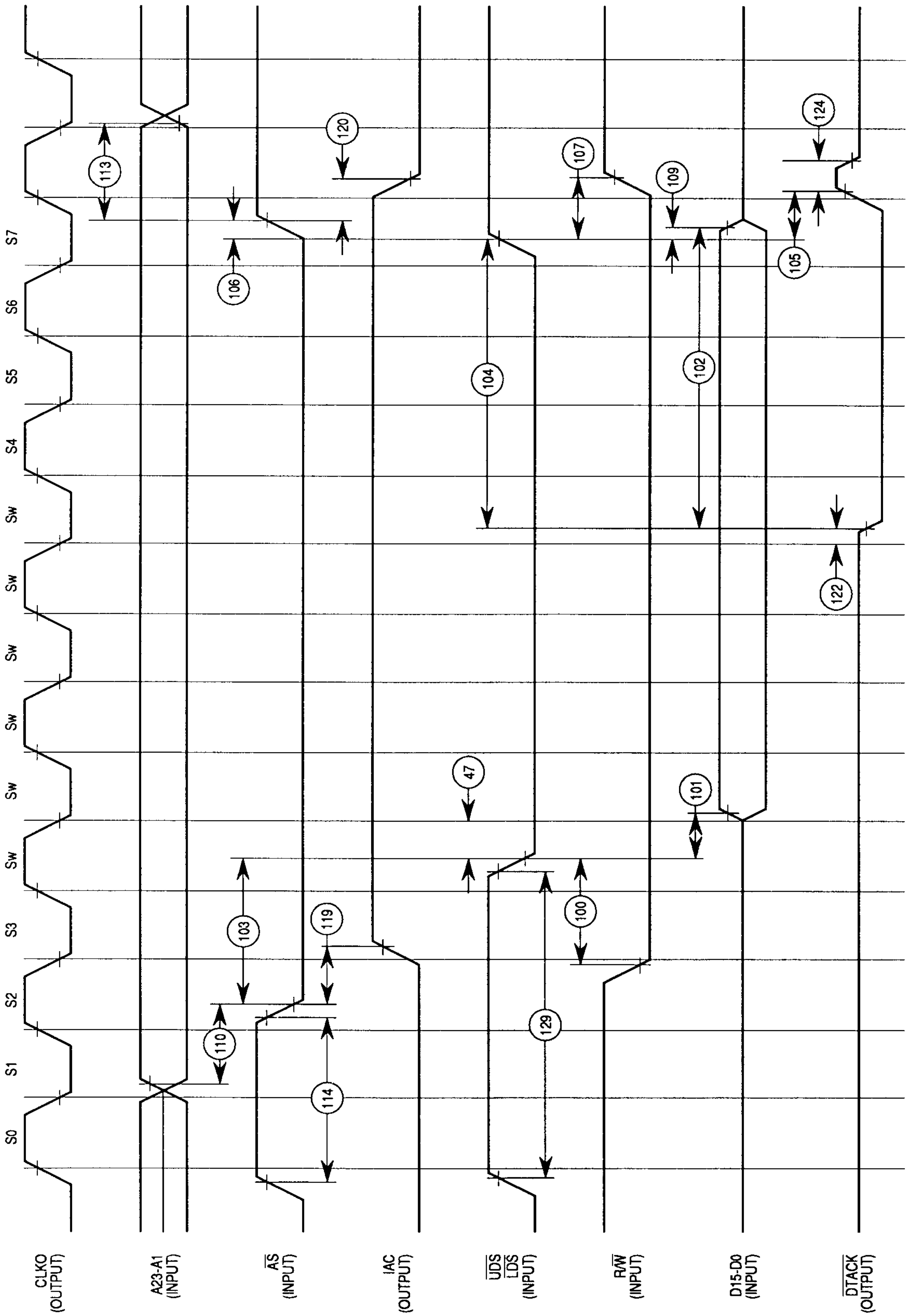


Figure 12. External Master Internal Asynchronous Write Cycle Timing Diagram

AC ELECTRICAL SPECIFICATIONS — EXTERNAL MASTER INTERNAL SYNCHRONOUS READ/WRITE CYCLES (see Figures 13, 14, and 15)

Num.	Characteristic	Symbol	16.67 MHz		Unit
			Min	Max	
110	Address Valid to $\overline{AS}$ Low	t_{AVASL}	15	—	ns
111	$\overline{AS}$ Low to Clock High	t_{ASLCH}	30	—	ns
112	Clock Low to $\overline{AS}$ High	t_{CLASH}	—	45	ns
113	$\overline{AS}$ High to Address Hold Time on Write	t_{ASHAH}	0	—	ns
114	$\overline{AS}$ Inactive Time	t_{ASH}	1	—	clk
115	$\overline{UDS}$/$\overline{LDS}$ Low to Clock High	t_{SLCH}	40	—	ns
116	Clock Low to $\overline{UDS}$/$\overline{LDS}$ High	t_{CLSH}	—	45	ns
117	R/$\overline{W}$ Valid to Clock High	t_{RWVCH}	30	—	ns
118	Clock High to R/$\overline{W}$ High	t_{CHRWH}	—	45	ns
119	$\overline{AS}$ Low to IAC High	t_{ASLIAH}	—	40	ns
120	$\overline{AS}$ High to IAC Low	t_{ASHIAL}	—	40	ns
121	$\overline{AS}$ Low to $\overline{DTACK}$ Low (0 Wait State)	t_{ASLDTL}	—	45	ns
122	Clock Low to $\overline{DTACK}$ Low (1 Wait State)	t_{CLDTL}	—	30	ns
123	$\overline{AS}$ High to $\overline{DTACK}$ High	t_{ASHDTH}	—	45	ns
124	$\overline{DTACK}$ High to $\overline{DTACK}$ High Impedance	t_{DTHDTZ}	—	15	ns
125	Clock High to Data Out Valid	t_{CHDOV}	—	30	ns
126	$\overline{AS}$ High to Data High Impedance	t_{ASHDZ}	—	45	ns
127	$\overline{AS}$ High to Data Out Hold Time	t_{ASHDOI}	0	—	ns
128	$\overline{AS}$ High to Address Hold Time on Read	t_{ASHAI}	0	—	ns
129	$\overline{UDS}$/$\overline{LDS}$ Inactive Time	t_{SH}	1	—	clk
130	Data In Valid to Clock Low	t_{CLDIV}	30	—	ns
131	Clock Low to Data In Hold Time	t_{CLDIH}	15	—	ns

NOTE: Specifications are valid only when SAM = 1 in the SCR.

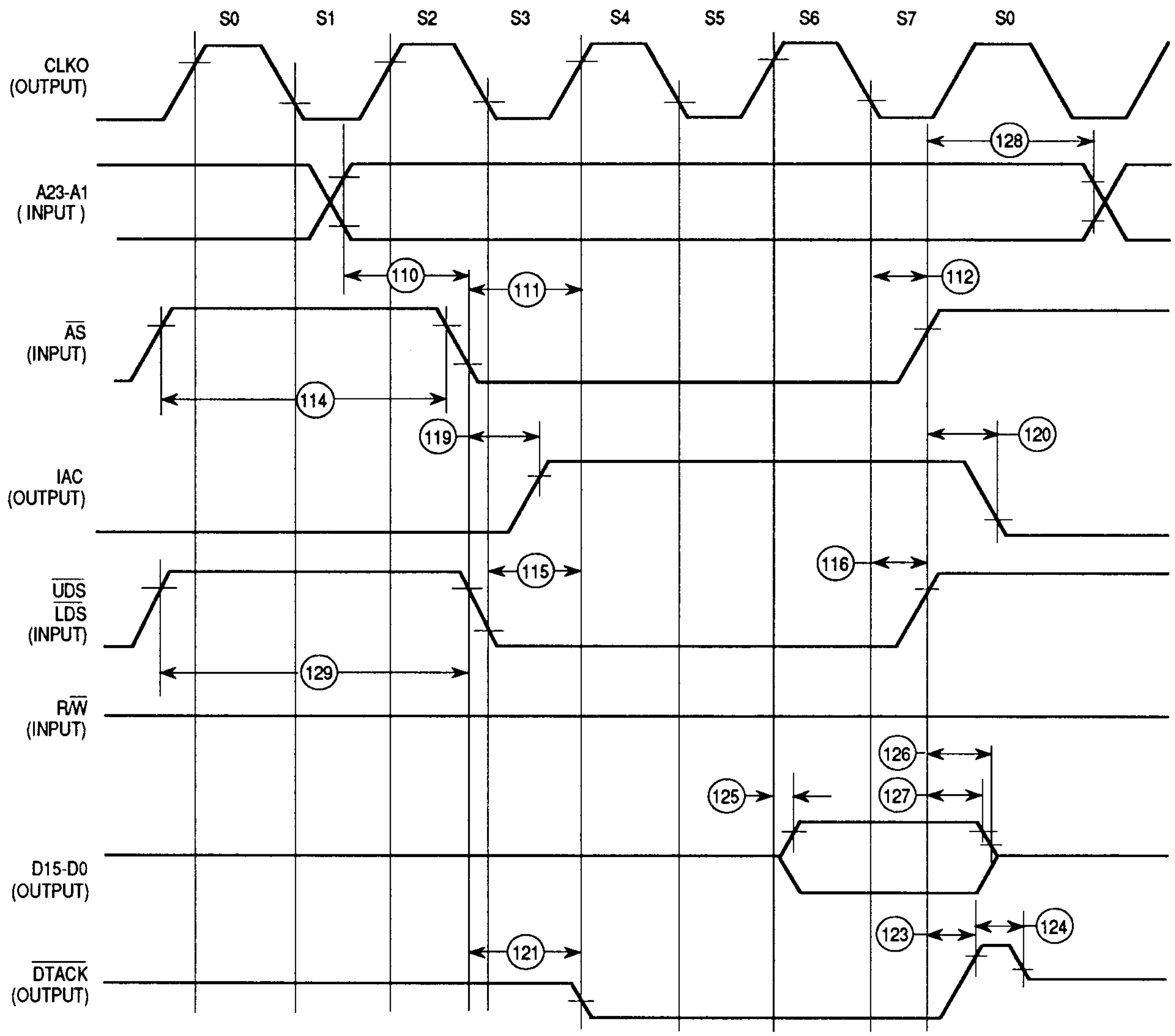


Figure 13. External Master Internal Synchronous Read Cycle Timing Diagram

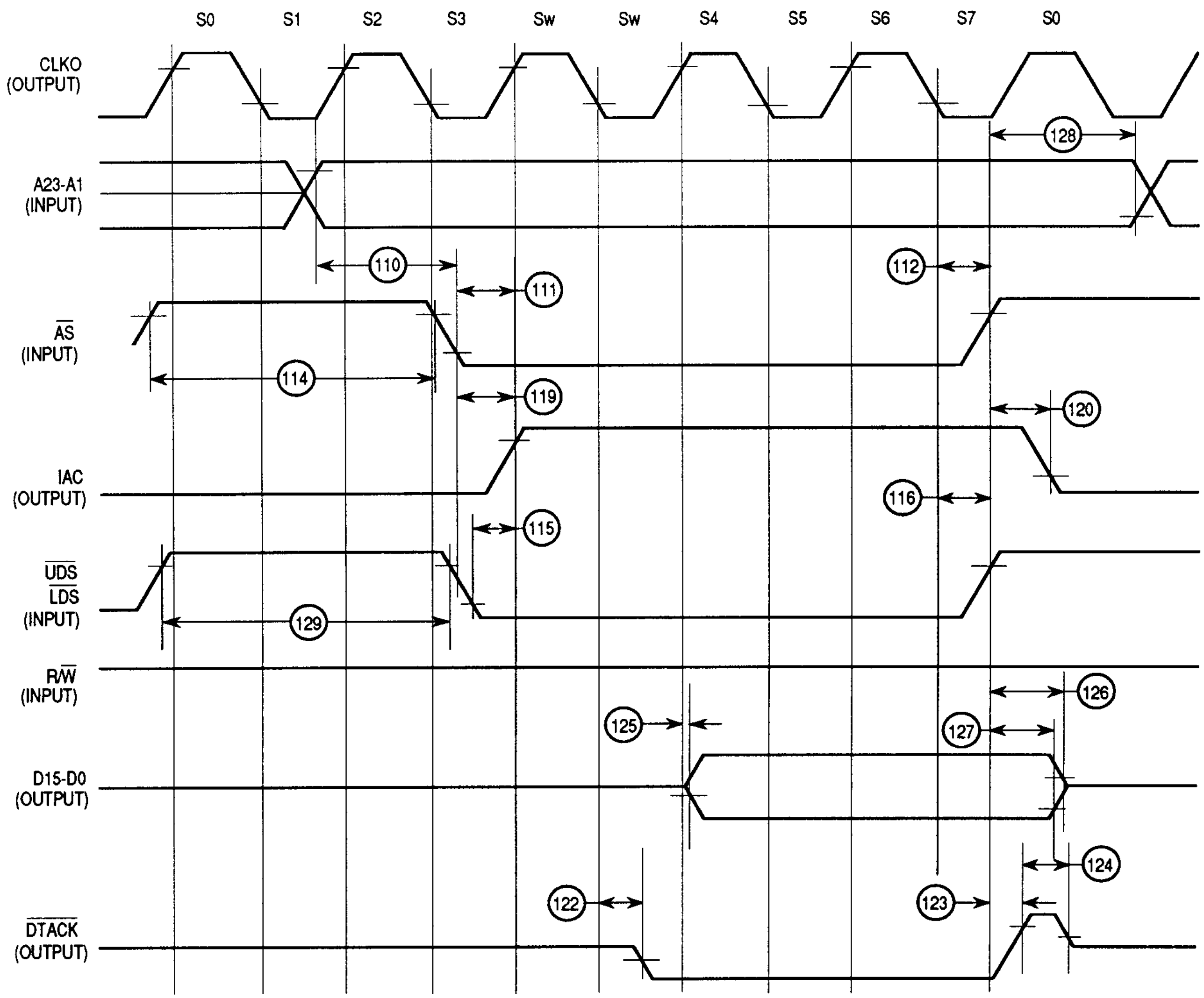


Figure 14. External Master Internal Synchronous Read Cycle Timing Diagram (One Wait State)

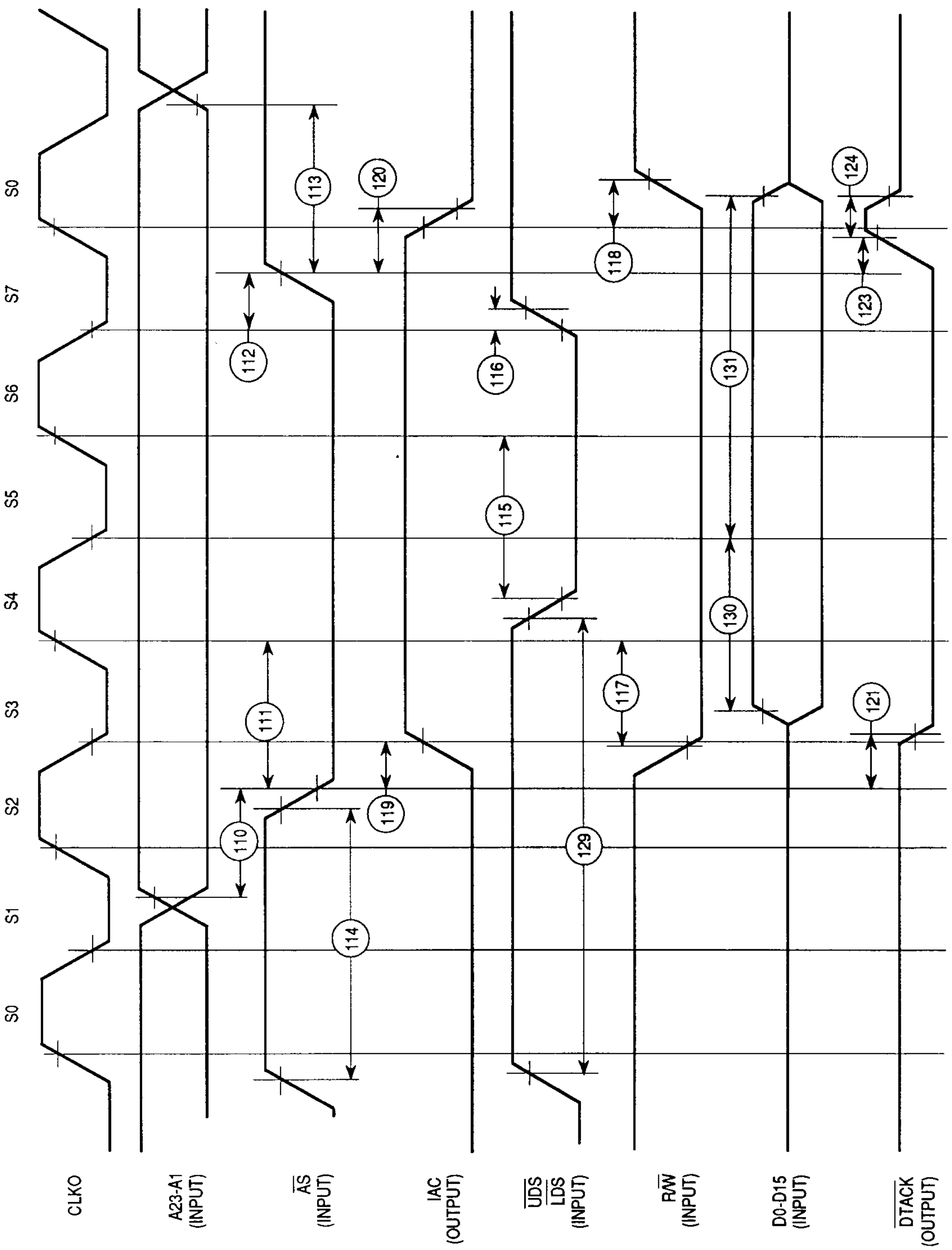


Figure 15. External Master Internal Synchronous Write Cycle Timing Diagram

AC ELECTRICAL SPECIFICATIONS — INTERNAL MASTER INTERNAL READ/WRITE CYCLES (see Figure 16)

Num.	Characteristic	Symbol	16.67 MHz Min	16.67 MHz Max	Unit
140	Clock High to IAC High	t_{CHIAH}	—	40	ns
141	Clock Low to IAC Low	t_{CLIAL}	—	40	ns
142	Clock High to $\overline{DTACK}$ Low (0 Wait State)	t_{CHDTL}	—	45	ns
143	Clock Low to $\overline{DTACK}$ High	t_{CLDTH}	—	40	ns
144	Clock High to Data Out Valid	t_{CHDOV}	—	30	ns
145	$\overline{AS}$ High to Data Out Hold Time	t_{ASHDOH}	0	—	ns

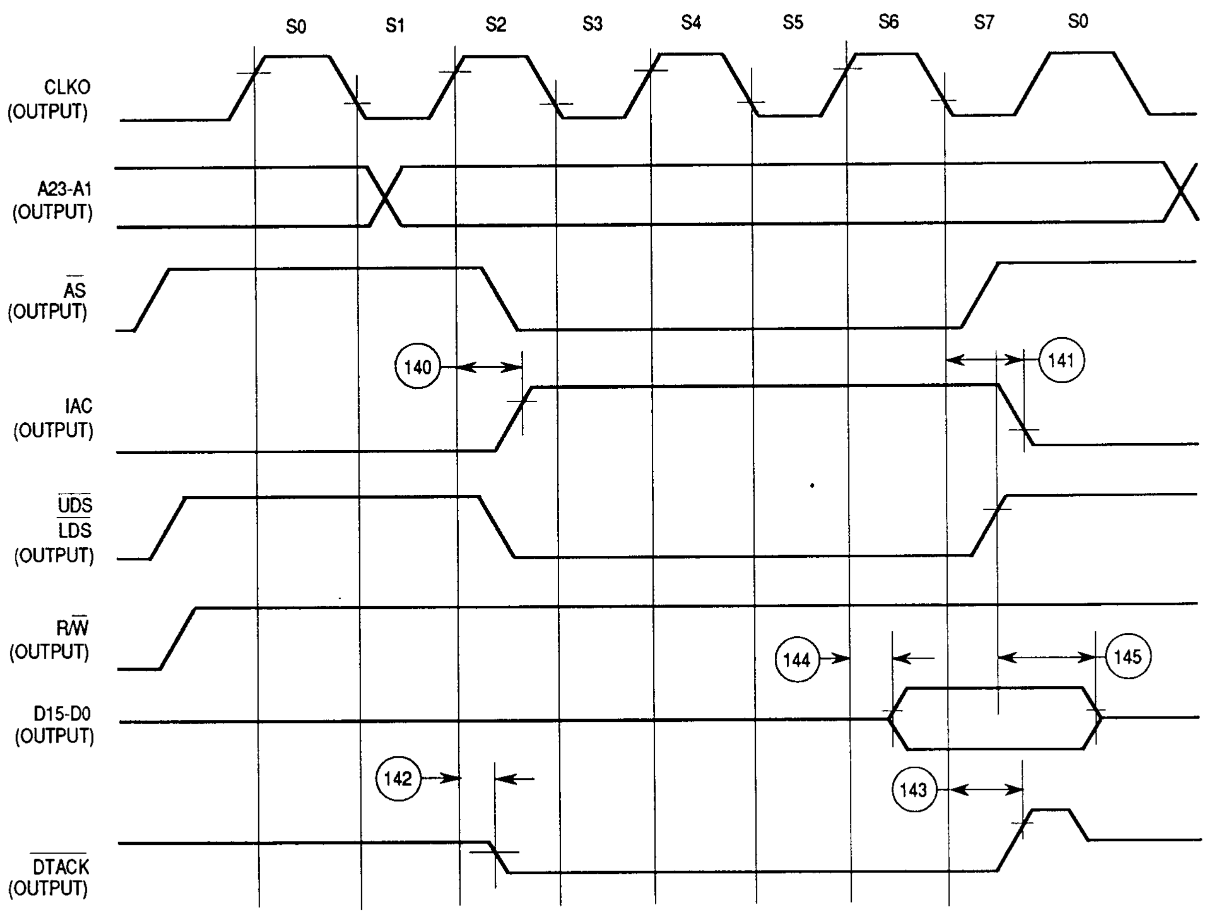


Figure 16. Internal Master Internal Read Cycle Timing Diagram

AC ELECTRICAL SPECIFICATIONS — CHIP-SELECT TIMING INTERNAL MASTER (see Figure 17)

Num.	Characteristic	Symbol	16.67 MHz		Unit
			Min	Max	
150	Clock High to $\overline{CS}$, $\overline{IACK}$ Low (see Note 2)	$t_{CHCSIAKL}$	—	40	ns
151	Clock Low to $\overline{CS}$, $\overline{IACK}$ High (see Note 2)	$t_{CLCSIAKH}$	—	40	ns
152	$\overline{CS}$ Width Negated	t_{CSH}	60	—	ns
153	Clock High to $\overline{DTACK}$ Low (0 Wait State)	t_{CHDTKL}	—	45	ns
154	Clock Low to $\overline{DTACK}$ Low (1–6 Wait States)	t_{CLDTKL}	—	30	ns
155	Clock Low to $\overline{DTACK}$ High	t_{CLDTKH}	—	40	ns
156	Clock High to $\overline{BERR}$ Low (see Note 1)	t_{CHBERL}	—	40	ns
157	Clock Low to $\overline{BERR}$ High Impedance (see Note 1)	t_{CLBERH}	—	40	ns
158	$\overline{DTACK}$ High to $\overline{DTACK}$ High Impedance	$t_{DTKHDTKZ}$	—	15	ns
171	Input Data Hold Time from S6 Low	t_{IDHCL}	5	—	ns
172	$\overline{CS}$ Negated to Data Out Invalid (Write)	t_{CSNDOI}	10	—	ns
173	Address, FC Valid to $\overline{CS}$ Asserted	t_{AFVCSA}	15	—	ns
174	$\overline{CS}$ Negated to Address, FC Invalid	t_{CSNAFI}	15	—	ns
175	$\overline{CS}$ Low Time (0 Wait States)	t_{CSLT}	120	—	ns
176	$\overline{CS}$ Negated to R/$\overline{W}$ Invalid	t_{CSNRWI}	10	—	ns
177	$\overline{CS}$ Asserted to R/$\overline{W}$ Low (Write)	t_{CSARWL}	—	10	ns
178	$\overline{CS}$ Negated to Data In Invalid (Hold Time on Read)	t_{CSNDII}	0	—	ns

NOTE:

1. This specification is valid only when the ADCE or WPVE bits in the SCR are set.
2. For loading capacitance less than or equal to 50 pF, subtract 4 ns from the maximum value given.
3. Specs 172–178 do not have diagrams. However, similar diagrams for $\overline{AS}$ are shown as 25, 11, 13, 14, 17, 20A, and 29, respectively.

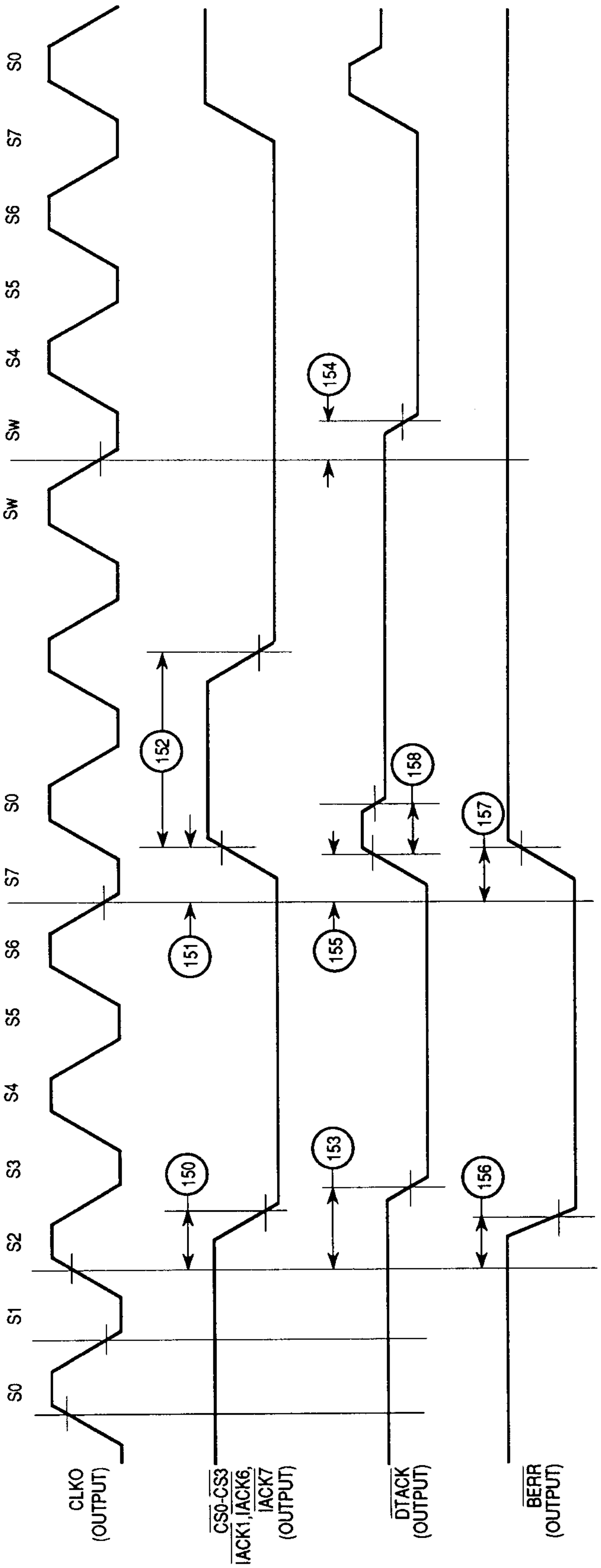


Figure 17. Internal Master Chip-Select Timing Diagram

AC ELECTRICAL SPECIFICATIONS — CHIP-SELECT TIMING EXTERNAL MASTER (see Figure 18)

Num.	Characteristic	Symbol	16.67 MHz		Unit
			Min	Max	
154	Clock Low to DTACK Low (1–6 Wait States)	t_{CLDTKL}	—	30	ns
160	AS Low to CS Low	t_{ASLCSL}	—	30	ns
161	AS High to CS High	t_{ASHCSH}	—	30	ns
162	Address Valid to AS Low	t_{AVASL}	15	—	ns
163	R/W Valid to AS Low (see Note 1)	t_{RWVASL}	15	—	ns
164	AS Negated to Address Hold Time	t_{ASHAI}	0	—	ns
165	AS Low to DTACK Low (0 Wait State)	$t_{ASLDTKL}$	—	45	ns
167	AS High to DTACK High	$t_{ASHDTKH}$	—	30	ns
168	AS Low to BERR Low (see Note 2)	$t_{ASLBERL}$	—	30	ns
169	AS High to BERR High (see Notes 2 and 3)	$t_{ASHBERH}$	—	30	ns

NOTE:
1. The minimum value must be met to guarantee write protection operation.
2. This specification is valid when the DCE or WPVE bits in the SCR are set.
3. Also applies after a timeout of the hardware watchdog.

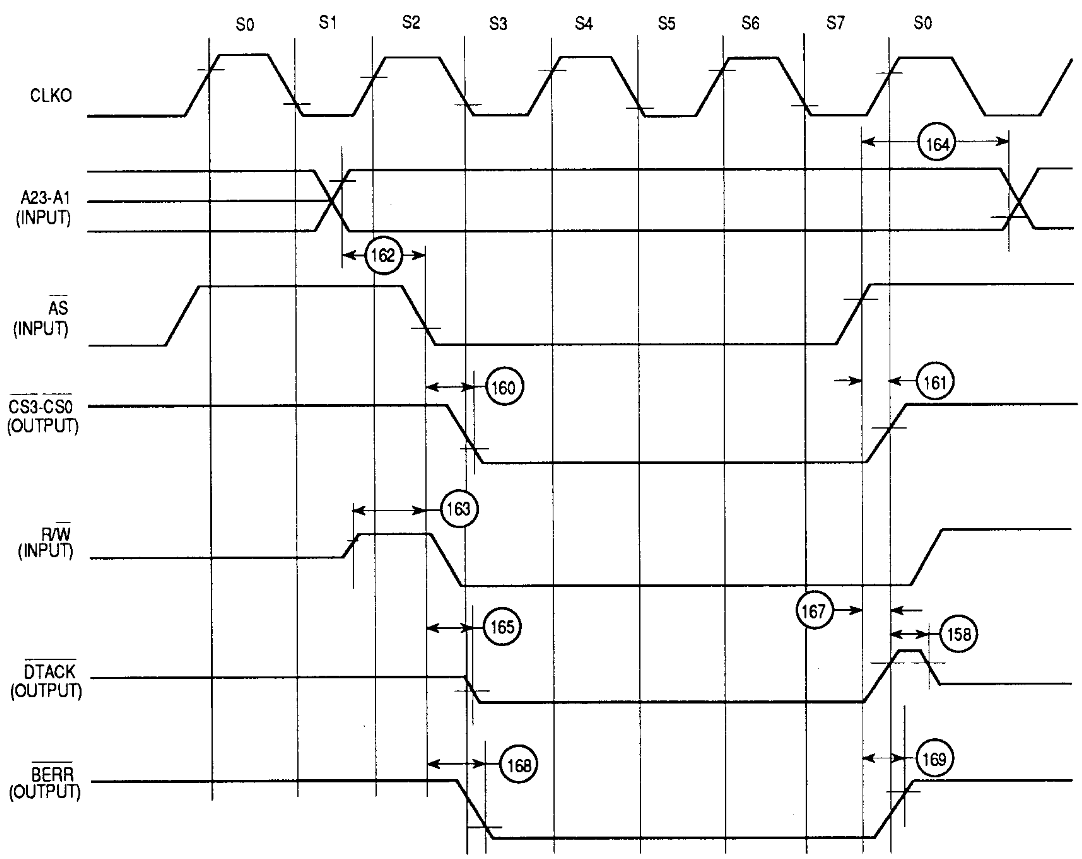


Figure 18. External Master Chip-Select Timing Diagram

AC ELECTRICAL SPECIFICATIONS — PARALLEL I/O

(see Figure 19)

Num.	Characteristic	Symbol	16.67 MHz		Unit
			Min	Max	
180	Input Data Setup Time (to Clock Low)	t_{DSU}	20	—	ns
181	Input Data Hold Time (from Clock Low)	t_{DH}	10	—	ns
182	Clock High to Data out Valid (CPU Writes Data, Control, or Direction)	t_{CHDOV}	—	35	ns

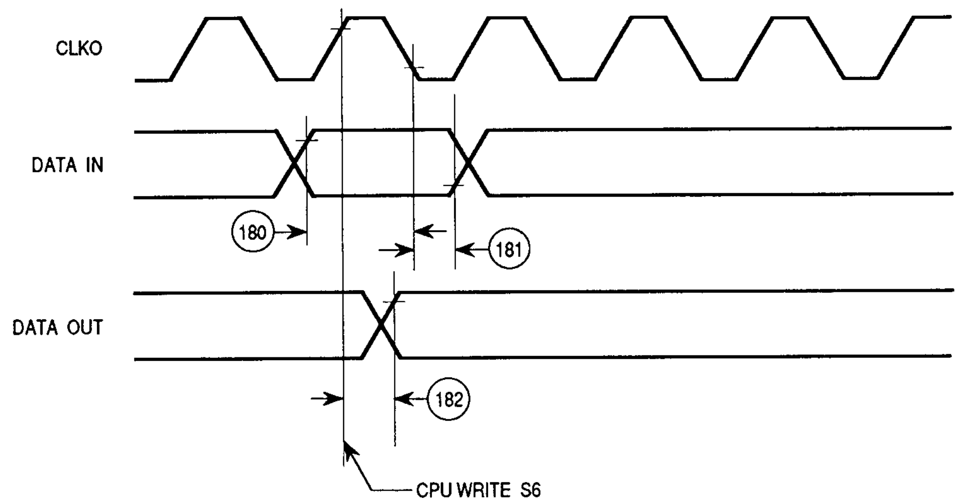


Figure 19. Parallel I/O Data In/Data Out Timing Diagram

AC ELECTRICAL SPECIFICATIONS — INTERRUPTS

(see Figure 20)

Num.	Characteristic	Symbol	16.67 MHz		Unit
			Min	Max	
190	Interrupt Pulse Width Low $\overline{IRQ}$ (Edge Triggered Mode)	t_{IPW}	50	—	ns
191	Minimum Time Between Active Edges	t_{AEMT}	3	—	clk

NOTE: Setup time for the asynchronous inputs IPL2–IPL0 and $\overline{AVEC}$ guarantees their recognition at the next falling edge of the clock.

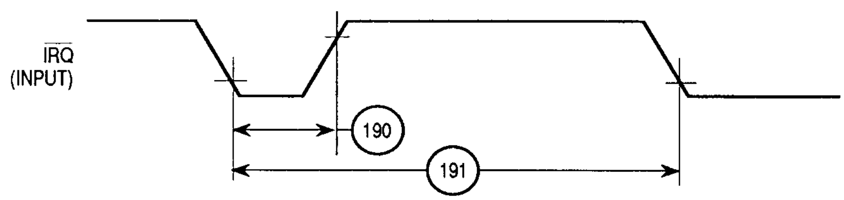


Figure 20. Interrupts Timing Diagram

AC ELECTRICAL SPECIFICATIONS — TIMERS

(see Figure 21)

Num.	Characteristic	Symbol	16.67 MHz		Unit
			Min	Max	
200	Timer Input Capture Pulse Width	t_{TPW}	50	—	ns
201	TIN Clock Low Pulse Width	t_{TICLT}	50	—	ns
202	TIN Clock High Pulse Width	t_{TICHT}	1.5	—	clk
203	TIN Clock Cycle Time	t_{cyc}	3	—	clk
204	Clock High to TOUT Valid	t_{CHTOV}	—	35	ns
205	$\overline{FRZ}$ Input Setup Time (to Clock High) (see Note)	t_{FRZSU}	20	—	ns
206	$\overline{FRZ}$ Input Hold Time (from Clock High)	t_{FRZHT}	10	—	ns

NOTE: $\overline{FRZ}$ should be negated during total system reset.

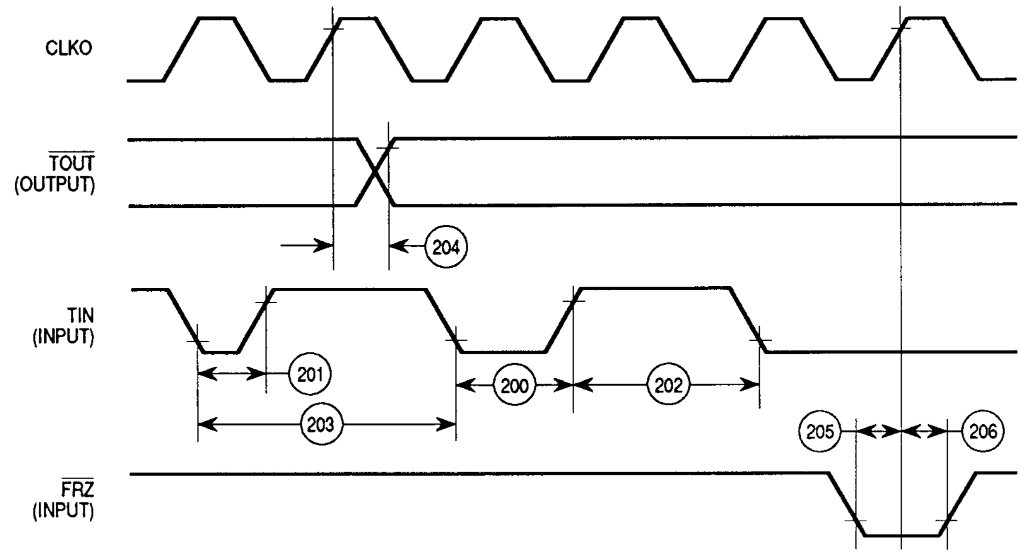


Figure 21. Timers Timing Diagram

AC ELECTRICAL SPECIFICATIONS — SERIAL COMMUNICATION PORT

(see Figure 22)

Num.	Characteristic	16.67 MHz		Unit
		Min	Max	
250	SPCLK Clock Output Period	4	64	clks
251	SPCLK Clock Output Rise/Fall Time	—	15	ns
252	Delay from SPCLK to Transmit (see Note 1)	0	40	ns
253	SCP Receive Setup Time (see Note 1)	40	—	ns
254	SCP Receive Hold Time (see Note 1)	10	—	ns

NOTES:
1. This also applies when SPCLK is inverted by CI in the SPMODE register.
2. The enable signals for the slaves may be implemented by the parallel I/O pins.

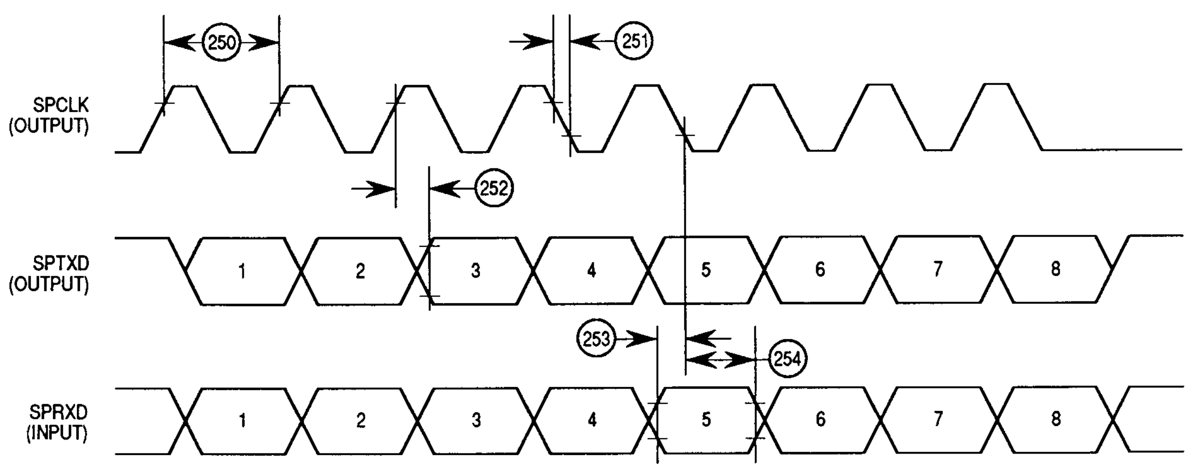


Figure 22. Serial Communication Port Timing Diagram

AC ELECTRICAL SPECIFICATIONS — IDL TIMING (All timing measurements, unless otherwise specified, are referenced to the L1CLK at 50% point of V_{DD}) (see Figure 23)

Num.	Characteristic	16.67 MHz		Unit
		Min	Max	
260	L1CLK (IDL Clock) Frequency (see Note 1)	—	6.66	MHz
261	L1CLK Width Low	55	—	ns
262	L1CLK Width High	55	—	ns
263	L1TXD, L1RQ, SDS1–SDS2 Rising/Falling Time	—	20	ns
264	L1SY1 (sync) Setup Time (to L1CLK Falling Edge)	30	—	ns
265	L1SY1 (sync) Hold Time (from L1CLK Falling Edge)	50	—	ns
266	L1SY1 (sync) Inactive Before 4th L1CLK	0	—	ns
267	L1TxD Active Delay (from L1CLK Rising Edge)	0	90	ns
268	L1TxD to High Impedance (from L1CLK Rising Edge) (see Note 2)	0	50	ns
269	L1RxD Setup Time (to L1CLK Falling Edge)	50	—	ns
270	L1RxD Hold Time (from L1CLK Falling Edge)	50	—	ns
271	Time Between Successive IDL syncs	20	—	L1CLK
272	L1RQ Valid before Falling Edge of L1SY1	1	—	L1CLK
273	L1GR Setup Time (to L1SY1 Falling Edge)	50	—	ns
274	L1GR Hold Time (from L1SY1 Falling Edge)	50	—	ns
275	SDS1–SDS2 Active Delay from L1CLK Rising Edge	10	90	ns
276	SDS1–SDS2 Inactive Delay from L1CLK Falling Edge	10	90	ns

NOTES:
1. The ratio CLK/L1CLK must be greater than 2.5/1.
2. High impedance is measured at the 30% and 70% of V_{DD} points, with the line at $V_{DD}/2$ through 10K in parallel with 130 pF.

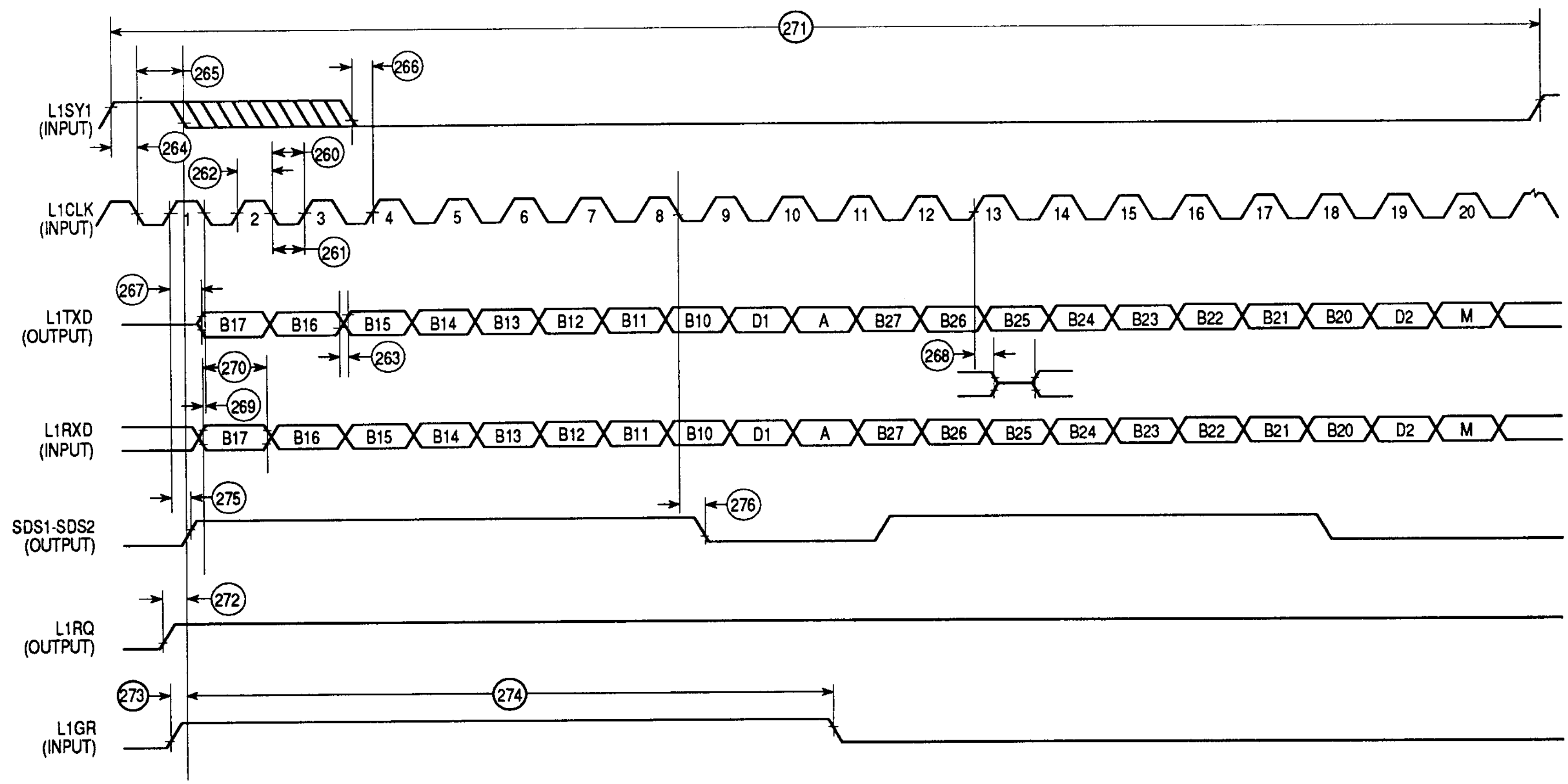


Figure 23. IDL Timing Diagram

AC ELECTRICAL SPECIFICATIONS — GCI TIMING

GCI supports the NORMAL mode and the GCI channel 0 (GCN0) in MUX mode.
Normal mode uses 512 kHz clock rate (256K bit rate).
MUX mode uses $256 \times n - 3088$ Kbits/sec (clock rate is data rate $\times$ 2).
The ratio CLK/L1CLK must be greater than 2.5/1.
(see Figure 24)

Num.	Characteristic	16.67 MHz Min	16.67 MHz Max	Unit
	L1CLK GCI Clock Frequency (Normal Mode) (see Note 1)	—	512	kHz
280	L1CLK Clock Period Normal Mode (see Note 1)	1800	2100	ns
281	L1CLK Width Low/High Normal Mode	840	1450	ns
282	L1CLK Rise/Fall Time Normal Mode (see Note 4)	—	—	ns
	L1CLK (GCI Clock) Period (MUX Mode) (see Note 1)	—	6.668	MHz
280	L1CLK Clock Period MUX Mode (see Note 1)	150	—	ns
281	L1CLK Width Low/High MUX Mode	55	—	ns
282	L1CLK Rise/Fall Time MUX Mode (see Note 4)	—	—	ns
283	L1SY1 Sync Setup Time to L1CLK Falling Edge	30	—	ns
284	L1SY1 Sync Hold Time from L1CLK Falling Edge	50	—	ns
285	L1TxD Active Delay (from L1CLK Rising Edge) (see Note 2)	0	100	ns
286	L1TxD Active Delay (from L1SY1 Rising Edge) (see Note 2)	0	100	ns
287	L1RxD Setup Time to L1CLK Rising Edge	20	—	ns
288	L1RxD Hold Time from L1CLK Rising Edge	50	—	ns
289	Time Between Successive L1SY1 in Normal Mode	64	—	L1CLK
	SCIT Mode	192	—	L1CLK
290	SDS1–SDS2 Active Delay from L1CLK Rising Edge (see Note 3)	10	90	ns
291	SDS1–SDS2 Active Delay from L1SY1 Rising Edge (see Note 3)	10	90	ns
292	SDS1–SDS2 Inactive Delay from L1CLK Falling Edge	10	90	ns
293	GCIDCL (GCI Data Clock) Active Delay	0	50	ns

NOTES:

1. The ratio CLK/L1CLK must be greater than 2.5/1.
2. Condition $C_L = 150$ pF
   L1TxD becomes valid after the L1CLK rising edge or L1SY1, whichever is later.
3. SDS1–SDS2 become valid after the L1CLK rising edge or L1SY1, whichever is later.
4. Schmitt trigger used on input buffer.

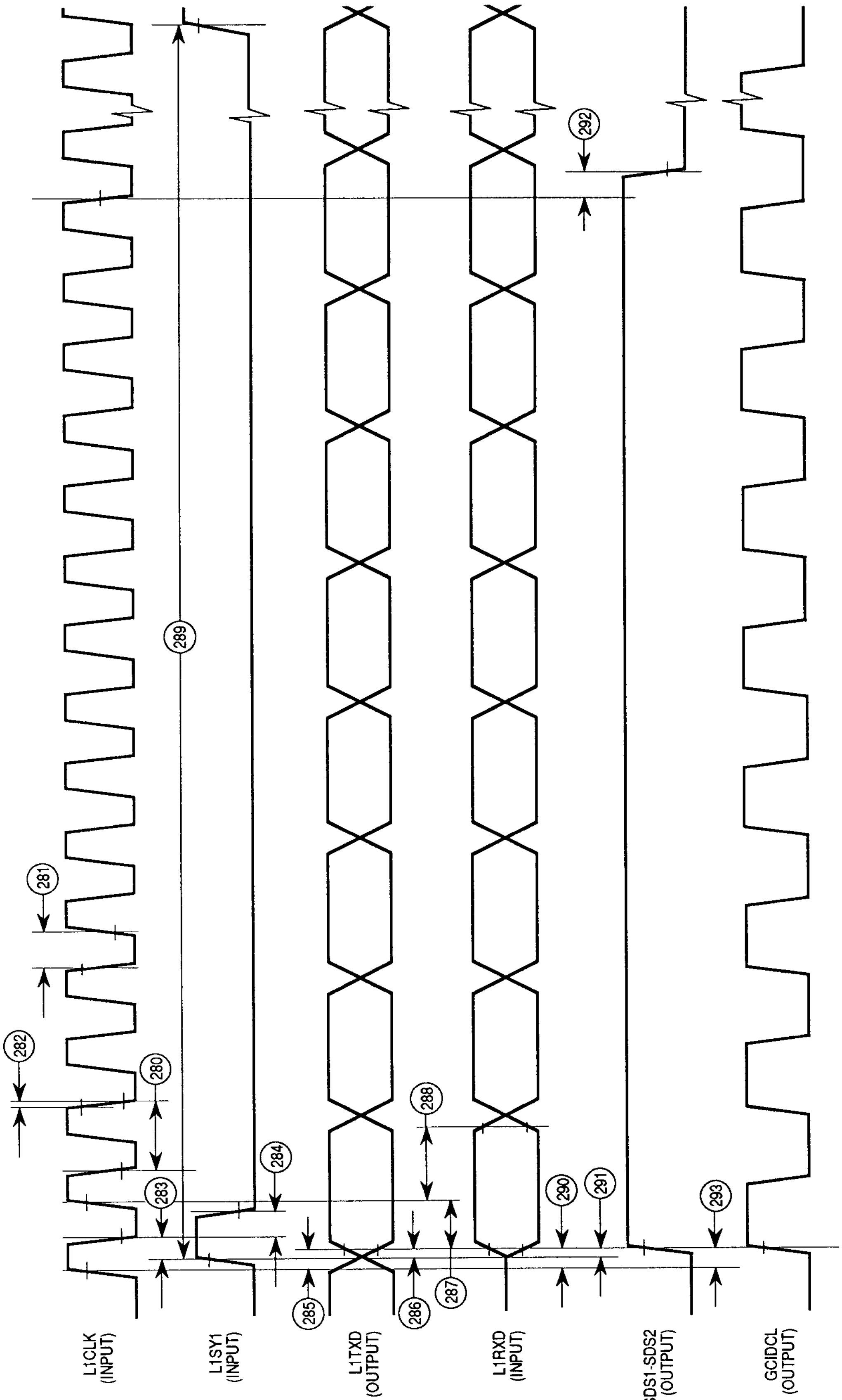


Figure 24. GCI Timing Diagram

AC ELECTRICAL SPECIFICATIONS — PCM TIMING

There are two syncs types:

Short Frame — Sync signals are one clock cycle prior to the data
Long Frame — Sync signals are N-bits that envelope the data, N>0
(see Figure 25)

Num.	Characteristic	16.67 MHz		Unit
		Min	Max	
300	L1CLK (PCM Clock) Frequency (see Note 1)	—	6.66	MHz
301	L1CLK Width Low/High	55	—	ns
302	L1SY0–L1SY1 Setup Time to L1CLK Falling Edge	20	—	ns
303	L1SY0–L1SY1 Hold Time from L1CLK Falling Edge	40	—	ns
304	L1SY0–L1SY1 Width Low	1	—	L1CLK
305	Time Between Successive Sync Signals (Short Frame)	8	—	L1CLK
306	L1TxD Data Valid after L1CLK Rising Edge (see Note 2)	0	100	ns
307	L1TxD to High Impedance (from L1CLK Rising Edge)	0	70	ns
308	L1RxD Setup Time (to L1CLK Falling Edge) (see Note 3)	20	—	ns
309	L1RxD Hold Time (from L1CLK Falling Edge) (see Note 3)	50	—	ns
310	L1TxD Data Valid After Syncs Rising Edge (Long) (see Note 2)	0	100	ns
311	L1TxD to High Impedance (from L1SY0–L1SY1 Falling Edge) (Long)	0	70	ns

NOTES:

1. The ratio CLK/L1CLK must be greater than 2.5/1.
2. L1TxD becomes valid after the L1CLK rising edge or the sync enable, whichever is later, if long frames are used.
3. Specification valid for both sync methods.

AC ELECTRICAL SPECIFICATIONS — NMSI TIMING

The NMSI mode uses two clocks, one for receive and one for transmit. Both clocks can be internal or external. When the clock is internal, it is generated by the internal Baud Rate Generator and it is output on L1RXD or L1TXD. All the timing is related to the external clock pin. The timing is specified for NMSI1. It is also valid for NMSI2 and NMSI3.
(see Figure 26)

Num.	Characteristic	Internal Clock		External Clock		Unit
		Min	Max	Min	Max	
315	RCLK1 and TCLK1 Frequency (see Note 1)	—	5.12	—	6.668	MHz
316	RCLK1 and TCLK1 Low/High	70	—	55	—	ns
317	RCLK1 and TCLK1 Rise/Fall Time (see Note 3)	—	—	—	—	ns
318	TxD1 Active Delay from TCLK1 Falling Edge	0	40	0	70	ns
319	$\overline{RTS1}$ Active/Inactive Delay from TCLK1 Falling Edge	0	40	0	100	ns
320	$\overline{CTS1}$ Setup Time to TCLK1 Rising Edge	50	—	10	—	ns
321	RXD1 Setup Time to RCLK1 Rising Edge	50	—	10	—	ns
322	RXD1 Hold Time from RCLK1 Rising Edge (see Note 2)	10	—	50	—	ns
323	$\overline{CD1}$ Setup Time to RCLK1 Rising Edge	50	—	10	—	ns

NOTE:

1. The ratio CLK/TCLK1 and CLK/RCLK1 must be greater than 2.5/1 for external clock.
   For internal clock the ratio must be greater than 3/1 (the input clock to the baud rate generator may be either CLK or TIN1), in both cases the maximum frequency is limited to 16.67 MHz.
   In asynchronous mode (UART), the bit rate is 1/16 of the clock rate.
2. Also applies to $\overline{CD}$ hold time when $\overline{CD}$ is used as an external sync in BISYNC or totally transparent mode.
3. Schmitt triggers used on input buffers.

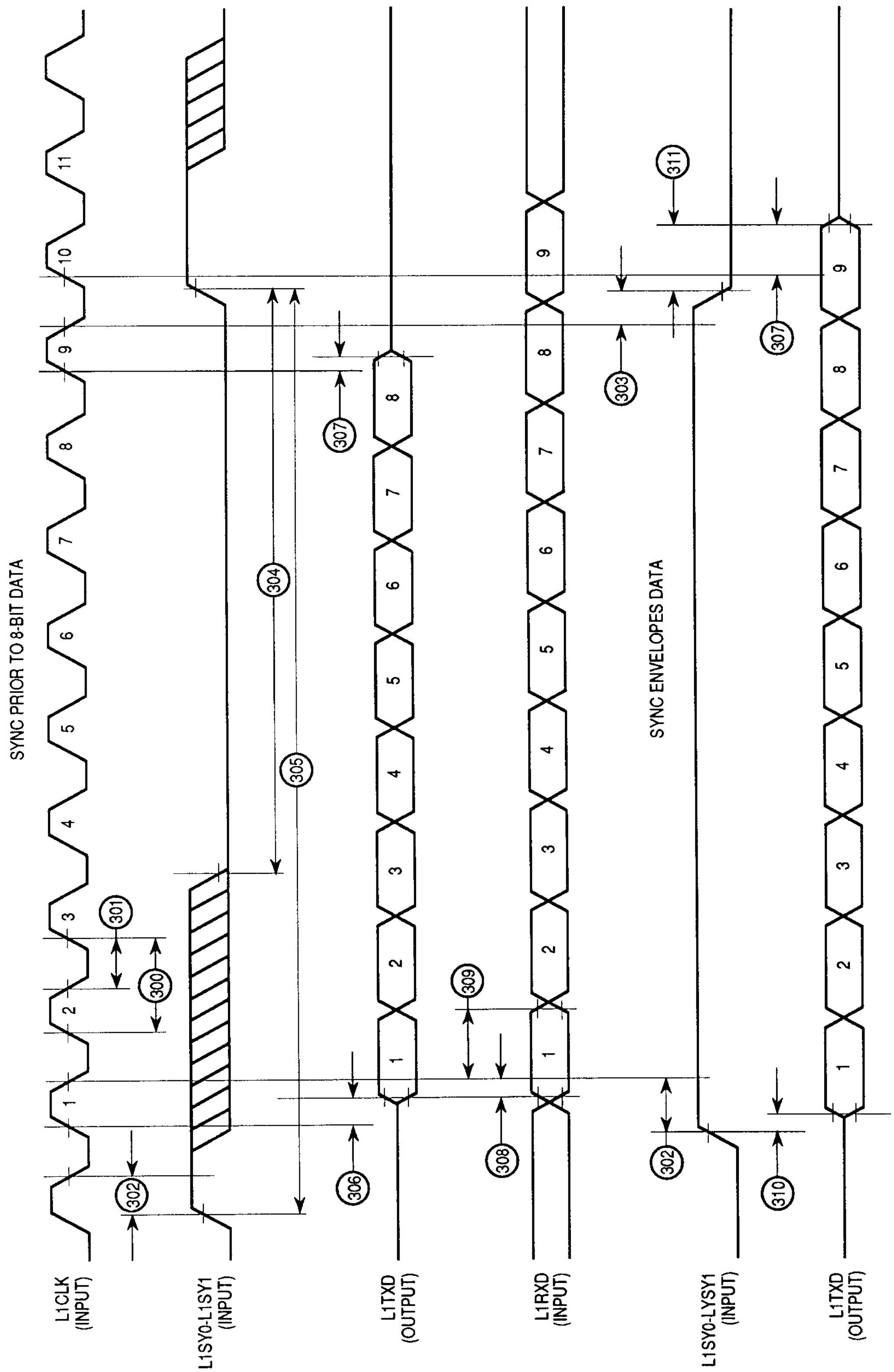


Figure 25. PCM Timing Diagram

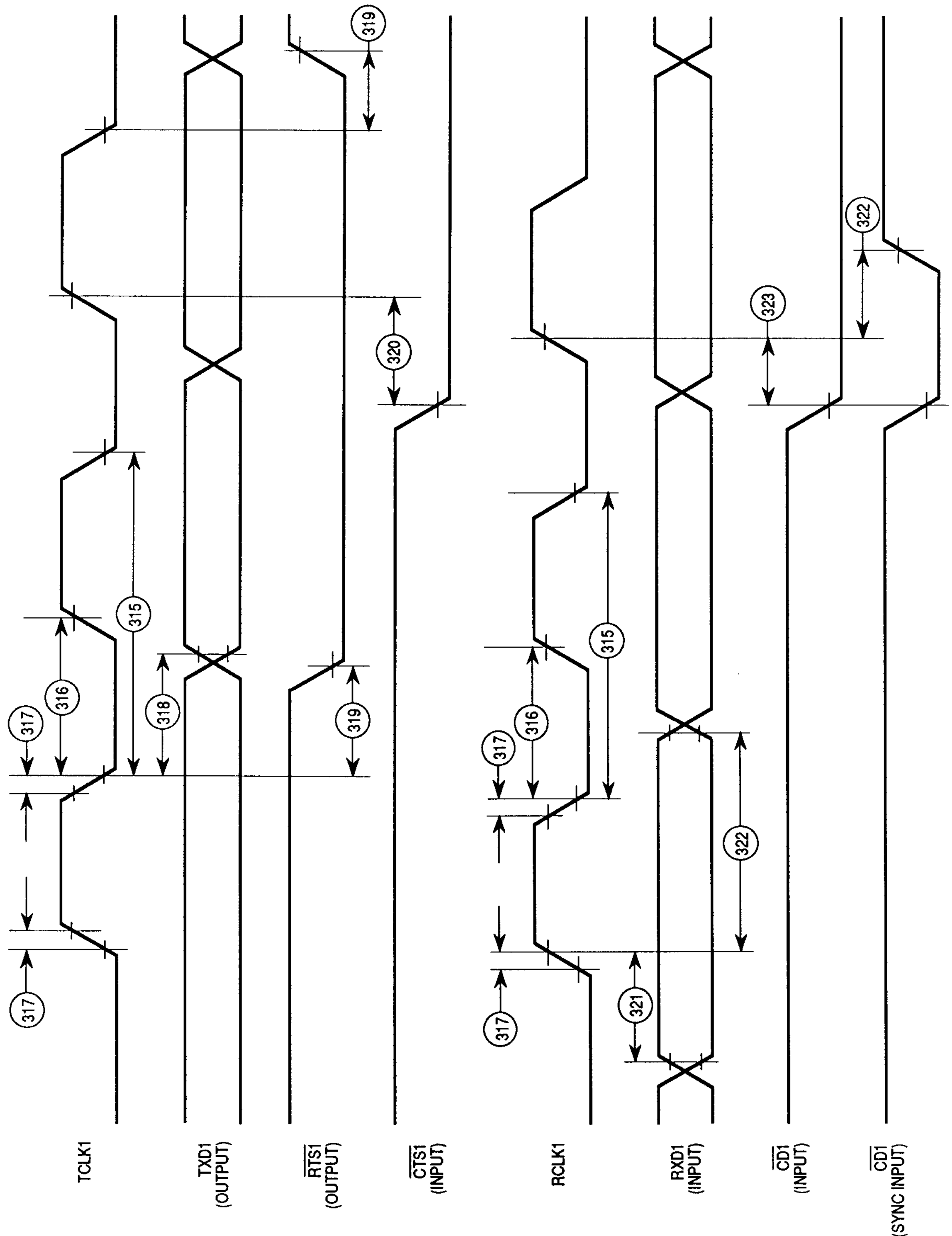


Figure 26. NMSI Timing Diagram

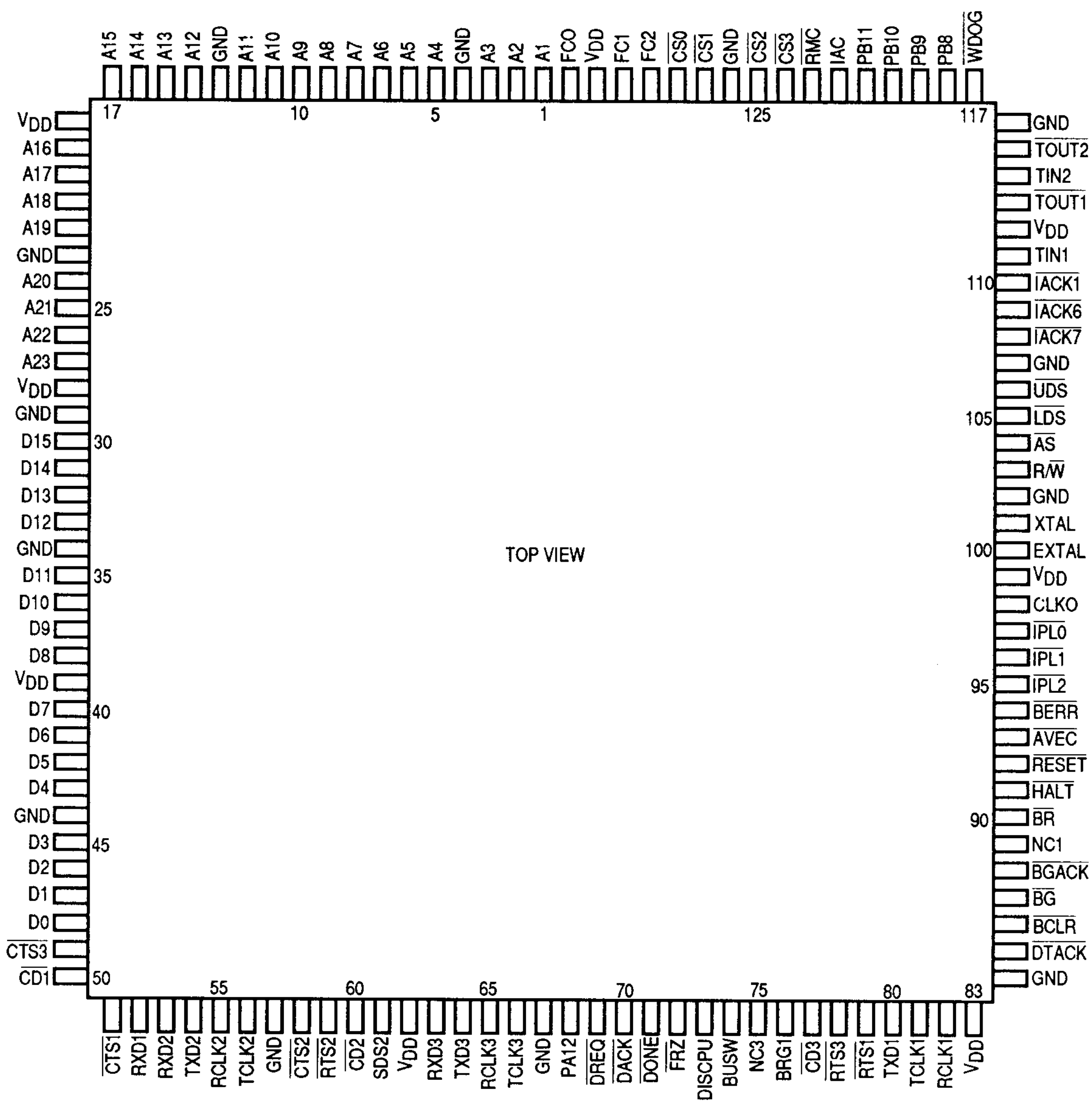
MECHANICAL DATA

PIN ASSIGNMENTS

Pin Grid Array

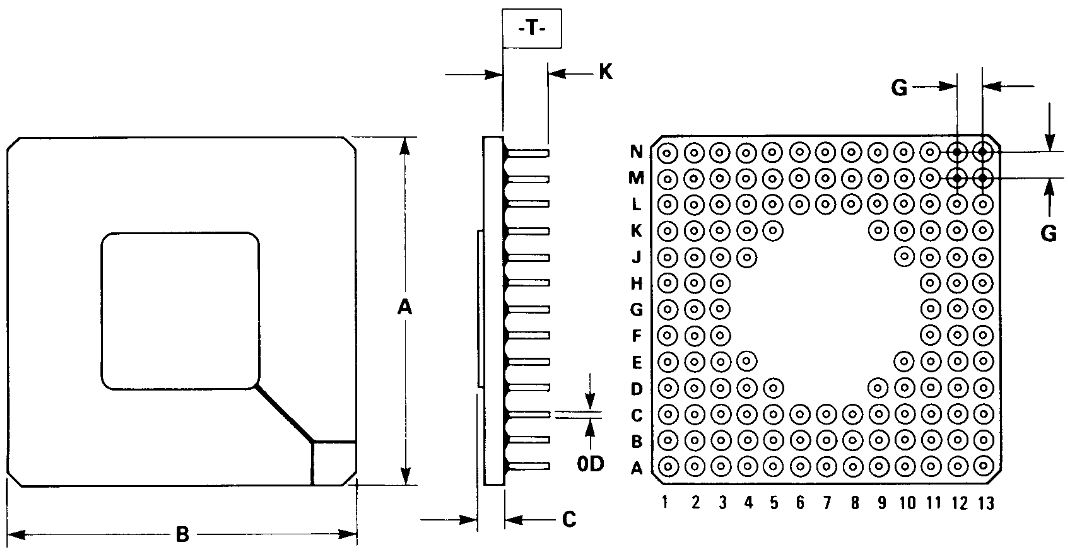
	1	2	3	4	5	6	7	8	9	10	11	12	13
N	PB10	TIN1	IACK1	GND	UDS	R/W	EXTAL	V_{DD}	IPL1	IPL2	RESET	HALT	RCLK1
M	CS3	TOUT2	TIN2	V_{DD}	IACK7	AS	GND	CLKO	BERR	BR	BGACK	BG	RTS3
L	CS2	PB11	GND	TOUT1	IACK6	LDS	XTAL	IPL0	AVEC	NC1	BCLR	TCLK1	CD3
K	CS0	RMC	IAC	PB9	WDOG				DTACK	V_{DD}	TXD1	RTS1	BUSW
J	FC2	CS1	GND	PB8						GND	BRG1	NC3	DISCPU
H	FC0	V_{DD}	FC1								FRZ	DONE	DACK
G	A1	A3	A2				BOTTOM VIEW				PA12	DREQ	GND
F	GND	A4	A5								TXD3	RCLK3	TCLK3
E	A6	A8	A9	V_{DD}						TXD2	CD2	SDS2	RXD3
D	A7	GND	A12	A15	A16				RXD2	CTS1	TCLK2	GND	V_{DD}
C	A10	A13	A17	GND	A23	D14	D11	V_{DD}	D4	D1	CD1	RCLK2	RTS2
B	A11	A18	A19	A20	V_{DD}	D13	D10	D8	D5	D2	D0	CTS3	CTS2
A	A14	A21	A22	GND	D15	D12	GND	D9	D7	D6	GND	D3	RXD1

Ceramic Surface Mount (CQFP)



PACKAGE DIMENSIONS

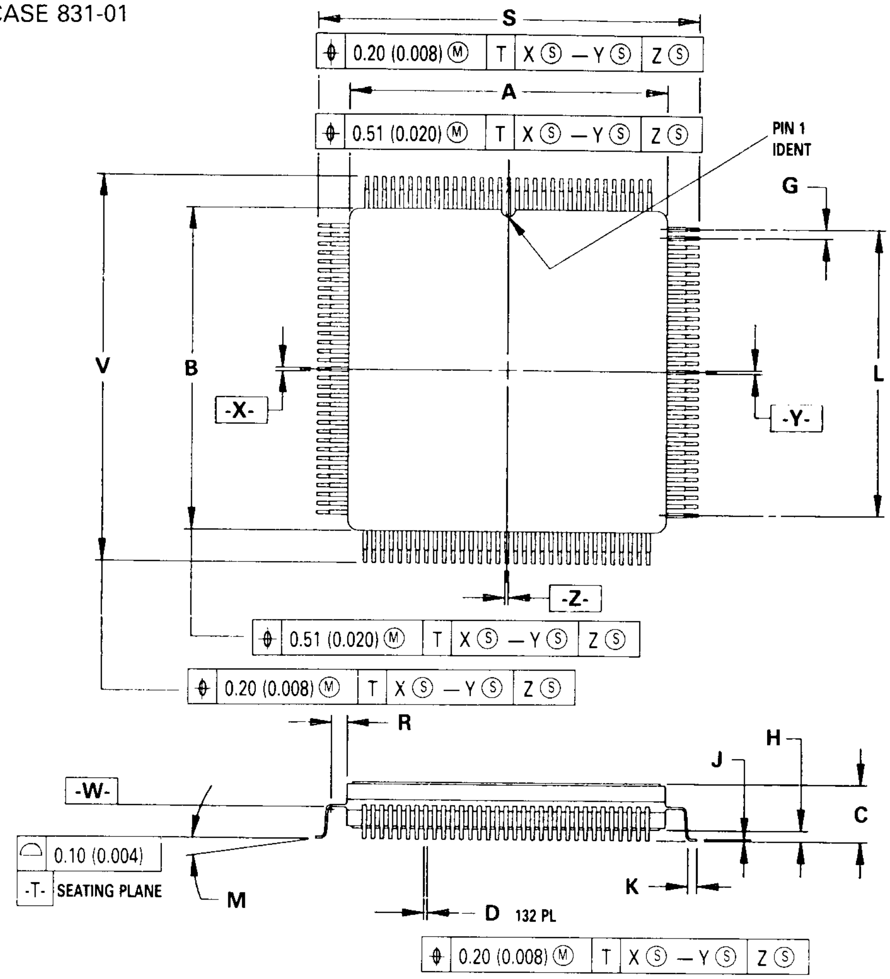
RC SUFFIX
PIN GRID ARRAY
CASE 789B-01



NOTES:
1. A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR LEADS (132 PL).
   | ⌖ | ϕ 0.13 (0.005) Ⓜ | T | A Ⓢ | B Ⓢ |
3. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	34.04	35.05	1.340	1.380
B	34.04	35.05	1.340	1.380
C	2.54	3.81	0.100	0.150
D	0.43	0.55	0.017	0.022
G	2.54 BSC		0.100 BSC	
K	4.32	4.95	0.170	0.195

FE SUFFIX
CERAMIC SURFACE MOUNT
CASE 831-01



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	21.85	22.86	0.860	0.900
B	21.85	22.86	0.860	0.900
C	3.94	4.31	0.155	0.170
D	0.204	0.292	0.0080	0.0115
G	0.64 BSC		0.025 BSC	
H	0.64	0.88	0.025	0.035
J	0.13	0.20	0.005	0.008
K	0.51	0.76	0.020	0.030
L	20.32 REF		0.800 REF	
M	0°	8°	0°	8°
R	0.64	—	0.025	—
S	27.31	27.55	1.075	1.085
V	27.31	27.55	1.075	1.085

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM A AND B DEFINE MAXIMUM CERAMIC BODY DIMENSIONS INCLUDING GLASS PROTRUSION AND MISMATCH OF CERAMIC BODY TOP AND BOTTOM.
4. DATUM PLANE -W- IS LOCATED AT THE UNDERSIDE OF LEADS WHERE LEADS EXIT PACKAGE BODY.
5. DATUMS X-Y AND Z TO BE DETERMINED WHERE CENTER LEADS EXIT PACKAGE BODY AT DATUM -W-.
6. DIM S AND V TO BE DETERMINED AT SEATING PLANE, DATUM -T-.
7. DIM A AND B TO BE DETERMINED AT DATUM PLANE -W-.

ORDERING INFORMATION

Package Type	Frequency (MHz)	Temperature	Order Number
Pin Grid Array RC Suffix	16.67 16.67	0°C to 70°C 0°C to 85°C	MC68302RC16 MC68302IRC16
Ceramic Surface Mount FE Suffix	16.67 16.67	0°C to 70°C 0°C to 85°C	MC68302FE16 MC68302IFE16

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