M402101BP

4×8 CROSSPOINT SWITCH WITH CONTROL MEMORY

DESCRIPTION

The M402101B is a semiconductor integrated circuit consisting of a 4×8 cross point switch capable of selecting 32 analog switches with 5 address inputs as well as 2 types of control signals.

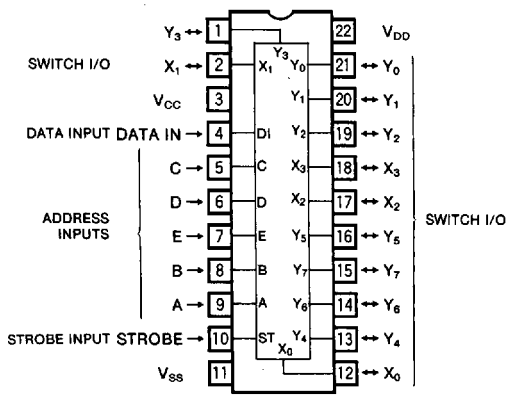
FEATURES

- Internal control latch circuit
- Internal level- shifter circuit
- Good crosstalk characteristics −100dB (@f=3kHz)
- Low on-state resistance 60Ω typical (@V_{DD}=15V)
- High off-state resistance more than $10^9\Omega$ typ.
- Excellent transfer linearity Distortion 0.05% typ. (@R_L=1kΩ, V_{DD}=5V, V_{SS}=−5V)
- 5V control logic

APPLICATION

Line switching of telephone and communication equipments.

PIN CONFIGURATION (TOP VIEW)

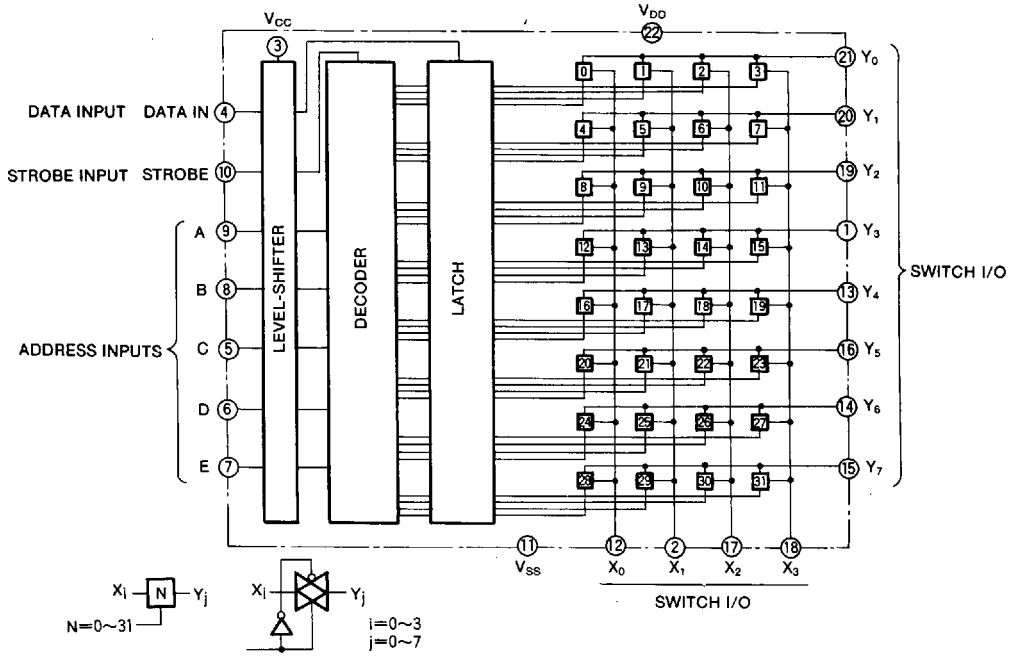


Outline 22P4H

FUNCTIONAL DESCRIPTION

The input address signals (A, B, C, D, E) are five-bit binary coded. When the STROBE input is high, the switch that corresponds to the value of the input address signals is selected. If, at this time, the DATA IN input is high, the switch is turned on and until DATA IN is pulled low. If the DATA IN is low, the switch is turned off and becomes in high-impedance state. When the STROBE becomes low, any of the switch conditions are not changed. The internal level-shifter makes possible to handle $15V_{p-p}$ analog signals by 5V control logic signals.

LOGIC DIAGRAM



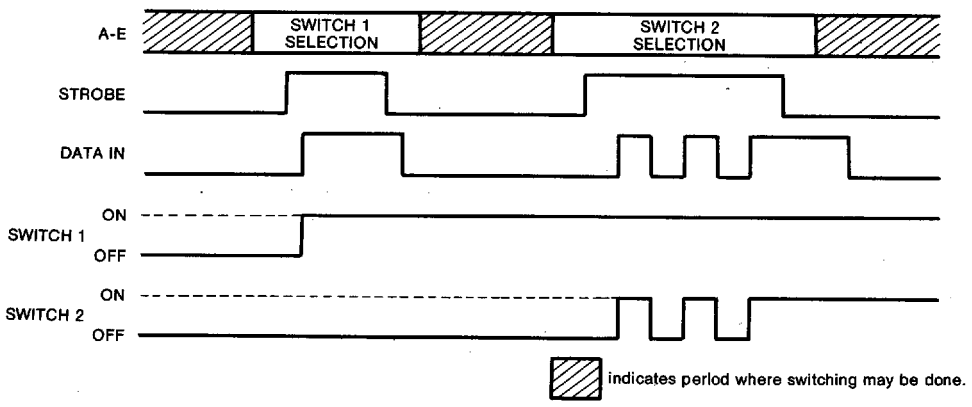
4×8 CROSSPOINT SWITCH WITH CONTROL MEMORY

FUNCTION TABLE (Note : 1)

		0	1	2	3	4	5	6	7	8	···	30	31
Control input	A	X	L L H H L L H H L L H H L L H H L L ··· L L H H										
	B	X	L L L L H H H H L L L L H H H H L L ··· H H H H										
	C	X	L L L L L L L L H H H H H H H H L L ··· H H H H										
	D	X	L L L L L L L L L L L L L L L L H H ··· H H H H										
	E	X	L L L L L L L L L L L L L L L L L L ··· H H H H										
	STROBE	L	H H H H H H H H H H H H H H H H H H ··· H H H H										
	DATA IN	X	L H L H L H L H L H L H L H L H L H ··· L H L H										
	0 X0Y0	NC	OFF ON ← NC										
	1 X1Y0	NC	→ OFF ON ← NC										
	2 X2Y0	NC	→ OFF ON ← NC										
	3 X3Y0	NC	→ OFF ON ← NC										
	4 X0Y1	NC	→ OFF ON ← NC										
	5 X1Y1	NC	→ OFF ON ← NC										
	6 X2Y1	NC	→ OFF ON ← NC										
	7 X3Y1	NC	→ OFF ON ← NC										
	8 X0Y2	NC	→ OFF ON ← NC										
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	30 X2Y7	NC	→ OFF ON ← NC										
	31 X3Y7	NC	→ OFF ON										

Note 1 : X : Irrelevant
ON : Low impedance between X_i—Y_j(i=0~3, j=0~7)
OFF : High impedance between X_i—Y_j(i=0~3, j=0~7)
NC : No change and previous state is maintained.

OPERATING TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=−40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage 1		−0.5∼20	V
V_{CC}	Supply voltage 2		−0.5∼20	V
$V_{DD}-V_{CC}$	Supply voltage 1−supply voltage 2		−0.5∼20	V
V_I	Input voltage	A∼E, STROBE, DATA IN	V_{SS}−0.5∼V_{DD}+0.5	V
V_I	Input voltage	X_0∼X_3, Y_0∼Y_7	V_{SS}−0.5∼V_{DD}+0.5	V
$V_{I/O}$	On-state voltage diffrence between input and output	X_0∼X_3, Y_0∼Y_7	+0.5	V
V_O	Output voltage	X_0∼X_3, Y_0∼Y_7	−0.5∼V_{CC}+0.5	V
I_I	Input current	A∼E, STROBE, DATA IN	±10	mA
$I_{I/O}$	Input Output current	X_0∼X_3/Y_0∼Y_7 (Switch off)	±10	mA
Tstg	Storage temperature		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{DD}	Supply voltage 1	V_{CC}	15	18	V
V_{CC}	Supply voltage 2	4.5	5	5.5	V
V_I	Input voltage (A∼E, STROBE, DATA IN)	V_{SS}		V_{CC}	V
V_I	Input voltage (X_0∼X_3, Y_0∼Y_7)	V_{SS}		V_{DD}	V
V_O	Output voltage (X_0∼X_3, Y_0∼Y_7)	V_{SS}		V_{DD}	V
T_{opr}	Operating free air temperature range	−40		+85	℃

ELECTRICAL CHARACTERISTICS (V_{CC}=5V)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{DD}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage (A∼E, STROBE, DATA IN)	Switch on R_{ON}<$R_{ON\ MAX}$ Switch off I_L<0.2μA V_{CC}=5V	5	4.0			4.0		V
			10	3.5			3.5		
			15	3.5			3.5		
V_{IL}	Low-level input voltage (A∼E, STROBE, DATA IN)		5			1.5		1.5	V
			10			1.5		1.5	
			15			1.5		1.5	
R_{ON}	On-resistance (Test circuit 1)	$V_I=\frac{V_{DD}-V_{SS}}{2}$	5		170	650		820	Ω
			10		75	150		185	
			15		60	100		130	
ΔR_{ON}	On-resistance difference (between 2 switches of the 32 switches)	$V_I=\frac{V_{DD}-V_{SS}}{2}$	5		16				Ω
			10		17				
			15		17				
I_O	Output off-leak current	Switch off	18			±0.3		±1.0	μA
I_{DD}	Quiescent supply current (per package)	V_I=V_{DD}, V_{SS}	5			10		150	μA
			10			20		300	
			15			40		600	
		V_I=3.5, 1.5V(Note 2)	15		2.2				
I_{IH}	High-level input current (A∼E, ST, DI)	V_{CC}=6V V_{IH}=6V	18			0.3		1.0	μA
I_{IL}	High-level input voltage (A∼E, ST, DI)	V_{CC}=6V V_{IL}=0V	18			−0.3		−1.0	μA

Note 2 : Only one input is set to this value and all other inputs are tied to V_{CC} or GND.

SWITCHING CHARACTERISTICS (V_{CC}=5V)

Symbol	Parameter	Test conditions	V_{SS}(V)	V_{DD}(V)	Limits Min	Limits Typ	Limits Max	Unit
f_{max}(I/O)	Maximum frequency	R_L=1kΩ Test circuit 2	−5	5		50		MHz
f_{max}	Maximum control frequency	R_L=1kΩ C_L=50pF Test circuit 3	0 0 0	5 10 15	0.6 1.6 2.5	5 10 11		MHz
t_{PLH}	Low- to high-level and high- to low-level output propagation time (Xn/Yn−Yn/Xn)	R_L=10kΩ C_L=50pF Test circuit 4	0 0 0	5 10 15		15 7 6	60 30 20	ns
t_{PHL}			0 0 0	5 10 15		10 6 5	60 30 20	ns
t_{PHZ}	High-level output disable time (STROBE−Yn/Xn)	R_L=1kΩ C_L=50pF Test circuit 5	0 0 0	5 10 15		200 115 100	530 370 340	ns
t_{PZH}	High-level output enable time (STROBE−Yn/Xn)		0 0 0	5 10 15		180 95 80	800 450 360	ns
t_{PZH}	High-level, low-level output enable time (DATA IN−Yn/Xn)	R_L=1kΩ C_L=50pF Test circuit 6	0 0 0	5 10 15		125 80 70	620 440 400	ns
t_{PZL}			0 0 0	5 10 15		130 80 70	620 440 400	ns
t_{PHZ}	High-level output disable time (A~E−Yn/Xn)	R_L=1kΩ C_L=50pF Test circuit 7	0 0 0	5 10 15		140 80 75	1070 720 520	ns
t_{PZH}	High-level output enable time (A~E−Yn/Xn)		0 0 0	5 10 15		125 65 60	900 470 380	ns
—	Sinewave distortion	R_L=1kΩ f_i=1kHz Test circuit 2	−5	5		0.05		%
—	Feedthrough (switch off)	R_L=1kΩ Test circuit 8	−5	5		−80		dB
—	Crosstalk	R_L=10kΩ Test circuit 9	0	(Note: 5) 10		150		mV
—	Crosstalk frequency	R_L=1kΩ (Note : 3) SW(A)=on, SW(B)=off Test circuit 10 (Note : 4)	−5 −5	5 5		1.5 0.1		MHz kHz
C_I	Input capacitance	A~E, STROBE, DATA IN, RESET				5	7.5	pF
		Signal input Xn				75		pF
		Signal input Yn				48		pF
CX_n/Y_n	Input/output capacitance					0.6		pF

Note 3 : $20 \cdot \log\frac{V_O(B)}{V_I(A)} = -40dB$, Note 4 : $20 \cdot \log\frac{V_O(B)}{V_I(A)} = -110dB$, Note 5 : V_{CC}=10V

TIMING REQUIREMENT (V_{CC}=5V, V_{SS}=0V)

Symbol	Parameter	Test conditions	V_{DD}(V)	Limits Min	Limits Typ	Limits Max	Unit
$t_{w(ST)}$	Strobe pulse width		5 10 15	600 240 190	135 60 45		ns
t_{SU}	Data setup time before A~E, STROBE		5 10 15	280 140 120	70 35 25		ns
t_h	Data hold time after A~E, STROBE		5 10 15	420 280 180	60 35 25		ns

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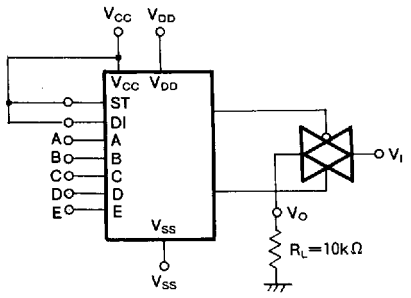
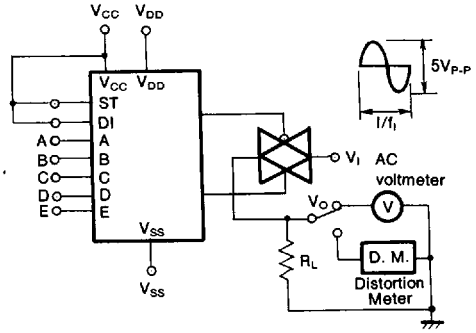
1 On-state resistance (R_{ON})



$$R_{ON}=10\times\frac{(V_I-V_O)}{V_O}[k\Omega]$$

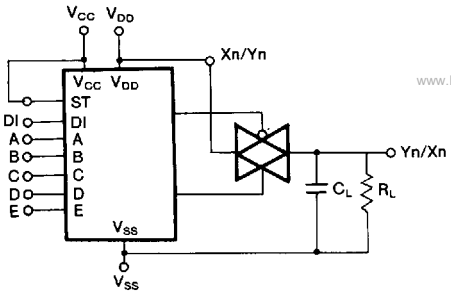
*Only one switch is on.
See function table for conditions of address inputs A through E.

2 Maximum frequency (f_{max}(I/O)) sinewave distortion

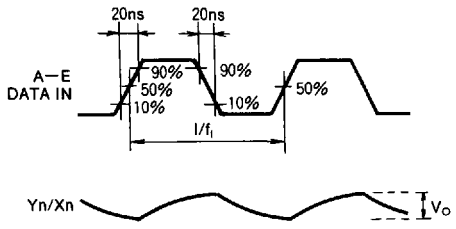


With an input sinewave of +2.5V_{P-P}, f_{max}(I/O) is equal to frequency (f_1) when $20\cdot\log_{10} V_O/V_1=-3dB$.
See function table for conditions of address inputs A through E.

3 Maximum control frequency ($f_{max}(C_{IN})$)

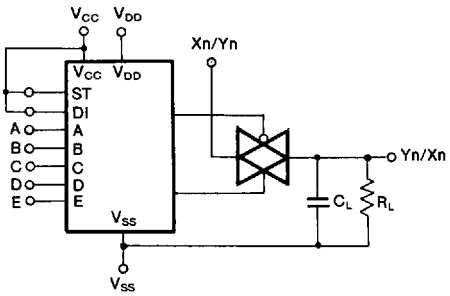


Timing diagram

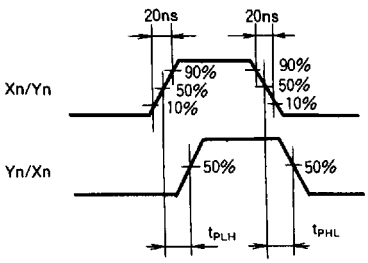


$f_{max}(C_{IN})$ is the value of f_1 when output amplitude reaches half the value of its original value at the time the input frequency $f_1=1kHz$.
See function table for conditions of address inputs A through E.

4 Low- to high-level and high- to low-level output propagation time (Xn/Yn–Yn/Xn)

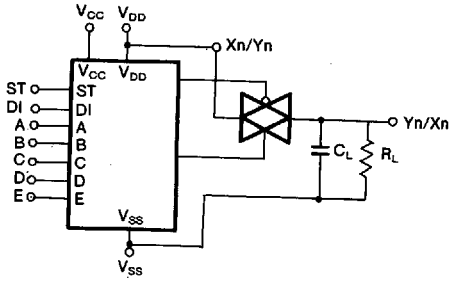


Timing diagram

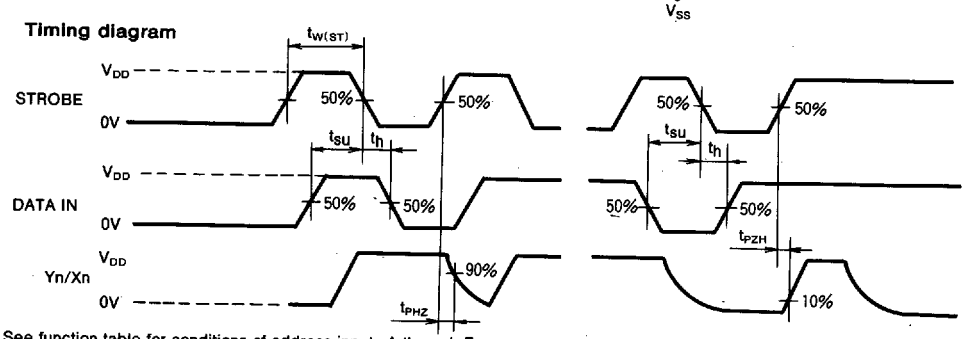


See function table for conditions of address inputs A through E.

5 High-level output disable/enable time (STROBE—Yn/Xn)

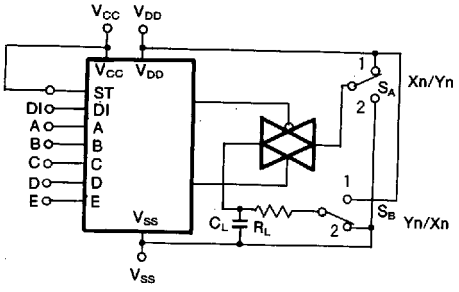


Timing diagram



See function table for conditions of address inputs A through E.

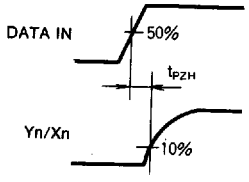
6 High-level, low-level enable time (DATA IN—Yn/Xn)



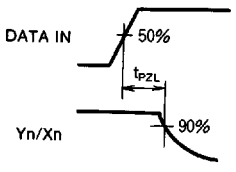
See function table for conditions of address inputs A through E.

Timing diagram

$S_A = 1$, $S_B = 2$



$S_A = 2$, $S_B = 1$



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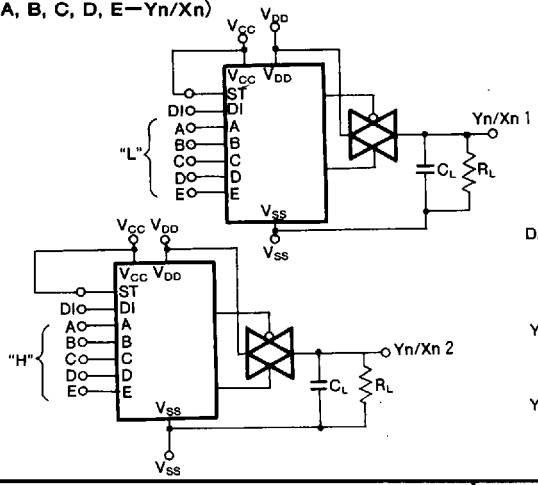
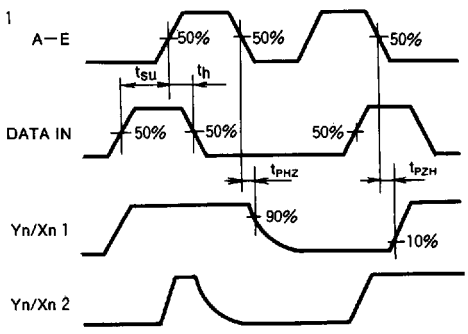
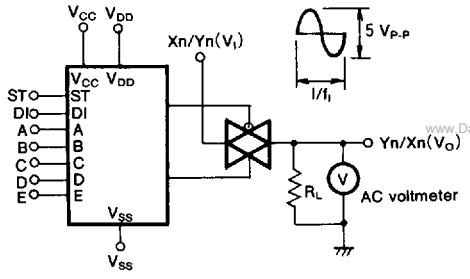
7 High-level output disable/enable time (A, B, C, D, E—Yn/Xn)



Timing diagram

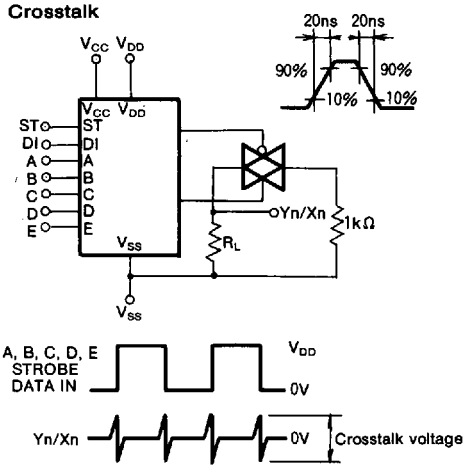


8 Feedthrough

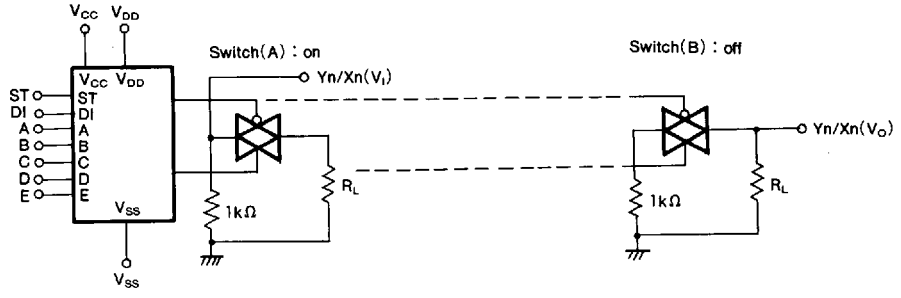


Using a $+2.5V_{P-P}$ sinewave input, feedthrough is $20 \cdot \log_{10} V_O/V_I$ when $f_I = 1.6kHz$. See function table for conditions of strobe, data-in and address inputs A through E.

9 Crosstalk



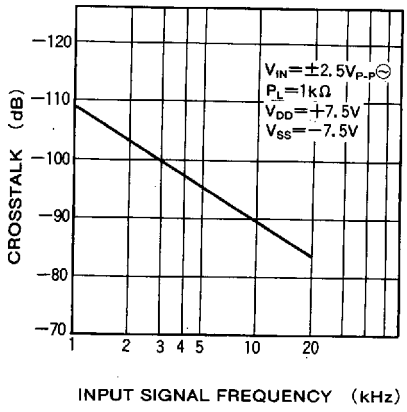
10 Crosstalk frequency



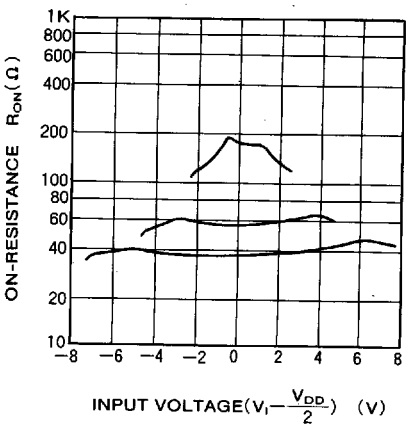
Using a $+2.5V_{P-P}$ sinewave input, cross talk frequency is to be measured as the frequency where $20 \cdot \log_{10} V_O/V_I$ equals $-40dB$ and $-110dB$. See function table for conditions of strobe data-in and A through E.

TYPICAL CHARACTERISTICS

CROSSTALK—INPUT SIGNAL FREQUENCY



R_{ON}—INPUT VOLTAGE ($V_I-\frac{V_{DD}}{2}$)



FREQUENCY RESPONSE