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Designing an IEEE 802.3 10BASE-FL Transceiver

INTRODUCTION

The ML4662 10BASE-FL Transceiver with the ML4621/ ML4622/ML4624 fiber optic quantizer construct both an internal and external 10BASE-FL MAU (Media Attachment Unit) described in the IEEE 802.3 standard. The ML4662 through its standard 802.3 AU (Attachment Unit) interface can be connected to an AUI cable, Ethernet Manchester Encoder/Decoder or Hub controller. The following topics will be discussed in this Application Note:

1) ML4662 Features
2) ML4621/ML4622/ML4624 (ML462X) Features
3) Filtering Power & Ground
4) Attachment Unit Interface
5) Interfacing ML4662 to National DP83950 Repeater Interface Controller
6) Interfacing ML4662 to AMD 79C980 Repeater
7) Interfacing ML4662 to AT&T T7202 Multi-Port Repeater
8) 10BASE-FL System Specification
9) Layout Considerations
10) Initial debug of the 10BASE-FL board

ML4662 FEATURES

The ML4662 integrates many of the functions needed for a 10BASE-FL transceiver. The Attachment Unit Interface complies with the IEEE standard offering Transmit, Receive, and Collision pair signals. Data transmission includes transmit squelch, a 1MHz idle signal, and the jabber function. The receiver accepts ECL compatible levels from the ML462X quantizer, passing through the receive squelch and into the AUI. The complete 10BASE-FL state machine is also incorporated including collision detect, loopback, and low light conditions.

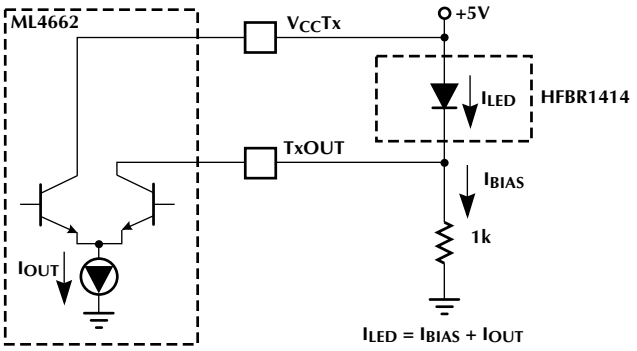


Figure 1.

One of the features is the capability to disable or enable the SQE function. This allows a 10BASE-FL transceiver to be connected to a DTE as well as a repeater. When connecting to a DTE, SQE must be enabled. When connecting to a repeater, SQE is disabled.

The ML4662 transmitter consists of a current driver output (TxOUT) which directly drives an HP fiber optic LED transmitter (HFBR1414). The output current is switched through the TxOUT pin during the on cycle and the V_{CC}Tx pin during the off cycle as shown in figure 1. Since the sum of the current in these two pins is constant, V_{CC}Tx should be connected as close as possible to the V_{CC} connection for the LED.

The 1KΩ pulldown resistor on the TxOUT pin prebiases the LED by applying a small forward current while the LED is in the "off" or low light state. The prebias current prevents the junction and parasitic capacitances from discharging completely when the LED is in the "off" state, thus reducing the amount of charge that the driver must transfer to turn the diode back on.

The resistor on the RTSET pin controls the amount of current driven by this pin (TxOUT). RTSET and the pulldown resistor together set the extinction ratio. To calculate RTSET value for a certain sink current (maximum 74mA) at TxOUT use this equation:

$$RTSET = (52mA/I_{OUT})\ 162\Omega$$

The ML4662 Transmitter has been designed to drive the cathode of the LED (note: higher optical power transmitted corresponds to the low logic state). Current flowing through the LED corresponds to a logic low. When Tx– > Tx+ (DO on AUI), current flows and this will be a logic low. When Tx+ > Tx– (DO on AUI), no current flows (except bias) corresponding to a logic high.

The receiver inputs are ECL levels (the ML4662 receiver inputs) coming from the ML462X. When $LMON_{IN}$ (TTL) coming from the ML462X is low, and the level of the received signal exceeds the receive squelch requirement, the receive data is buffered and transmitted out to DI pair.

The five LED status outputs are active low, open collector outputs. They provide a visible status of the link as follows:

$\overline{\textbf{XMT}}$: is on when transmission is taking place.

$\overline{\textbf{RCV}}$: is on when the transceiver is receiving a frame from the ML462X (V_{IN}+ and V_{IN}–).

$\overline{\text{CLSN}}$: is on when the transmitter and the receiver are active at the same time (collision). When a collision takes place a 10MHz ± 15% square wave with a 50% ±10% duty cycle will be sent out to COL+ and COL– output pins.

$\overline{\text{JAB}}$: turns on when the transmitter is on for more than 20 to 150 msec. When the jabber is on, in order to not bring down the network, the jabber logic disables the transmitter and turns on the collision signal COL+ and COL–.

$\overline{\text{LMON}}$: is on when $LMON_{IN}$ coming from the ML462X is low and there are signal transitions on RX+ and RX–.

ML462X FEATURES

The ML462X data quantizer is used for signal recovery applications in Fiber Optic systems. The ML462X has a wide bandwidth and large gain which makes it capable of accepting an input signal from a fiber optic receiver as low as 2mV. This analog input gets converted to digital outputs at the TTLOUT pin or ECL+ and ECL– output pins.

The TTL output has been disabled in this Application Note by pulling up TTL_{VCC} and TTL_{GND} since ECL output levels are required by the ML4662. The 3K pulldown resistors on the ECL outputs of the ML4621 keep the outputs biased in their operating range. Due to internal pulldown resistors in the ML4622 and the ML4624, the external pulldown resistors are not required if the ECL output are the only outputs being used. The ML4662 inputs present a minimal load to the ML462X ECL outputs.

ML462X includes a two stage input limiting amplifier with a DC restoration feedback loop. The bandwidth of the ML4621 can be adjusted to the particular needs of the application with the capacitor across pin 7 and 8 (CF1 and CF2 for high corner frequency). The 0.1µF (ML4621) or the 0.01µF (ML4622/24) input capacitors on V_{IN}+ and V_{IN}– set the low corner frequency. (The output source impedance of the fiber optic receiver must be kept low "about 50Ω" to make the input capacitors on V_{IN}+ and V_{IN}– effective).

Since the logic condition for the 802.3 FOIRL is as follows:

"light" = 0
"dark" = 1

The received signal has to get inverted before it goes to the RXIN+ & RXIN– inputs of the ML4662. When the output of the Fiber Optic receiver (HFBR2416) is connected to the V_{IN}+ of the ML462X, the signal is non-inverted at the ECL+ & ECL– outputs. Therefore, the ECL+ must be connected to the RXIN– of the ML4662 and the ECL– to the RXIN+ of the ML4662. The output of the Fiber Optic receiver (HFBR2416) may be connected to the V_{IN}– of the quantizer to invert the ECL outputs of the ML462X. If this is done, the following connections must be made.

ECL+ → RXIN+
ECL– → RXIN–

The Link Monitor function is implemented by the minimum signal discriminator and the threshold generator circuits. The $TTL_{LINKMON}$ and $ECL_{LINKMON}$ outputs both indicate when the input data signal is less than a user defined acceptable level. This is done by monitoring the input signal and peak detecting the output of the limiting amplifier and comparing this level with the voltage at V_{THADJ}. V_{THADJ} is set by the user as specified in the data sheet. To set the minimum input signal of the ML4621 to 3mV, V_{REF} can be tied directly to V_{THADJ} to provide 2.5V at V_{THADJ}.

ML4621: $V_{THADJ} = 600\ V_{INTH(P)} + 0.7$ (1)
ML4622: $V_{THADJ} = 500\ V_{INTH(P–P)}$ (2)
ML4624: $V_{THADJ} = 417\ V_{INTH(P–P)}$

In these equations V_{INTH} is the peak or peak to peak value of the input signal. The receiver sensitivity can be calculated when the Hewlett Packard HFBR2416 with a typical responsivity of 6mV/µW is being used.

ML4621: $V_{INTH(P)}$ = 3mV(Peak) ($V_{THADJ} = V_{REF}$)
Received Power = 6mV(P–P)/(6mV/µW)
= 1µW = –30dBM (PEAK)

ML4622: $V_{INTH(P–P)}$ = 5mV(Peak to Peak)($V_{THADJ} = V_{REF}$)
Received Power = 0.833µW = –30.7dBM (PEAK)

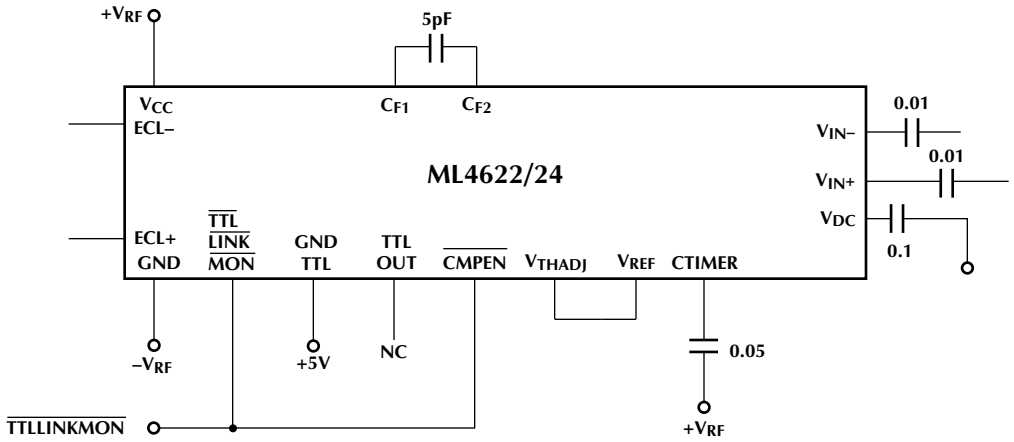
Note: Peak Power = Average Power + 3dBM

This meets the IEEE802.3 10BASE-FL receiver specifications. A lower threshold level can be set by dividing down V_{REF} with a resistor divider, as shown in Figure 2b. By choosing 1K and 140Ω, the V_{THADJ} will be 2.2 volt in the ML4621 which will set the minimum power level at about 2.4mV peak and minimum launch power at –33dBM (considering worst responsivity of 4.5mV/µW). However due to a better stability of the link monitor in the ML4622, both standards will be met considering the worst conditions by tying the V_{THADJ} to V_{REF}. For more detailed information refer to Application Note 6 and Application Brief 1.

In the case of oscillation at $TTL_{LINKMON}$, hysteresis can be added to the ML4621 in two different ways as follows:

1. Adding a feedback resistor from the $TTL_{LINKMON}$ output to the V_{THADJ} (this will only work if a resistor divider is being used to arrive at V_{THADJ}).
2. A capacitive feedback can be implemented by connecting a capacitor from the $TTL_{LINKMON}$ to the ISET pin on the minimum signal discriminator (this will apply if V_{REF} is tied to the V_{THADJ}.
   Note: Adding a 300 ohm to 600 ohm pull-up resistor at the $TTL_{LINKMON}$ to +5Volt may be needed for the stability.

Based on the layout, the value of the hysteresis resistor and capacitor change. Since hysteresis has been added internally to the ML4622 and the ML4624 to increase the stability, the external hysteresis components are not required.



NOTE: IF TTLOUT IS USED, TIE GNDTTL TO UNFILTERED GROUND AND REMOVE L1. IF TTLOUT AND ECL OUTPUTS ARE BOTH USED, ADD 3k PULLDOWN RESISTORS AT ECL OUTPUTS.

Figure 2A. Fiber Optic Receive Circuit A

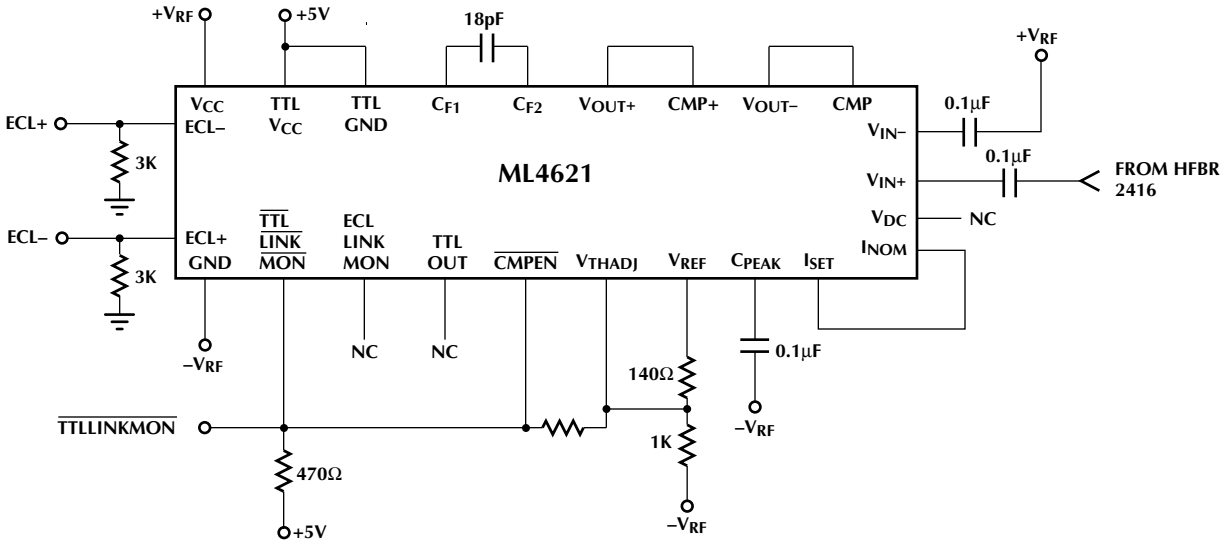


Figure 2B. Fiber Optic Receive Circuit B

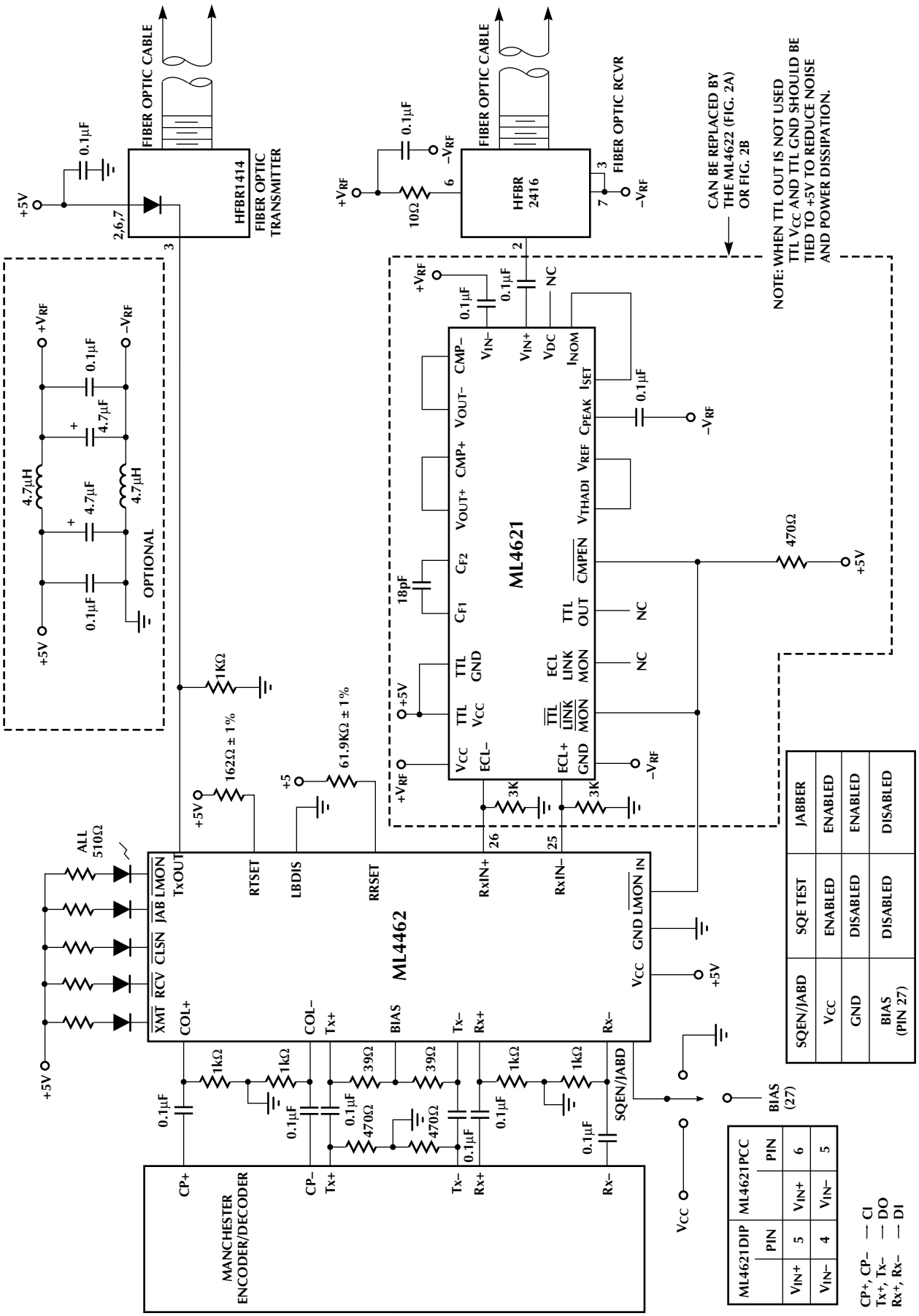
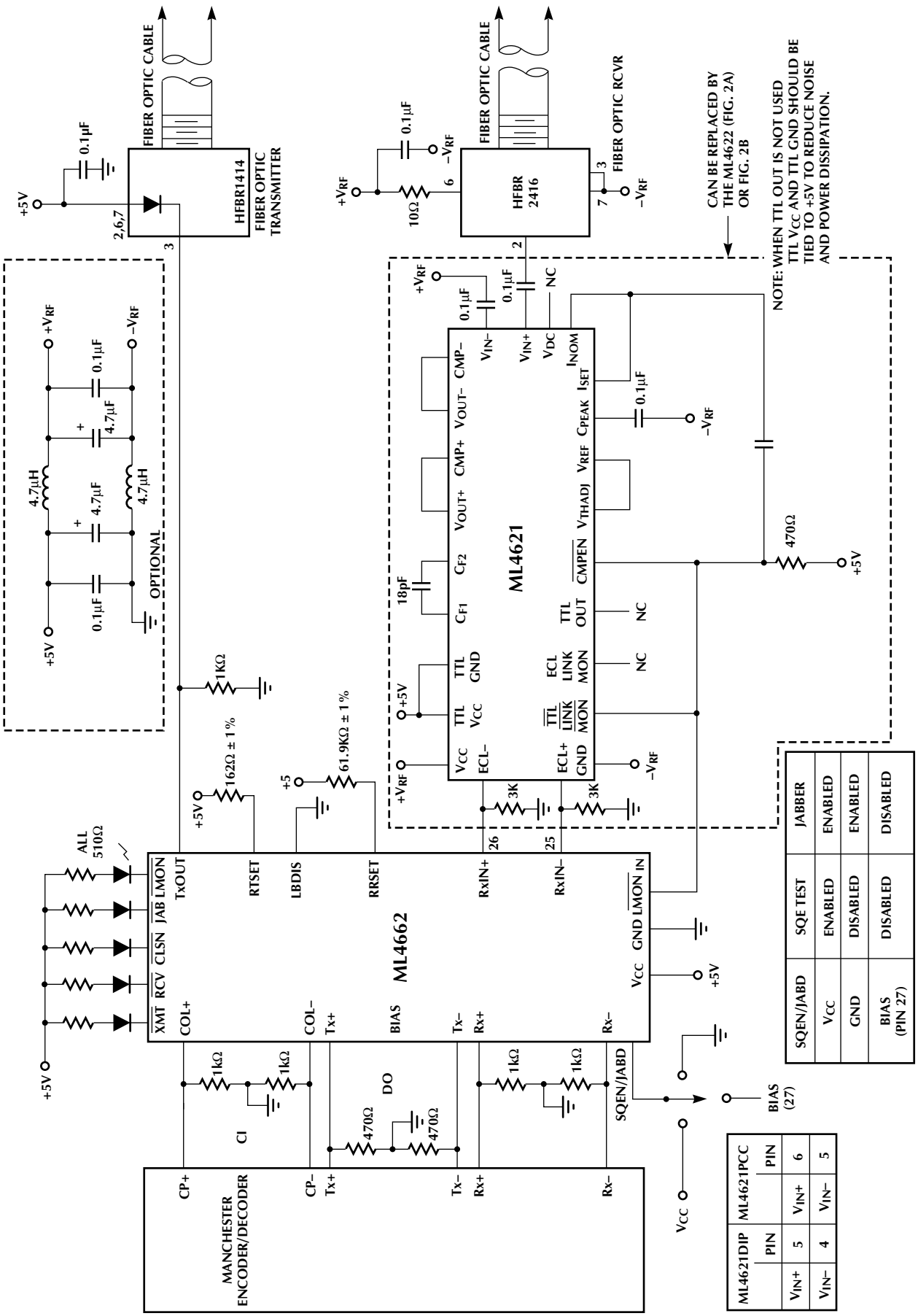


Figure 3. Internal MAU with AC Coupling



SQEN/JABD	SQE TEST	JABBER
V_{CC}	ENABLED	ENABLED
GND	DISABLED	ENABLED
BIAS (PIN 27)	DISABLED	DISABLED

ML4621DIP PIN	ML4621PCC PIN
V_{IN+} 5	V_{IN+} 6
V_{IN-} 4	V_{IN-} 5

Figure 4. Internal MAU with DC Coupling

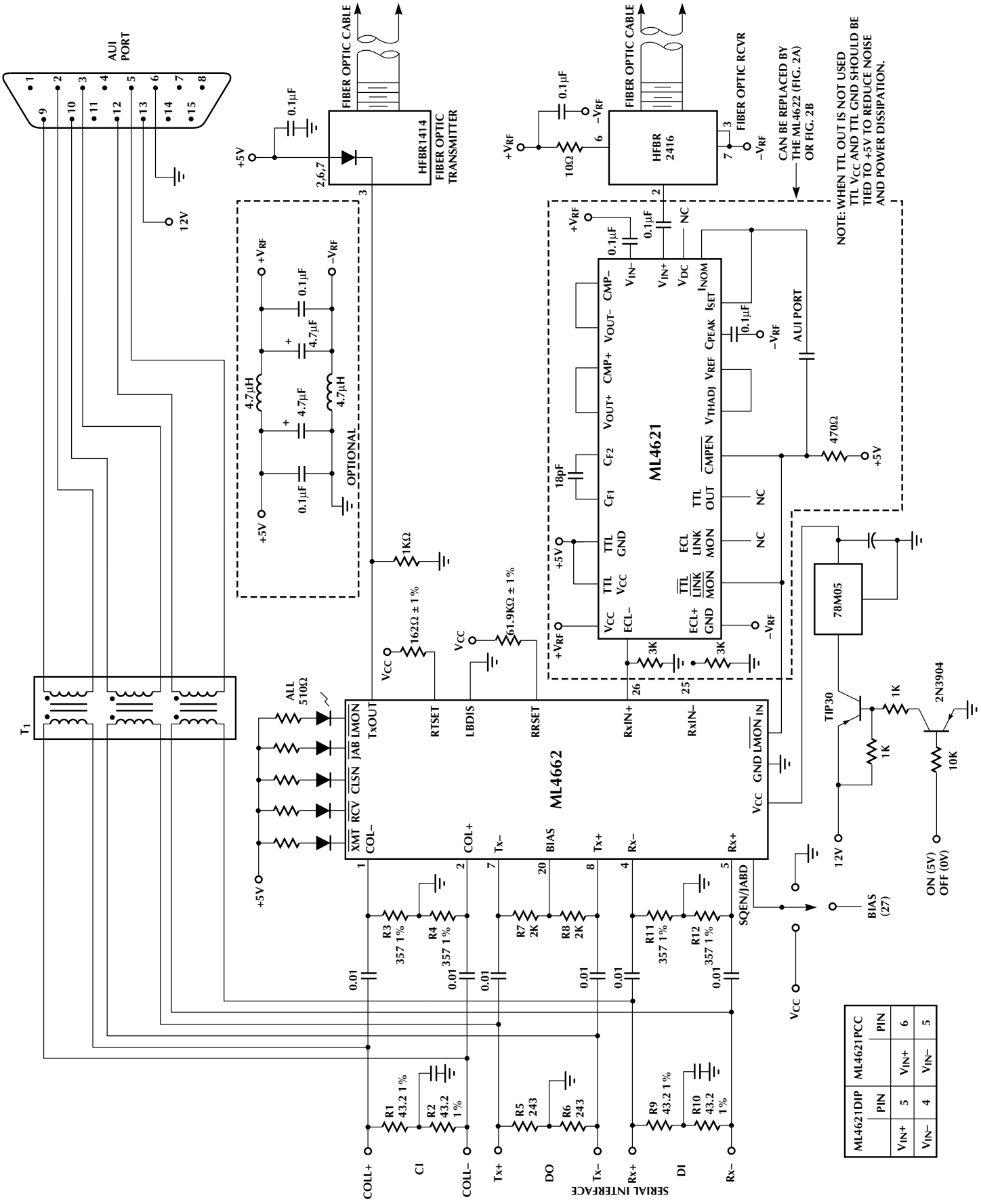


Figure 5. Internal MAU with Shared AUI Port.

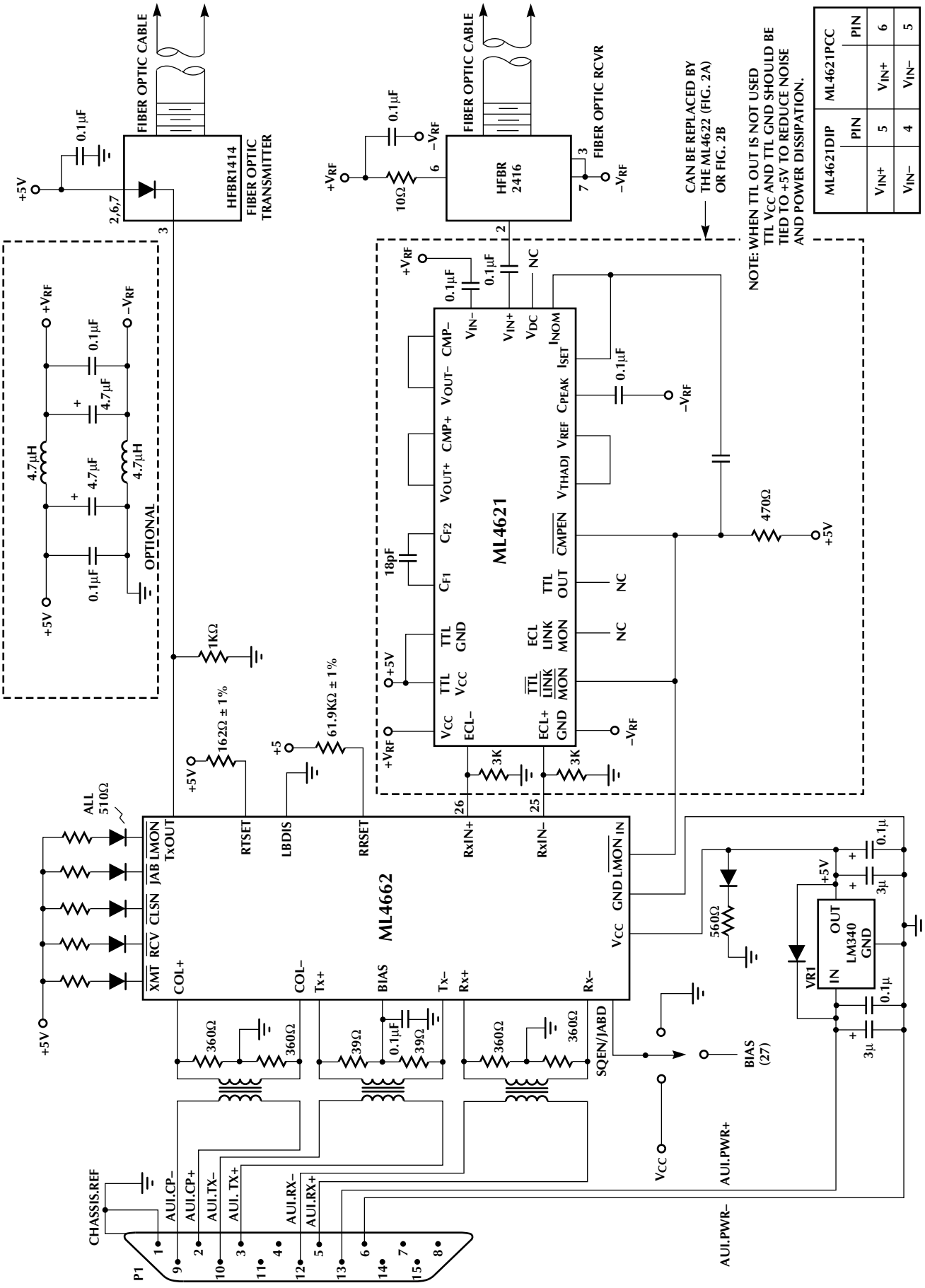


Figure 6. External MAU

FILTERING POWER AND GROUND

Filtering is necessary since unintended feedback through the power supply system (the metallic conductive path of the +5V power line or the Ground reference line for the receiver) can create sustained oscillations or degrade the sensitivity of the receiver. Filters in the power supply for the post-amplifiers, comparator stages and the receiver, prevent noise generated by the quantizer output from being conducted back through the power system to the input amplifier stage.

The quantizer inputs are sensitive low level inputs. V_{CC} and Ground Decoupling are necessary. Disabling the TTL output (by connecting TTL_{GND} and TTL_{VCC} to V_{CC}) of the quantizer will also reduce noise.

ATTACHMENT UNIT INTERFACE

The ML4662 and the ML462X can be used as an internal MAU with the option of having a shared AUI port or as an external MAU. Figures 3, 4, 5 and 6 show a detailed schematic for these three configurations.

Internal MAU: The AU interface may be AC coupled through 0.1µF capacitors across DO, DI, CI pair (Figure 3). They may be DC coupled if the DC levels DO (2V to V_{CC} – 0.5V), DI (3.6V to 4.5V), CI (3.6V to 4.5V) of the manchester encoder/decoder & the ML4662 are the same (Figure 4). (If DC coupling is used, the BIAS pin is not connected and the 39Ω resistors are not needed.) If AC coupling interface is used, DO which is an input must be DC biased (shifted up in voltage) through the BIAS pin for the proper common mode input voltage.

DI and CI are emitter follower outputs which need external 1KΩ or greater (depending on the particular manchester encoder/decoder) pulldown resistors to ground.

By using 1K pull down resistors we can minimize power dissipation by not having to drive the 78Ω AUI cable.

Internal MAU with Shared AUI Port: The AU interface is AC coupled through isolation transformers T1 (Figure 5). This is to protect the transceiver chip, from 16V with respect to the system ground at AUI interface during a fault condition (as specified in 7.4.1.6 and 7.4.2.6 section of the IEEE 802.3 standards for both the driver and the receiver). In addition, it blocks the DC offset voltage of the AUI port that may not match that of the transceiver. An AUI connection requires termination impedance of 78Ω [(R1 + R2)||(R3 + R4)] on the receive end of the transmission lines (DI and CI). The 357Ω resistors for R3 and R4 are chosen to properly bias the driver circuitry. The 2K resistors on TX+ and TX– provide common mode bias input voltage for the ML4662.

The 243Ω resistors (R5, R6) drive the DO pair (either the DO pair of the AUI port of the ML4662). The output AUI drivers of the transceiver must be tri-stated in order to not load down the transmission lines when the AUI port is connected and the FIBER OPTIC port is disconnected.

When the device is powered down, the TX±, RX± and COLL± pins form a substrat diode to the ground. Hence, the output of DO, DI and CI is clamped to one diode drop. Since this is not desirable, we need to add six 0.01µ capacitors at these pins as shown in figure 5. This way we isolate the Manchester Encoder/Decoder at TX pair and the AUI at RX and COL pairs.

+5V to the chip and to all the circuit must be removed when the chip is powered down. This includes power to the chip, +5V at RRSET and RTSET resistors and all status LEDs.

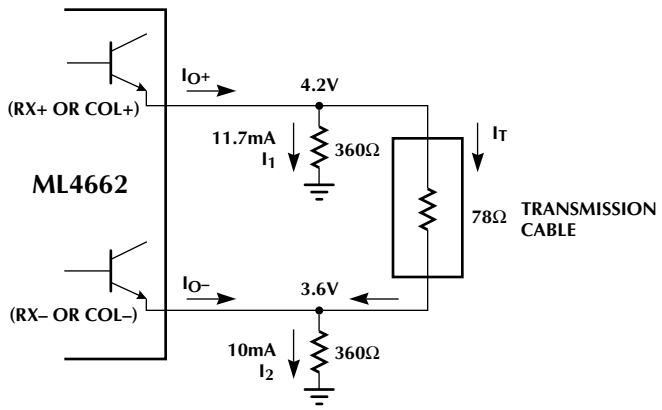


Figure 7. AUI Driver Circuitry.

External MAU: The AU interface is AC coupled through isolation transformers (Figure 6). An AUI connection requires termination impedance of 78Ω. Two 39Ω, 1% resistors tied to DO pair provide impedance matching (78Ω) as well as the proper common mode input voltage to the ML4662.

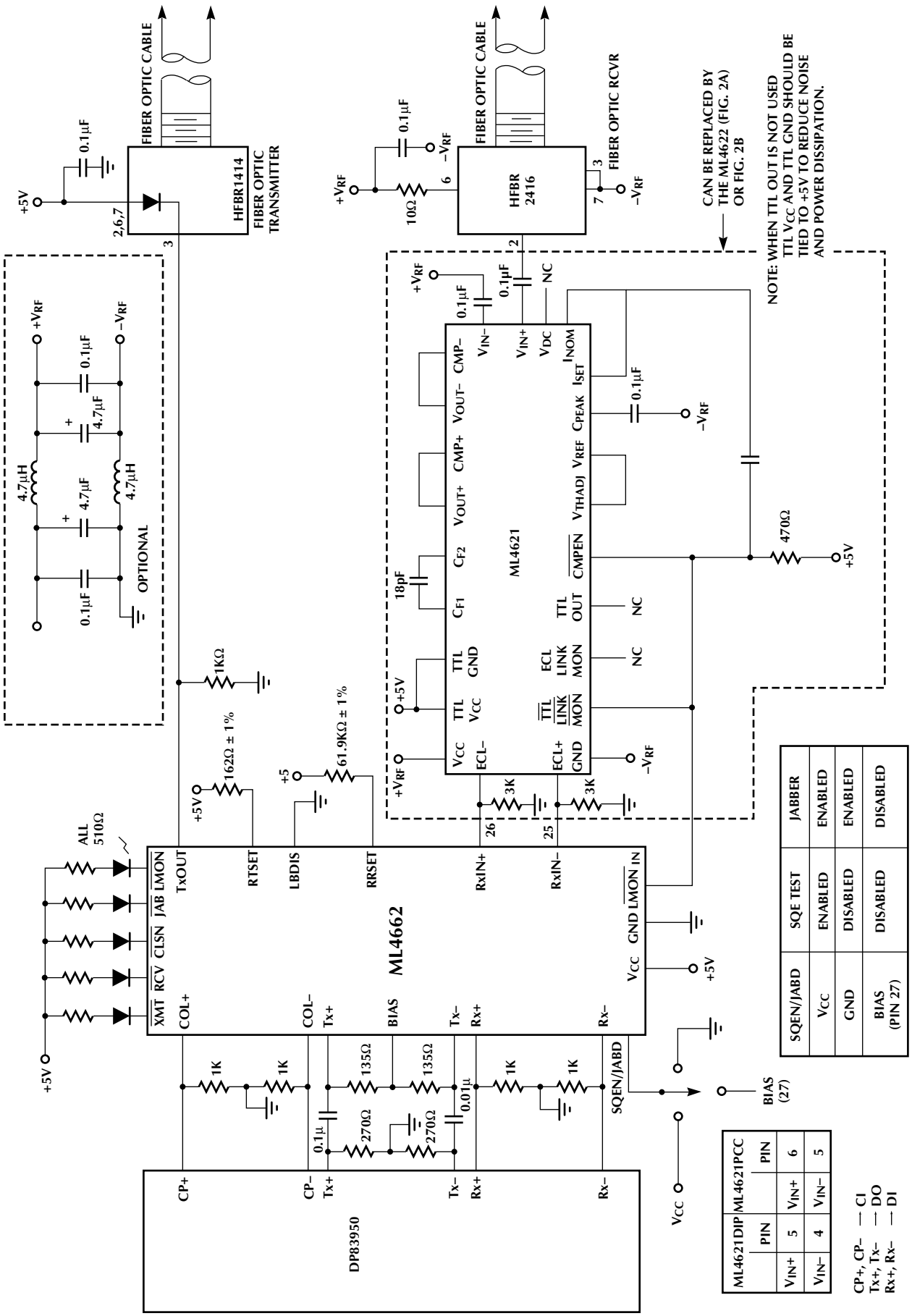
DI and CI pairs are emitter follower outputs. The output structure of the driver stage (RX+, RX–, COL+, COL–) is open emitter (Figure 7). The output is biased at typically 4.2V when high and 3.6V when low. That is a differential voltage of about +0.6V across a 78Ω load.

The pulldown resistors have to be chosen such that during transmission, a minimum of 2.0mA can be sourced by RX– or COL–. By using a 360Ω pulldown resistors the RX– or COL– source 2.3mA and the RX+ or COL+ source 19.4mA as follows:

$I_T = 0.6V/78\Omega = 7.7mA$

$I_{O}+ = I_1 + I_T$
$I_{O}+ = (4.2V/360\Omega) + 7.7mA$
$I_{O}+ = 11.7mA + 7.7mA$
$I_{O}+ = 19.4mA$
$I_{O}- + I_T = I_2$
$I_{O}- = I_2 - I_T$
$I_{O}- = (3.6V/360\Omega) - 7.7mA$
$I_{O}- = 10mA - 7.7mA$
$I_{O}- = 2.3mA$

The termination resistance must be low enough (minimum 200Ω) to not shut off either of the output drive transistors, but not too low in which case the output transistors could saturate.



SQEN/JABD	SQE TEST	JABBER
VCC	ENABLED	ENABLED
GND	DISABLED	ENABLED
BIAS (PIN 27)	DISABLED	DISABLED

ML4621DIP PIN		ML4621PCC PIN	
VIN+	5	VIN+	6
VIN–	4	VIN–	5

Figure 8. Interfacing the ML4662 to DP83950

INTERFACING ML4662 TO DP83950 OR DP83955

The ML4662 and ML462X can be used in a HUB application. Figure 8 shows the interface between the ML4662 and the National Semiconductor DP83950 Repeater Interface Controller (RIC) The DI and CI pairs are DC coupled but DO is AC coupled with 0.01µF in each lead. The 1KΩ pulldown resistors on the DI and CI pairs provide the necessary source current to drive DI & CI pairs.

N-PORT FIBER REPEATER

To build a fiber repeater network we need to use existing 10BASE-T multiport repeater controller chips with fiber optic transceivers. National (DP83950 or DP83955) and AMD (79C980, IMR), repeater chips, can be interfaced to the ML4662 10BASE-FL transceiver. Each Twisted Pair (TP) port of these chips has an internal 10BASE-T transceiver. A different approach should be taken for designing the ML4662 with these chips.

National Repeater: The integrated 10BASE-T transceivers in the National repeater chip can be disabled. Since each Twisted Pair (TP) port is compatible with AUI (Attachment Unit Interface) compliant transceivers, we interface each TP port to the ML4662 through the AUI interface as shown in figure 8. The receive and collision pair (RX±, COL±) are DC coupled and the transmit pair (TX±) is AC coupled. AC coupling is needed at the transmit pair due to different common mode voltage between the TX± of the ML4662 and the National chip. Loopback is enabled in the ML4662 in order to have collision circuit enabled.

AMD repeater: The TP ports in the IMR repeater chip are designed to interface to 10BASE-T only, and it is difficult to interface them to AUI. So the interface between the IMR and the ML4662 is through the AUI of the ML4662 and the TP port of the IMR. To have a successful link, the following steps should be done:

— Link test pulse should not be sent to the ML4662. Since the link test pulses does not get generated on the TXD– of the IMR chip, this pin drives the TX– of the ML4662 as a single ended input, figure 9.

— A resistor divider is used to biased the TX+ of the ML4662 properly (about 3.2V).

— Another resistor divider is used to bias the receive data at RXD– of the IMR.

— The IMR detects a collision during simultaneous transmission and reception. So, the CI pair (COL±) of the ML4662 is not used in this design.

— A 100 ohm resistor eliminates the reflection and it takes care of over driving the TX– by the TXD–.

— A 100 ohm resistor might be needed to eliminate reflection due to the length of RX+ signal line.

— A pulldown resistor at the RX+ of the ML4662 satisfies the ML4662 output requirement.
A 0.1µF capacitor is used to AC couple the receive signal due to different common mode voltage range of the RX+ and RXD+.

— Loopback on the ML4662 should be disabled. This is due to interpreting loopback data as collision by the IMR.

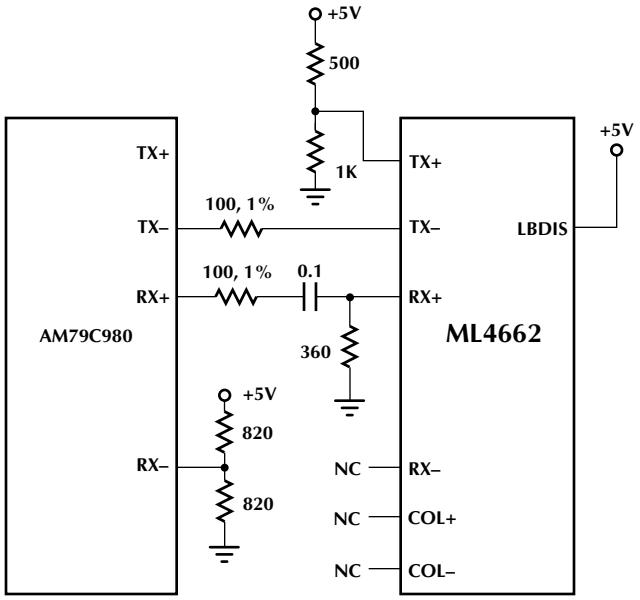


Figure 9. Interfacing the ML4662 to the AMD Repeater

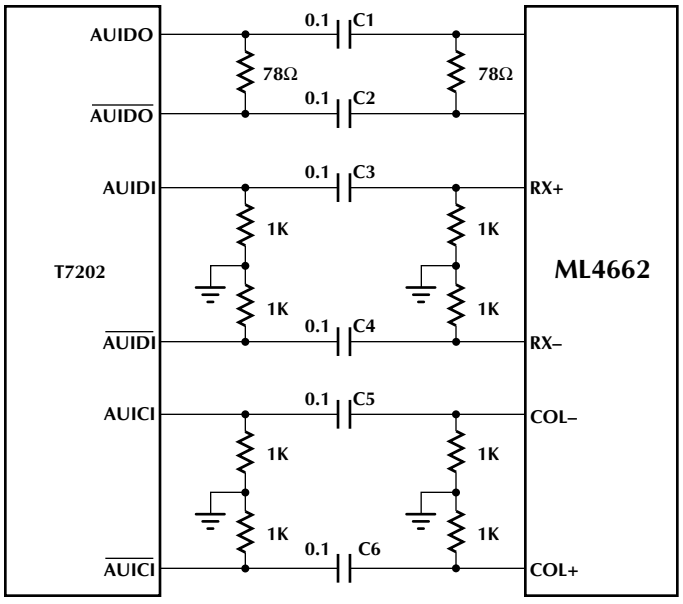


Figure 10. Interfacing the ML4662 to the AT&T Repeater

Interfacing the ML4662 to T7202: T7202 is AT&T multiport repeater controller IC with 12 twisted pair ports and 2 AUI ports. The ML4662 can interface to the AUI port of the T7202 without the need for a transformer as shown in figure 10. The following should be done:

— The DO pair (TX+ and TX–), input to the ML4662 must be DC biased for the common mode input voltage. This is accomplished by having two 39 ohm resistors to the BIAS pin of the ML4662.

— The CI pair should be wired with the reversed polarity so that COL+ of the ML4662 goes to the CI of the AT&T part and the COL– to the CI+.

10BASE-FL SYSTEM SPECIFICATIONS

Some of the key parameters required by the IEEE 802.3 10BASE-FL Standard are listed below:

Transmitter Specifications

1. Peak Emission Wavelength = 790 to 860nm.
2. Spectral Width < 75nm. This is determined by measuring the Full Spectral Width at Half Maximum Amplitude (FWHM) of the LED optical emission. This parameter must be measured at the maximum temperature at which the LED will be operated.
3. Minimum Extinction ≥ 13dB
   Extinction = $|P_{I(ON)} - P_{T(OFF)}|$, where P_T = peak transmitted optical power measured in dBm.
4. Optical Rise/Fall time T_R and T_F < 10ns.
5. $|T_R - T_F| \leq 3$ns.
6. Transmitter Jitter ≤ 2ns.
7. Nominal average power, beginning of life –15dBm
8. Transmit power tolerance ±3dBm
9. Transmit power degradation, end of life –2dB

Receiver Specifications

1. Overdrive limit = –12dBm (average) maximum.
2. Sensitivity ≥ –32.5dBm (average) minimum.
3. The data output of the receiver must be inhibited before the Bit Error Ration of the fiber optic link degrades to greater than 10^{-9}.

Total Link Specifications

1. Transmitter/Receiver must be compatible with fibers having the following core/cladding diameters: 50/125, 62.5/125, 85/125 and 100/140.
2. Link must operate at least at a maximum length of 2Km with each type of fiber.

LAYOUT CONSIDERATIONS

The fiber optic transceiver consisting of the ML4662 transceiver and the ML462X fiber optic quantizer are simple to implement from a data point of view. Electrically, the quantizer is resolving 2mv signals in a logic environment that has an abundance of 5 volt signals. The fiber optic receiver and the quantizer require careful layout, attention to noise coupling, and very clean power supply busses. The following recommendations should be considered while laying out the printed circuit artwork.

POWER SUPPLY

1. Isolate and filter the power and ground to the ML462X (analog portion) and HP receiver (to ensure that noise is not coupled into the low level receiver inputs). This can be accomplished with a pi filter that has a 4 to 7µH inductor in both the power lead as well as the ground lead.
2. Make sure that adequate decoupling is used on both sides of the pi filter, on each chip, and at the fiber optic transmitter and receiver. The fiber optic receiver should be decoupled from the +5 Volt Filtered bus with a 10 ohm resistor and decoupling capacitor. Allow room for large (0.47µF) decoupling capacitors and determine if they can be reduced during testing of the prototypes.

GROUND PLANE

1. The printed circuit board should be a 4 layer board with the +5V. and ground each providing a shielding plane on the inner layers. The fiber optic receiver and the ML462X analog front ends should have its own power supply planes separate from the +5 Volt and Ground planes for the remaining circuitry. These planes should be separated by an air gap physically and electrically by the power supply pi filter from the logic +5 volt and ground.
2. Connect unused pins of HP receiver to the low level receiver Ground.

TRANSMITTER

1. The transmitter output (TXOUT) traces should be as short as possible and make them wide to lower their characteristic inductance.
2. Keep RRSET and RTSET traces (of the ML4662) and resistors away from each other.

GENERAL LAYOUT

1. The physical layout for the receiver should be in a straight line to minimize the trace lengths and potential for noise coupling between the logic signals at the output of the quantizer and the low level signals on the inputs.
2. The trace from the output of the HP fiber optic receiver to the ML462X (V_{IN}+, V_{IN}–) should be as short as possible and shielded if possible.
3. Because of the high gain low level input circuitry in the ML462X, parasitic feedback from the high-level logic-compatible output must be kept to a minimum in order

to prevent undesired oscillations. This is accomplished with a layout which physically separates the receiver inputs (V_{IN}+, V_{IN}–) and outputs (ECL+, ECL–, TTLOUT, CMPEN, $TTL_{LINKMON}$, $ECL_{LINKMON}$).

4. If the TTL outputs of the ML462X are not used, Connect GNDTTL and VCCTTL to +5 volt (this will disable the TTL driver).

INITIAL DEBUG OF THE 10BASE-FL BOARD

1. AUI is connected but Fiber Optic cable is not connected.
   a. Look for 1MHz Idle signal at pin 18 of the ML4662. If there is no Idle signal, verify the following:
      i) Ground and +5V to the ML4662.
      ii) RRSET must be 61.9k (1%) at pin 13 of the ML4662 to +5V
      iii) RTSET should be 162 ohm at pin 12 of the ML4662 to +5V to set the current driven by the TxOUT to 52mA.
   b. The LMON LED must be OFF. If the LMON LED is ON, check the $TTL_{LINKMON}$. If it is low, measure the noise level at filtered power and ground, V_{IN}+ and V_{IN}– of the ML462X. If the peak noise level at the input of the ML462X is greater than the minimum V_{INTH} (Equations 1 and 2), the $TTL_{LINKMON}$ gets activated (low).
   c. The RX LED must be OFF. Otherwise there must be transitions on RX+ and RX– (pins 25 and 26 of the ML4662) less than 3µsec apart because of one of the following reasons:
      i) Too much noise at the inputs of the ML462X (not filtering properly).
      ii) Feedback between the inputs and outputs of the ML462X (poor layout).
      iii) Crosstalk between TxOUT (pin 18 of the ML4662) and inputs of the ML462X (poor layout).
2. Connect Receive Fiber (HFBR2416) to Fiber Optic LED transmitter (HFBR1414) which is sending active idle signal. (Either from another MAU's LED transmitter or from the same MAU's LED transmitter with loopback disabled.)
   a. The LMON LED must go ON and the RX LED must be OFF. If the LMON LED is OFF, verify the following steps:
      i) The Receive Power must be within the 10BASE-FL standard range.
      ii) Verify the idle signal at V_{IN}+ or V_{IN}– of the ML462X
      iii) $TTL_{LINKMON}$ (pin 2 of the ML462X) must be low.
   b. If the RX LED is ON as well as the LMON LED, check step 1c.
3. Start to transmit. The LMON and TX LEDs must be ON. The RX and CLSN LEDs must be OFF in the transmitting MAU if two MAU's are being used. In this case, if the RX and CLSN LEDs are on, check step 1c.
4. Disconnect the Fiber Optic cable from the HFBR2416. The LMON LED must go OFF. If the LMON LED stays on, check step 1b. The RX LED must be OFF. Otherwise check step 1c.
5. After successfully completing the initial debug of the 10BASE-FL board, verify that the board meets 10BASE-FL specifications.

Figure 11 is schematic of the 10BASE-FL evaluation board (ML4662EVAL) which meets the 10BASE-FL standard. This board incorporates all the above critical points of the layout as shown in Figures 12 through 17. The ML4662EVAL is available for purchasing.

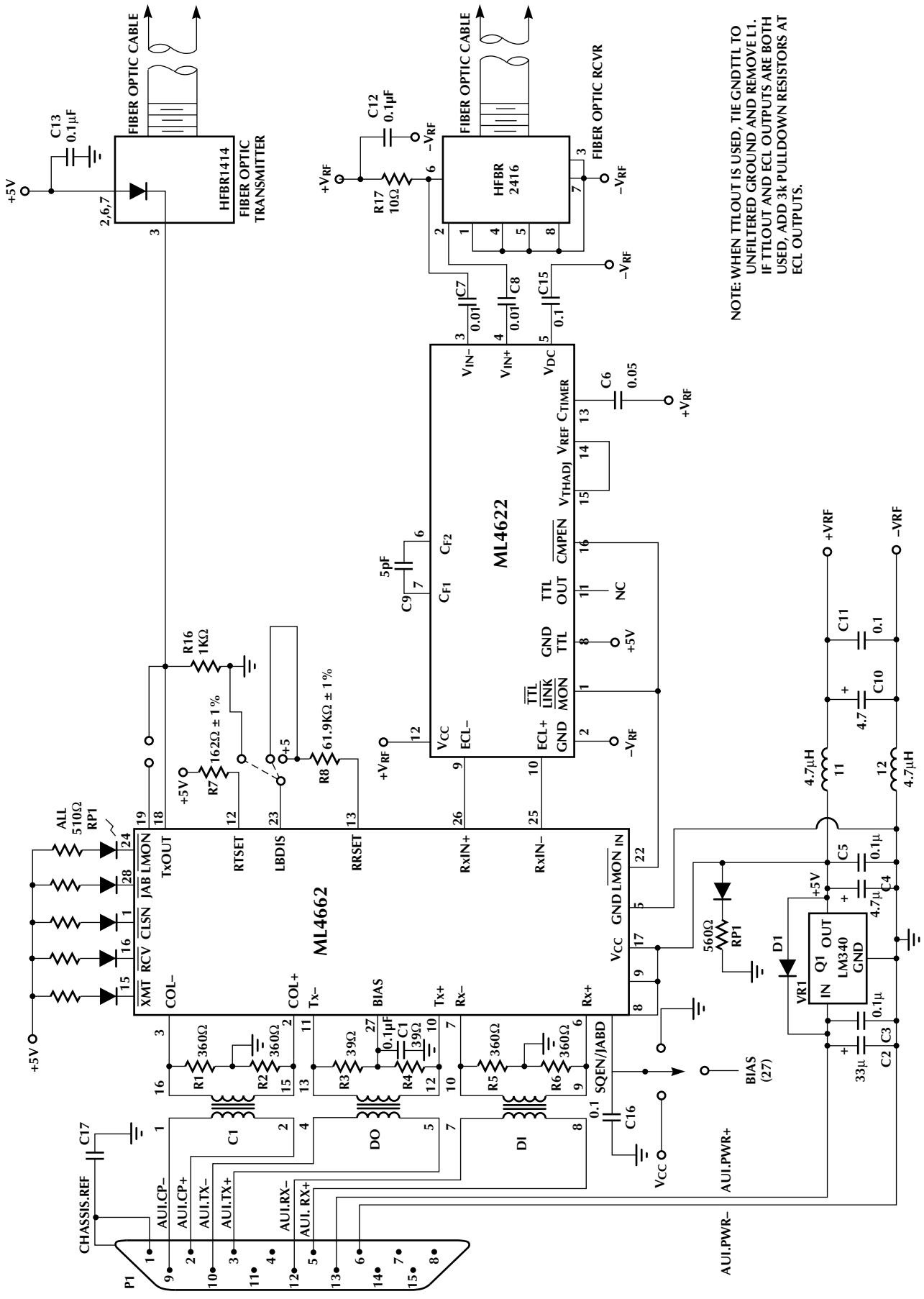


Figure 11. ML4662 EVAL Board

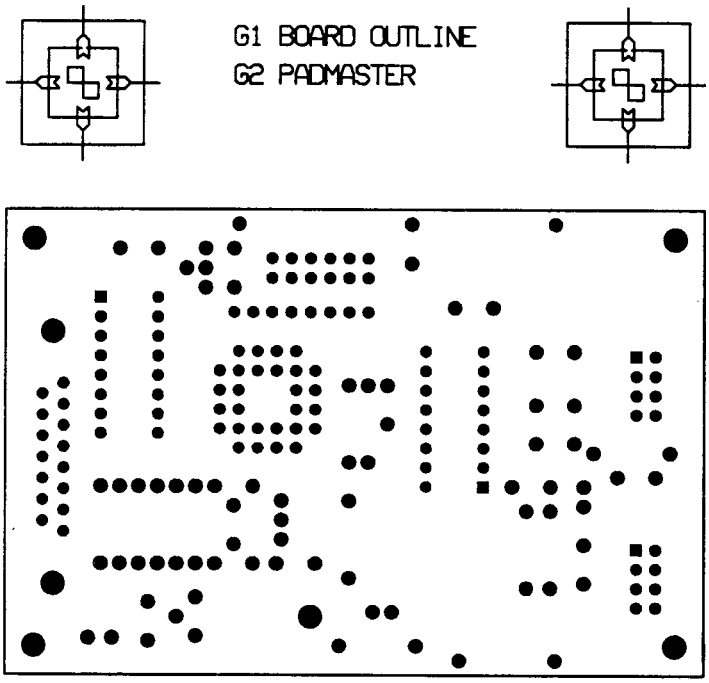


Figure 12.

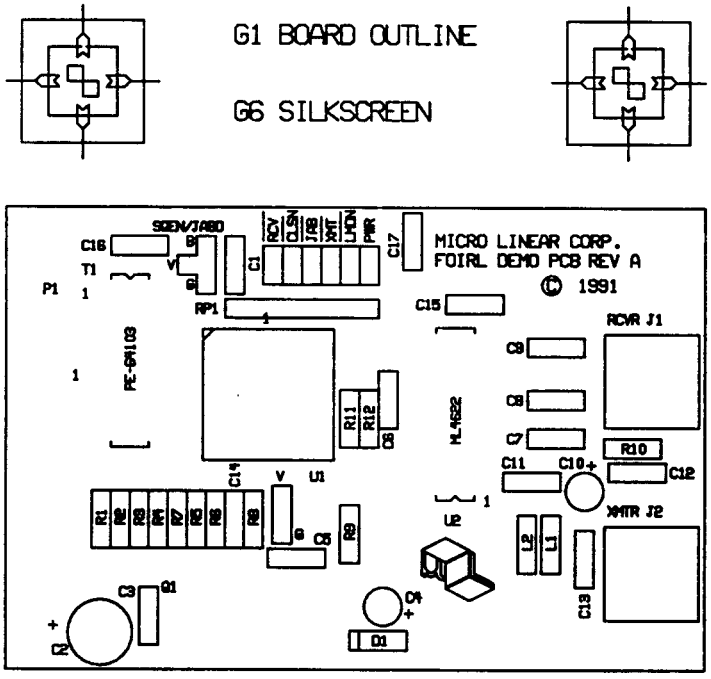


Figure 13.

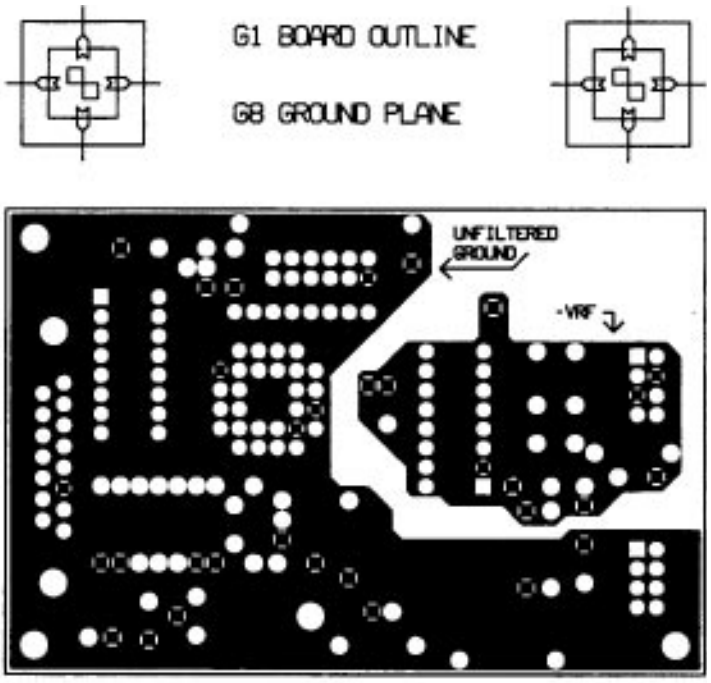


Figure 14.

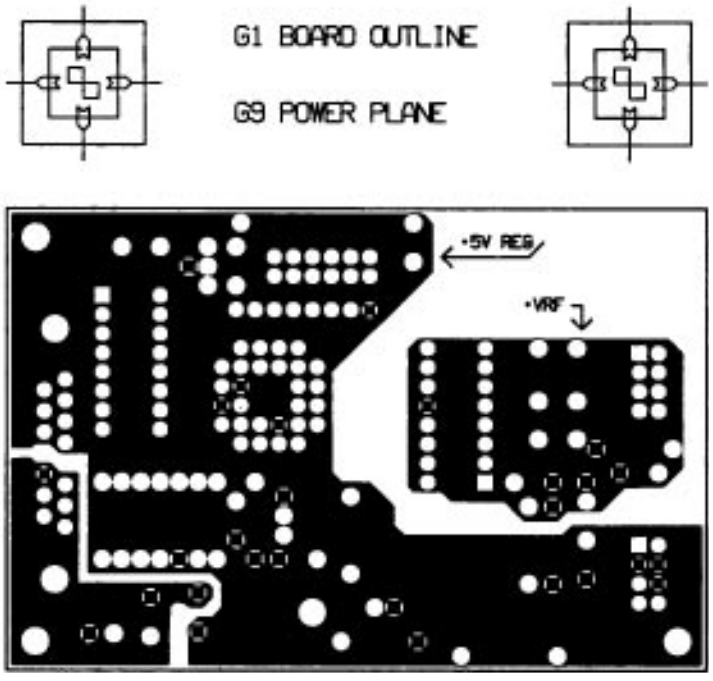


Figure 15.

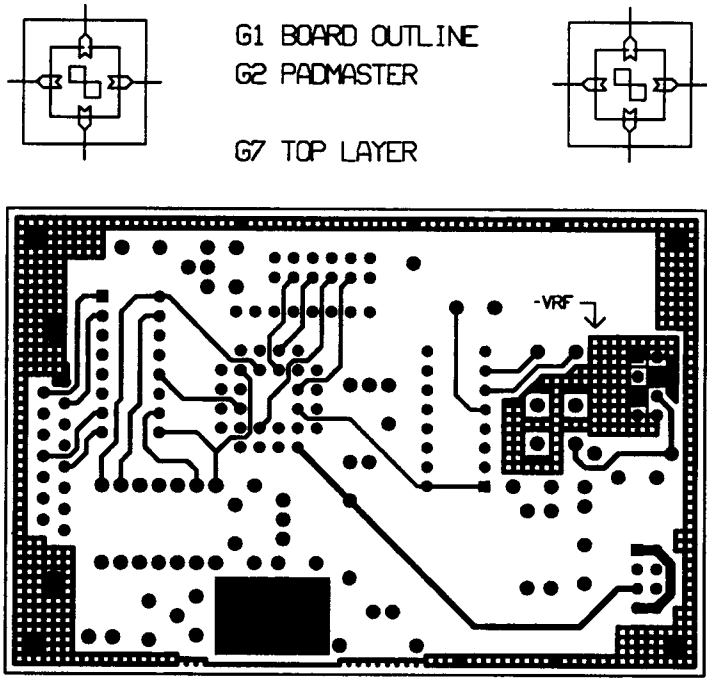


Figure 16.

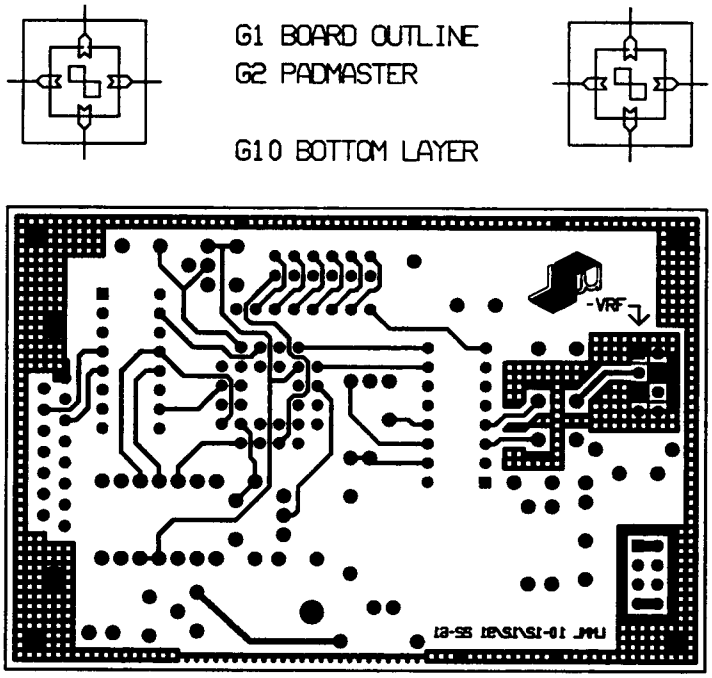


Figure 17.

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