Product Brief

Intel® E7520 Chipset

Embedded Computing

Intel® E7520 Chipset

for Intel® Core™2 Duo Processors and Intel® Core™ Duo Processors

Product Overview

The Intel® E7520 chipset for embedded computing – utilizing dual-processor, high-bandwidth chipset technology – enables reduced power consumption with improved platform reliability and system manageability compared to previous-generation Intel® chipsets. The 667 MHz front-side bus supports Intel® Core™2 Duo processors (T7400[A], L7400[A]) and Intel® Core™ Duo processors (T2500[A], L2400[A]), providing high bandwidth for increased memory and I/O throughput, specifically optimized to offer a value-sensitive solution for embedded and communications applications.

Intel Core 2 Duo processors are based on Intel® Core™ microarchitecture with support for Intel® 64 architecture[5] (Intel® 64) and 36 bits of physical addressing, delivering breakthrough, energy-efficient performance to help equipment manufacturers optimally balance processing capabilities within power and space constraints. Intel Core Duo processors are derived from the Intel® Pentium® M processor with significant hardware architecture enhancements in stack management, instruction execution, and branch prediction. These processors, when paired with the Intel E7520 chipset, provide an ideal solution for a wide range of performance-intensive, low-power communication and embedded applications in smaller form factor designs. While incorporating advanced processor technology, these processors remain software-compatible with previous IA-32 processors.

The Intel® E7520 Memory Controller Hub (MCH) includes PCI Express*[1] serial I/O technology and DDR2 memory technology to help increase I/O bandwidth and reduce system latency for data-intensive applications. It is the central hub for all data passing among the core system elements, including processors, memory, PCI Express I/O, and legacy I/O subsystems.

Memory

This platform can be designed to support single- or dual-channel DDR2-400 memory (up to 4 GB). DDR2-400 memory technology is ideal for storage and memory-intensive applications, providing up to 20% increase in memory bandwidth and up to 40% decrease in power consumption over DDR 333. The memory subsystem interface to the MCH is dual channel, supporting up to four registered DIMMs per channel – depending on memory technology – for a total system bandwidth of up to 6.4 GB/s.

PCI Express

For demanding I/O and networking applications, PCI Express interfaces attach a variety of Intel and third-party I/O solution components and adapters directly to the Intel E7520 MCH at throughput speeds of up to 4 GB/s on each x8 interface, allowing I/O to keep pace with the rest of the platform. The MCH has three x8 PCI Express interfaces which can each be bifurcated into two x4 interfaces for additional configuration flexibility.

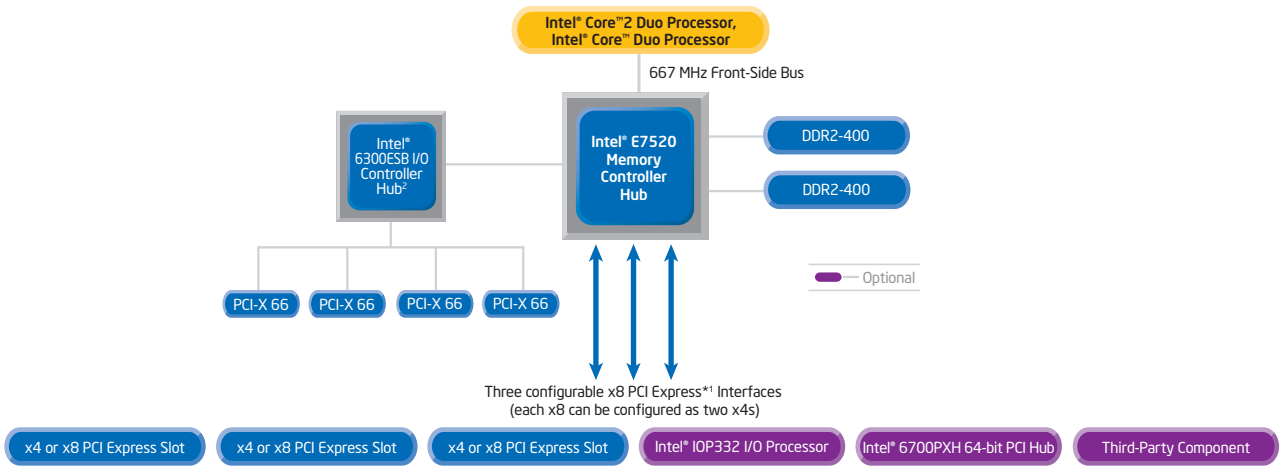

Figure 1: Intel® E7520 Chipset with Intel® Core™2 Duo and Intel® Core™ Duo Processors

[1] PCI Express reduced-power state L0s not supported.

[2] Intel® 6300ESB ICH supports up to 4 PCI-X down devices.

Intel® 6300ESB I/O Controller Hub

Available as the I/O controller hub for legacy I/O support, the Intel® 6300ESB I/O Controller Hub (ICH) attaches directly to the MCH through the Intel® Hub Interface 1.5 connection. For the most demanding storage data transfers, it integrates dual independent SATA controllers, each capable of up to 150 MB/s transfer rate. Four Hi-Speed USB 2.0 ports allow easy I/O connection while offering improved bandwidth compared to USB 1.1 devices. The Intel 6300ESB ICH includes a PCI-X 64/66 bus supporting up to four PCI-X 64/66 MHz masters.

Intel® 6700PXH 64-bit PCI Hub (Optional)

The Intel® 6700PXH 64-bit PCI Hub connects to the MCH through a point-to-point x8 or x4 PCI-X Express interface. Each hub contains two bus segments that can be independently configured to operate in PCI (33 or 66 MHz) or 64-bit PCI-X mode (66, 100, or 133 MHz), for either 32-bit or 64-bit PCI/PCI-X devices. In addition, each hub integrates two PCI standard hot plug controllers – one per PCI/PCI-X interface – and can be independently configured up to two PCI-X 64/133 MHz segments.

Features	Benefits
Supports Intel® Core™2 Duo Processors with 667 MHz front-side bus and 4 MB L2 Cache, and Intel® Core™ Duo Processors with 667 MHz front-side bus and 2 MB L2 cache	• Dual-core processor is optimized for multithreaded applications and multitasking, meeting the need for high-performance, low-power applications with small form-factor constraints
PCI Express*	• Direct connection between the MCH and PCI Express component/adapters; bandwidth up to 4 GB/s on each x8 PCI Express interface; higher bandwidth and less I/O bottlenecks than PCI-X
DDR2-400 memory interface	• Maximum memory bandwidth of 6.4 GB/s • Decreased power consumption – especially important on dense rack, hot-plug controller and blade configurations
Intel® 6700PXH 64-bit PCI Hub (Optional)	• Supports two independent 64-bit, 133 MHz PCI-X segments and two hot-plug controllers (one per segment) • Enhancements to PCI/PCI-X performance and platform flexibility
Intel® Hub Interface 1.5 connection	• Point-to-point connection between the MCH and the Intel® 6300ESB I/O Controller Hub provides 266 MB/s of bandwidth
Advanced Platform RAS	• Features such as memory ECC, Intel® x4 Single Device Data Correction[3] (x4 SDDC), DIMM sparring, DIMM scrubbing and memory mirroring can improve system reliability • 32-bit cyclic redundancy check on PCI Express • Hot swap PCI Express enhances serviceability • SMBus port hooks into Intel® E7520 MCH for remote management operation and support for a variety of third-party base management controller and BIOS solutions

Product	Product Code	Package
Intel® E7520 Memory Controller Hub (MCH)	NQE7520MC	1077 Flip Chip-Ball Grid Array (FC-BGA)
Intel® 6300ESB I/O Controller Hub	FWE6300ESB	689 Plastic Ball Grid Array (PBGA)
Intel® 6700PXH 64-bit PCI Hub (optional)	RG82870P2	567 Flip Chip-Ball Grid Array (FC-BGA)

[A] Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. See http://www.intel.com/products/processor_number for details.

[5] 64-bit computing on Intel® architecture requires a computer system with a processor, chipset, BIOS, operating system, device drivers and applications enabled for Intel® 64 architecture. Processors will not operate (including 32-bit operation) without an Intel® 64-enabled BIOS. Performance will vary depending on hardware and software configurations. Consult with your system vendor for more information.

[3] In an x4 DDR memory device, the Intel x4 Single Device Data Correction (x4 SDDC), provides error detection and correction for one to four data bits within a single device, and provides error detection for up to eight data bits within two devices.

Intel Access

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