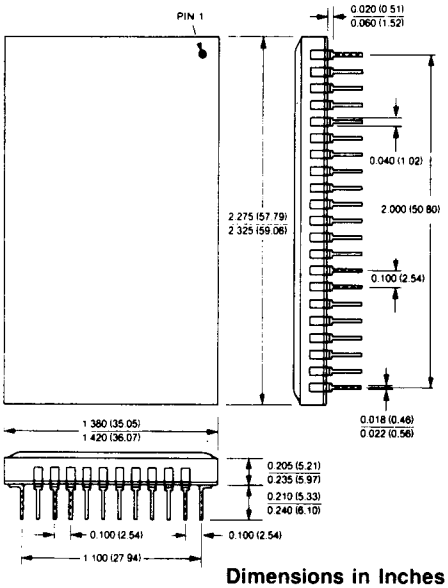
8 and 16-Channel DIP Packaged 12-bit Data Acquisition Systems

FEATURES

- Complete DAS:
  - Multiplexer
  - Address Counter
  - Instrumentation Amp
  - Track-Hold Amp
  - 12-Bit A/D Converter
  - 3-State Output Buffer
  - Timing and Control Logic
- 8 Differential or 16 Single-ended Input Channels
- Instrumentation Amplifier Gains from 1 to 1000
- Random or Sequential Addressing
- 50,000 Channels/sec Guaranteed Throughput
- Small 62-Pin Package
- Full Mil Operation −55°C to +125°C
- MIL-PRF-38534 Optional

62 PIN PACKAGE



Dimensions in Inches (millimeters)

DESCRIPTION

MN7150-8 and MN7150-16 are complete, single-package, 12-bit data acquisition systems. Built with contemporary hybrid construction techniques, each system contains: an overvoltage protected (±35V) input multiplexer; a multiplexer channel-address latch/counter; a high-impedance ($10^8\Omega$) instrumentation amplifier that can have its gain set from 1 to 1000; a high-speed (10μsec max acquisition time) track-hold amplifier with hold capacitor; a high-speed (10μsec max conversion time) 12-bit A/D converter with 3-state output buffer; a 10 Volt buffered reference; and all timing and control logic necessary to operate the system with a single strobe command. The MN7150-8 offers 8 differential input channels; while the MN7150-16 offers 16 single-ended input channels. Both devices guarantee minimum throughput rates of 50,000 channels/sec.

The gain of MN7150's internal instrumentation amplifier is set anywhere from 1 to 1000 with a single external resistor making the full scale input range of the system variable from ±10V to ±10mV. This resistor, ±15V and +5V supplies with bypass caps, and user-optional gain and offset adjust potentiometers are all that is required to configure a fully functional, 12-bit, 50kHz data acquisition system.

MN7150 offers outstanding flexibility. The 12 bits of digital output data can be accessed in any combination of 3 four-bit bytes and a 4-bit mux-address register permits input-channel addresses to be read back if desired. Track-hold acquisition time and droop rate can be varied by adding an external resistor or capacitor. Expansion to 32 single-ended or 16 differential input channels is accomplished with 2 additional IC's.

MN7150 is packaged in a unique, 62-pin, hermetically sealed, ceramic package that occupies approximately 3.2 sq. in.. Devices are fully specified for 0°C to +70°C and −55°C to +125°C (MN7150H) operation, and for military/aerospace applications, 100% screening to MIL-PRF-38534 is optional.

MN7150 8 and 16-CHANNEL DIP-PACKAGED, 12-Bit DATA ACQUISITION SYSTEMS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN7150	0°C to +70°C
MN7150H, MN7150H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+V_{CC}, Pin 43)	−0.5 to +18 Volts
−15V Supply (−V_{CC}, Pin 44)	+0.5 to −18 Volts
+5V Supply (+V_{dd}, Pin 18)	−0.5 to +7 Volts
Analog Inputs (Pins 1-4, 51-62, Note 1)	±35 Volts
Digital Inputs	0 to +7 Volts

ORDERING INFORMATION

PART NUMBER — MN7150-16H/B CH

- Select MN7150-8 or MN7150-16 model
- Standard Part is specified for 0°C to +70°C operation.
- Add "H" suffix for specified −55°C to +125°C operation.
- Add "/B" to "H" devices for Environmental Stress Screening.
- Add "CH" to "H/B" devices for 100% screening according to MIL-PRF-38534.

SPECIFICATIONS (T_A = +25°C, Supply Voltages = ±15V and +5V unless otherwise specified)

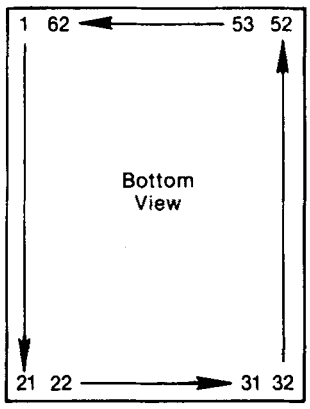
ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Number of Input Channels: MN7150-8 MN7150-16		8 Differential 16 Single-Ended		
Input Voltage Ranges (Note 2): Unipolar Bipolar		0 to +10 −10 to +10		Volts Volts
Common Mode Voltage Range CMRR: G = 1 (10kHz) G = 1000 (60Hz)	±10	 72 100		Volts dB dB
Input Resistance Input Capacitance: Off Channels On Channel: MN7150-8 MN7150-16		100 10 50 100		MΩ pF pF pF
Input Bias Current: Initial (+25°C) Drift (Note 3)		±100 Doubles Every 10°C	±200	pA
Input Offset Current: Initial (+25°C) Drift (Note 3)		±25 Doubles Every 10°C	±50	pA
Input Offset Voltage (Note 4): Initial (+25°C) Drift (Note 3)		±7 20+10G	±12	mV µV/°C
Voltage Noise (RTI, Note 5): G = 1 G = 1000		150 1.6		µV(RMS) µV(RMS)
DIGITAL INPUTS				
Logic Levels: Mux Enable (Pin 5): Logic "1" Logic "0" Other Inputs (Note 6): Logic "1" Logic "0"	+4 +2 	 	 +0.8 +0.8	Volts Volts Volts Volts
Loading: Mux Enable (Pin 5, Note 19) Load Input (Pin 19, Note 14) Other Inputs (Pins 8, 13-16, 20, 21, 26, 31; Note 14)		1kΩ Pullup to +5V 2 1		 LS TTL Loads LS TTL Load
TRANSFER CHARACTERISTICS (Notes 7, 8)				
Integral Linearity Error: Initial (+25°C) Max Over Temperature (Note 3)		±¼ ±½	±½ ±1	LSB LSB
Differential Linearity Error: Initial (+25°C) Drift (Note 3)		±½ ±2		LSB ppm of FSR/°C
12-Bit No Missing Codes		Guaranteed Over Temperature		
Unipolar Offset Error (Notes 9, 10): Initial (+25°C) Drift (Note 3)		±0.05 ±15	±0.1 ±20	%FSR ppm of FSR/°C
Bipolar Zero Error (Notes 9, 11): Initial (+25°C) Drift (Note 3)		±0.05 ±25	±0.1 ±35	%FSR ppm of FSR/°C
Gain Error (Notes 9, 12): Initial (+25°C) Drift (Note 3)		±0.1 ±10	±0.2 ±30	% ppm/°C
DIGITAL OUTPUTS (Note 13)				
Logic Levels: Logic "1" Logic "0"	+2.4	 	 +0.4	Volts Volts
Fanout (Note 14)		5		TTL Loads
Logic Coding (Note 15): Unipolar Ranges Bipolar Ranges		SB OB		

DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
T/H Acquisition Time (Note 16)		9	10	μsec
A/D Conversion Time		9	10	μsec
Throughput Rate (Continuous Convert Mode)	50	55		kHz
$\overline{\text{Strobe}}$ Command Pulse Width	40			nsec
T/H Aperture Jitter T/H Output Droop Rate		1 1		nsec μV/μsec
Feedthrough (@1kHz, Note 17)		±0.005	±0.01	%
Mux Crosstalk Attenuation (@1kHz)		74		dB
Setup Time Digital Inputs (Note 18) to Strobe Hold Time Digital Inputs (Note 18) from Strobe	50		 50	nsec nsec
POWER SUPPLIES				
Power Supply Range: ±15V Supplies +5V Supply	±14.5 +4.75	±15 +5	±15.5 +5.25	Volts Volts
Power Supply Rejection: +15V Supply −15V Supply +5V Supply		±0.003 ±0.003 ±0.001		%FSR/%Supply %FSR/% Supply %FSR/% Supply
Current Drains: +15V Supply −15V Supply +5V Supply		42 −42 125	60 −55 135	mA mA mA
Power Consumption		1885	2400	mW

SPECIFICATION NOTES

1. The MN7150's input multiplexer can withstand continuous voltages up to 20 volts greater than either supply and instantaneous transients up to several hundred volts. In a power-off condition, analog input voltage should not exceed ±20 volts.
2. The gain of the MN7150's internal instrumentation amplifier is set from 1 to 1000 with a single external resistor between pins 47 and 48. Listed input ranges (0 to +10V, ±10V) are for the MN7150's A/D converter. If amplifier gain is greater than 1, the system input range will equal 0 to +10V or ±10V divided by G.
3. Listed specification applies over specified temperature range as selected by part number suffix.
4. This specification applies only to the front end of the MN7150 and is defined as the voltage seen at the output of the T/H amplifier with the T/H in the track mode, with the mux inputs grounded and with the instrumentation amplifier G = 1.
5. Measured at the output of the T/H amplifier.
6. Includes Strobe (pin 8), Mux Address inputs (pins 13-16), Load (pin 19), Clear (pin 20), and Enables (pins 21, 26, 31).
7. Transfer specifications refer to the entire system from mux input to A/D converter output with instrumentation amplifier G = 1.
8. FSR = Full Scale Range. In the unipolar mode, FSR = 10 volts. In the bipolar mode, FSR = 20 volts. For a 12-bit system, 1 LSB = 0.024%FSR.
9. Initial offset and gain errors are adjustable to zero with optional external potentiometers.
10. Unipolar Offset error is defined as the difference between the actual and the ideal input voltage at which the 0000 0000 0000 to 0000 0000 0001 transition occurs when operating on a unipolar input range.
11. Bipolar zero error is defined as the difference between the actual and the ideal input voltage at which the 0111 1111 1111 to 1000 0000 0000 transition occurs when operating on a bipolar input range.
12. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 to 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0001 to 0000 0000 0000.
13. Includes Parallel Data, Mux Address and Status (E.O.C.) outputs.
14. One LS TTL load is defined as sinking 20μA with a logic "1" applied and sourcing 0.4mA with a logic "0" applied. One TTL load is defined as sinking 40μA with a logic "1" applied and sourcing 1.6mA with a logic "0" applied.
15. SB = Straight Binary. OB = Offset Binary. See Output Coding table for details.
16. Includes mux switching and settling time, instrumentation amp settling time and T/H amp acquisition time. Specified for a 20V step settling to ±0.01% FSR.
17. Measured at the output of the T/H with the T/H in the hold mode.
18. Includes Mux Address. Mux Enable, Clear and Load inputs.
19. The MN7150's Mux Enable input (pin 5) goes directly to the enable input of a 506A type CMOS multiplexer and has a 1kΩ pullup resistor to +5V. The enable input of the multiplexer itself draws ±10μA max.

PIN DESIGNATIONS

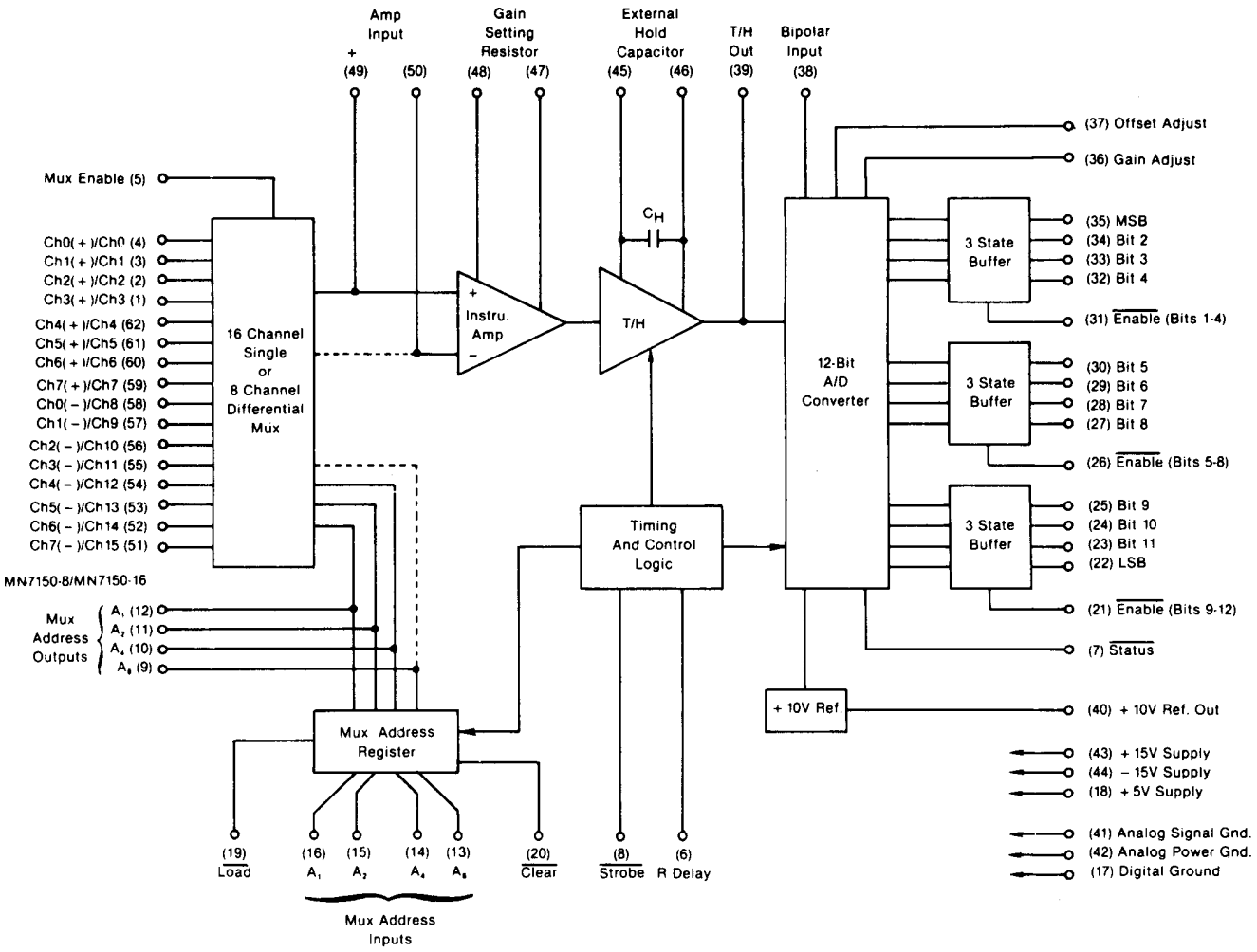


Dot on top of package references pin 1

1	Ch3(+)/Ch3	22	Bit 12 (LSB)	43	+15V Supply
2	Ch2(+)/Ch2	23	Bit 11	44	−15V Supply
3	Ch1(+)/Ch1	24	Bit 10	45	External Hold Cap
4	Ch0(+)/Ch0	25	$\overline{\text{Bit 9}}$	46	External Hold Cap
5	Mux Enable	26	$\overline{\text{Enable}}$ (Bits 5-8)	47	Gain Setting Resistor
6	R Delay	27	Bit 8	48	Gain Setting Resistor
7	$\overline{\text{Status}}$ (E.O.C.)	28	Bit 7	49	Instru. Amp (+) Input
8	Strobe	29	Bit 6	50	Instru. Amp (−) Input
9	A_8	30	$\overline{\text{Bit 5}}$	51	Ch7 (−)/Ch15
10	A_4 } Mux Address	31	$\overline{\text{Enable}}$ (Bits 1-4)	52	Ch6 (−)/Ch14
11	A_2 } Outputs	32	Bit 4	53	Ch5 (−)/Ch13
12	A_1	33	Bit 3	54	Ch4 (−)/Ch12
13	A_8	34	Bit 2	55	Ch3 (−)/Ch11
14	A_4 } Mux Address	35	Bit 1 (MSB)	56	Ch2 (−)/Ch10
15	A_2 } Inputs	36	Gain Adjust	57	Ch1 (−)/Ch9
16	A_1	37	Offset Adjust	58	Ch0 (−)/Ch8
17	Digital Ground	38	Bipolar Input	59	Ch7 (+)/Ch7
18	+5V Supply	39	Track-Hold Output	60	Ch6 (+)/Ch6
19	$\overline{\text{Load}}$	40	+10V Reference Out	61	Ch5 (+)/Ch5
20	$\overline{\text{Clear}}$	41	Analog Signal Ground	62	Ch4 (+)/Ch4
21	$\overline{\text{Enable}}$ (Bits 9-12)	42	Analog Power Ground		

Pins 1-4 and 51-62 are defined for MN7150-8/MN7150-16.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

SUMMARY OF OPERATION—The falling edge of a Strobe pulse loads the multiplexer (mux) channel address and initiates a signal-acquisition and data-conversion cycle. If sequential addressing is being used, the next channel will be accessed. If random addressing is being used, the channel whose address has been applied to the Mux Address Inputs will be accessed. The falling edge of Strobe simultaneously fires an internal one-shot (10μsec pulse duration) whose output controls the operational mode of the track-hold amplifier (T/H). The T/H is driven into the signal-acquisition (tracking) mode for 10μsec during which the mux and instrumentation amplifier settle and the T/H acquires the new signal. After 10μsec, the falling edge of the one-shot drives the track-hold amp into the hold mode, gates on the internal clock, generates a start-convert signal for the 12-bit A/D converter, and drives the Status Output to a logic "1". Gating off the clock during the time the mux is settling into its new channel and the T/H is acquiring a new signal reduces noise errors. When the conversion is complete (a maximum 10μsec later), the Status output returns to a logic "0" indicating that the conversion is complete, that the digital output is valid, and that the T/H amplifier has returned to the tracking mode. The unit is now ready to be triggered for the acquisition and conversion of the next channel.

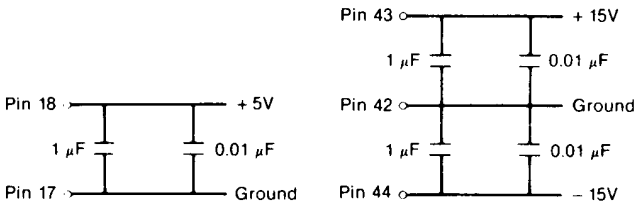
LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN7150-8 and MN7150-16. Units are designed with separate pins for Analog Power Ground (pin 42), Digital Ground (pin 17) and Analog Signal Ground (pin 41), and if your system distinguishes these grounds, the MN7150's pins should be connected respectively. If not, the MN7150's three ground pins should be tied together as close to the unit as possible and all connected to system analog ground, preferably through a large analog ground plane beneath the package.

For the MN7150-16, the inverting input to the internal instrumentation amplifier (pin 50) is not connected to the internal multiplexer and this pin should be connected along with pin 41 (Analog Signal Ground) to the signal-source reference point.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Pins 36 (Gain Adjust), 37 (Offset Adjust) and 38 (Bipolar Input) are particularly noise susceptible. Care should be taken to avoid long runs or runs close to digital lines when utilizing these inputs. If optional gain and offset adjusting is used, care should be taken to locate potentiometers and series resistors as close to the MN7150 as possible.

The output of the MN7150's T/H amp is internally connected directly to the input of the A/D converter. When operating in a unipolar (0 to + 10V) mode, however, pin 39 (T/H Output) must be connected to pin 38 (Bipolar Input) for proper operation. For bipolar (± 10V) operation, pin 40 (+ 10V Ref. Out) must be connected to pin 38 (Bipolar Input) and pin 39 left open.

MN7150 has internal 0.01μF bypass capacitors on each supply line. It is recommended that power supplies be additionally decoupled with tantalum and ceramic capacitors located as close to the device as possible. For optimum performance and noise rejection, 1μF tantalum capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams.



POWER SUPPLY DECOUPLING

DIGITAL PIN FUNCTIONS

Pin Designation	Function
Mux Enable (Pin 5)	"0" disables internal mux. "1" enables internal mux. Use to disable internal mux when addressing additional external multiplexers.
$\overline{\text{Status}}$ (E.O.C.) (Pin 7)	End of conversion. "0" = signal acquisition cycle in progress. "1" = A/D conversion cycle in progress. 1→0 indicates conversion complete. See Timing Diagrams.
$\overline{\text{Strobe}}$ (Pin 8)	"1"→"0" falling edge updates (increments) mux channel and initiates signal acquisition and A/D conversion cycles.
Mux Address Out (pins 9-12)	Output of mux address register. Shows channel currently on. Straight binary coding. See section describing Channel Address Modes.
Mux Address In (Pins 13-16)	Selects mux channel in random address mode. Straight binary coding. See section describing Channel Address Modes.
$\overline{\text{Load}}$ (Pin 19)	"0" = random address mode. "1" = sequential address mode.
$\overline{\text{Clear}}$ (Pin 20)	A logic "0" applied to this pin forces mux address to Ch0 on next falling edge of strobe regardless of Load and Mux Address Inputs. Tie to logic "1" when not in use.
$\overline{\text{Enable}}$ (Bits 9-12) (Pin 21)	"0" enables three-state buffer for A/D converter bits 9-12 (LSB). "1" disables buffer.
$\overline{\text{Enable}}$ (Bits 5-8) (Pin 26)	"0" enables three-state buffer for A/D converter bits 5-8. "1" disables buffer.
$\overline{\text{Enable}}$ (Bits 1-4) (Pin 31)	"0" enables three-state buffer for A/D converter bits 1(MSB)-4. "1" disables buffer.

ANALOG PIN FUNCTIONS

Pin Designation	Function
R Delay (Pin 6)	Connect external resistor to lengthen T/H acquisition time when instrumentation amp is set for high gain. R = (Acq. Time) 10^9 – 9kΩ. For normal operation pin 6 must be connected to +5V.
Gain Adjust (Pin 36)	Connect user-optional, external, 20kΩ, gain-adjust potentiometer here.
Offset Adjust (Pin 37)	Connect user-optional, external, 20kΩ, offset-adjust potentiometer here.
Bipolar Input (Pin 38)	Connect to T/H Output (pin 39) for unipolar (0 to + 10V) operation. Connect to + 10V Ref. Out (pin 40) for bipolar (± 10V) operation.
T/H Output (Pin 39)	Connect T/H Output to Bipolar Input (pin 38) for unipolar operation. Leave open for bipolar operation.
+ 10V Ref. Out (Pin 40)	Connect to Bipolar Input (pin 38) for bipolar (± 10V) operation. Open for unipolar (0 to + 10V) operation. Accuracy = ± 0.05% typical. Drift = ± 10ppm/°C typical. Buffer if used to drive external load.
External Hold Capacitor (Pins 45-46)	Add external polypropylene or teflon hold capacitor to improve T/H droop rate.
Gain Setting Resistor (Pins 47-48)	Select gain resistor with formula R = 20k/(G – 1). Leave open for G = 1.
Instrumentation Amp Inputs (Pins 49-50)	Use when adding additional external multiplexers for expanded single-ended or differential operation. Connect pin 50 to Analog Signal Common for MN7150-16.

STATUS OUTPUT (E.O.C.)—The status or End of Conversion (E.O.C.) output (pin 7) indicates whether the MN7150 is tracking or converting an input signal. When Status is a logic "0", the MN7150's internal T/H amplifier is in the tracking mode and digital output data from the previous conversion is still valid. When the Status is a logic "1", the T/H is in the hold mode, the internal A/D is converting, and the output data is not valid. The falling edge of Status indicates that the conversion is complete, that the output data is valid, and that the T/H has returned to the tracking mode.

CHANNEL ADDRESS MODES

The MN7150-8 and MN7150-16 may have their input multiplexer channels either randomly or sequentially addressed. For random addressing, pin 19 (Load) must have a logic "0" applied. For sequential addressing, pin 19 must have a logic "1" applied.

Address Mode	Mux Enable	$\overline{\text{Load}}$	$\overline{\text{Clear}}$	Address Inputs	Address Outputs	$\overline{\text{Strobe}}$
Random	1	0	1	Next Channel	On Channel	1→0
Sequential	1	1	1	Don't Care	On Channel	1→0
Free Running Sequential (Note 2)	1	1	1	Don't Care	On Channel (Note 1)	1→0

NOTES

1. In the free running sequential address mode, the channel address output lines indicate the channel currently being sampled (Ch_n) while digital output data is valid for the previously sampled channel. ($Ch_n - 1$).

2. The free running sequential mode is implemented by tying the Status output (pin 7) to the Strobe input (pin 8). At the end of each conversion, the falling edge of Status increments the address counter and initiates the next acquisition/conversion cycle.

RANDOM ADDRESSING—For random channel addressing, the Load pin (pin 19) must be tied to logic "0"; the Clear pin (pin 20) tied to logic "1" (or left open); and the desired channel address (in 8421 binary) applied to the Mux Channel Address Inputs (pins 13-16, pin 16 = A_1, pin 15 = A_2, pin 14 = A_4, pin 13 = A_8). In this address mode, the MN7150's internal address latch/counter acts as a 4-bit parallel register. The falling edge of the Strobe pulse latches the new channel address and initiates the data acquisition and conversion cycle. For the MN7150-8 (8-channel differential input), address line A_8 is not required and pin 13 is a "don't care".

When Clear (pin 20) has a "0" applied, the next falling edge of the Strobe command will drive the mux to channel 0 (address 0000) regardless of the data on the address input lines and regardless of the signal applied to the Load line.

Because the Strobe line activates the control logic and does not drive the address latch directly, channel-address input data must be valid 50nsec both before and after the falling edge of the Strobe pulse.

SEQUENTIAL ADDRESSING—For sequential channel addressing, the Load pin (pin 19) and the Clear pin (pin 20) must both be tied to logic "1". In this mode, the internal address latch/counter acts as a 4-bit counter, and the falling edge of the Strobe pulse increments the channel address and initiates the data acquisition and conversion cycle. Channel 0 will be accessed after channel 7 (MN7150-8) or channel 15 (MN7150-16). If one changes from random to sequential addressing, the next channel accessed will be one higher than the channel last randomly addressed. Changing digital data appearing at the address inputs will not affect the MN7150 when it is in the sequential address mode.

SEQUENTIAL ADDRESSING CONTINUOUS CONVERSIONS—The MN7150 can be made to continuously sequence through channels acquiring and converting data by applying logic "1's" to the Load and Clear pins (pins 19 and 20) and tying the Status (E.O.C.) output (pin 7) back to the Strobe input (pin 8). In this mode, Status going low at the end of a conversion becomes the falling edge of Strobe that addresses the next channel and initiates the next data acquisition and conversion cycle. After each channel has been converted and the Status has dropped to a "0", the output data will be valid for approximately the next 10μsec while the multiplexer is switching channels and the T/H is acquiring the new signal. When continuously converting in this manner, an external Strobe signal should be provided at power-on to avoid possible latch-up.

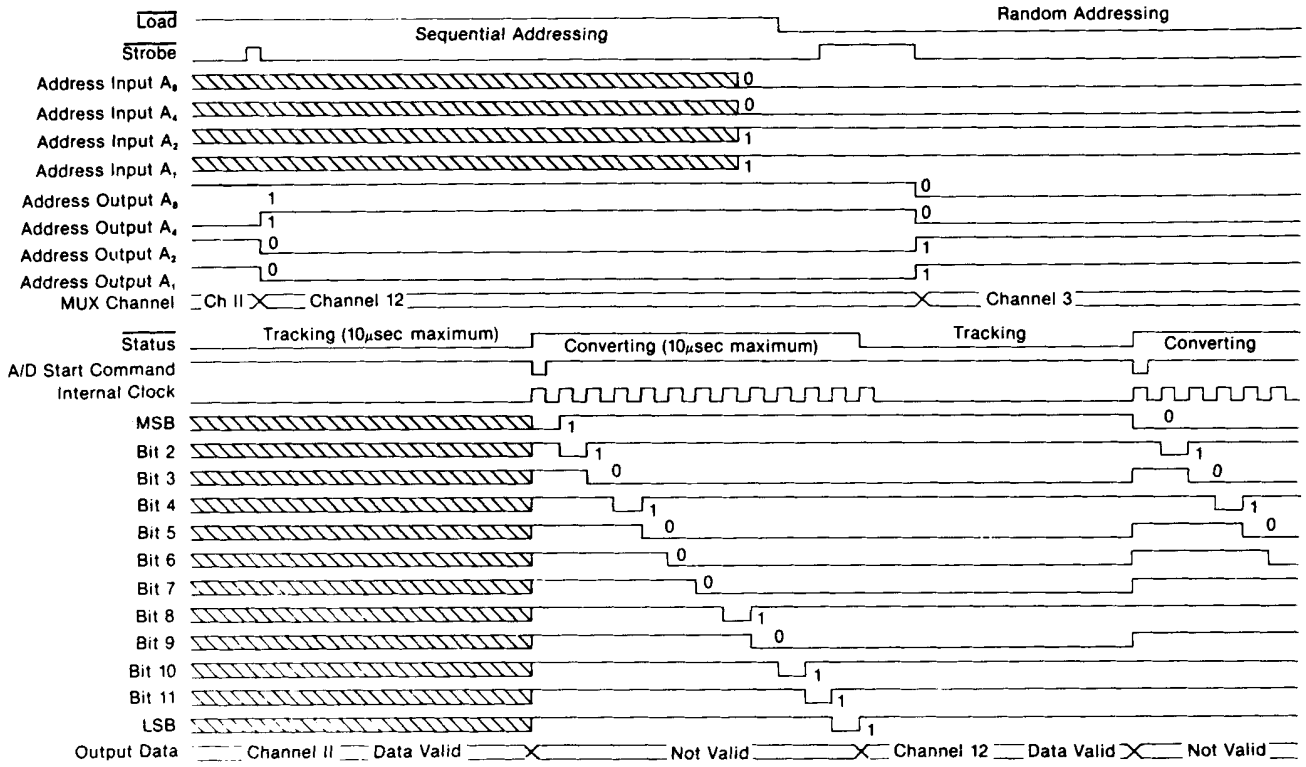
Address inputs				Mux Enable	Channel Selected	
A_8	A_4	A_2	A_1			
X	X	X	X	0	None	
0	0	0	0	1	0	
0	0	0	1	1	1	
0	0	1	0	1	2	
0	0	1	1	1	3	
0	1	0	0	1	4	
0	1	0	1	1	5	
0	1	1	0	1	6	
0	1	1	1	1	7	MN7150-8
1	0	0	0	1	8	
1	0	0	1	1	9	
1	0	1	0	1	10	
1	0	1	1	1	11	
1	1	0	0	1	12	
1	1	0	1	1	13	
1	1	1	0	1	14	
1	1	1	1	1	15	MN7150-16

NOTES

1. For the MN7150-8, Mux Address Input Line A_8 (pin 13) is a "don't care". Pin 13 is connected to the MN7150-8's address latch/counter, however, the A_8 output of the latch/counter is not connected to the MN7150-8's internal mux.

CHANNEL ADDRESS OUTPUTS—The MN7150's Channel Address Outputs (pins 9-12) are tied directly to the unit's internal address counter/latch. They indicate, in 8421 binary, the multiplexer channel presently being accessed. When using external multiplexers for expanded differential or single-ended operation, these outputs can be used to address the external multiplexers, eliminating the need for any additional address decoding circuitry. When using sequential addressing, the appropriate Channel Address Outputs can be NORed together to generate a frame sync pulse each time channel 7 (8 channel systems) or channel 15 (16 channel systems) is being addressed. In microprocessor-based systems, the Address Outputs can be 3-state buffered to add channel read-back capability.

TIMING DIAGRAM



TIMING DIAGRAM NOTES

1. MN7150's internal clock and A/D start-convert command signals are not pinned out externally. They are included here to help the user understand MN7150 operation.
2. The data acquisition/conversion cycle is initiated by the falling edge of strobe. The strobe has a minimum positive or negative pulse width of 40nsec. In other words, strobe must be positive a minimum of 40nsec prior to its falling edge and negative a minimum of 40nsec after its falling edge.
3. Strobe may be brought high after an acquisition/conversion cycle has begun with a new cycle not beginning until the next falling edge.
4. Mux Address, Load and Clear inputs must be valid 50nsec before and after the falling edge of strobe.
5. Mux Address Outputs become valid typically 40nsec after the falling edge of strobe.
6. The internal clock is gated off during the 10μsec signal acquisition period to reduce noise.
7. When Status = "1", the internal T/H is in the hold mode, and the A/D converter is performing a conversion. When Status = "0", the conversion is complete; output data is valid; and the T/H has returned to the track mode. Data will remain valid until Status goes high again.
8. When the Status goes high indicating that an A/D conversion has begun, the MSB goes to a "0" and all other output bits go to a "1". Output bits are set to their final state on succeeding rising clock edges.
9. When enabling 3-state output buffers to access digital data, data becomes valid no longer than 50nsec after an enable line is brought low.

DIGITAL OUTPUT CODING

Analog Input Voltage (Volts)				
Unipolar Ranges		Bipolar Ranges		Digital Output
General	0 to +10V	General	±10V	MSB LSB
FS	+10.0000	+FS	+10.0000	1111 1111 1111
FS – 1½LSB	+9.9963	+FS – 1½LSB	+9.9927	1111 1111 111Ø*
½FS + ½LSB	+5.0012	0 + ½LSB	+0.0024	1000 0000 000Ø*
½FS – ½LSB	+4.9988	0 – ½LSB	–0.0024	0111 1111 111Ø*
½FS – 1½LSB	+4.9963	0 – 1½LSB	–0.0073	0111 1111 110Ø*
0 + ½LSB	+0.0012	–FS + ½LSB	–9.9976	0000 0000 000Ø*
0	0.0000	–FS	–10.0000	0000 0000 0000

NOTES

1. FSR stands for full scale range and is equivalent to the nominal peak-to-peak voltage of the selected input voltage range.
2. 1LSB for a 12-bit system is equivalent to FSR/4096. Therefore, for a 20V FSR, 1LSB = 4.88mV; for a 10V FSR, 1LSB = 2.44mV, etc.
3. For unipolar input ranges, output coding is straight binary. For bipolar input ranges, output coding is offset binary.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

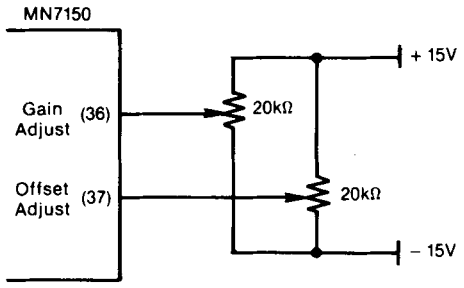
EXAMPLE: For an MN7150 operating on its ± 10V input range, the transition from digital output 0000 0000 0000 to 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of –9.9976 volts. Subsequently, any input voltage more negative than –9.9976 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of –0.0024 volts, and the 1111 1111 1111 to 1111 1111 1110 transition should occur at +9.9927 volts. An input more positive than +9.9927 volts will give all "1's".

OPTIONAL OFFSET AND GAIN ADJUSTMENTS—The MN7150 will operate as specified without additional adjustments. If desired, however, system absolute accuracy error can be reduced to ±1LSB by following the trimming procedure described below. Adjustments should be made following warmup, and to avoid interaction, the offset adjustment must be made before the gain adjustment. Multiturn potentiometers with TCR's of 100 ppm/°C or less are recommended to minimize drift with temperature. Series resistors can be ±20% carbon composition or better. If these adjustments are not used, Pins 36 and 37 should be left open. Do not ground. If gain and offset adjusting is being performed on the MN7150-16, reference voltages may be applied to any channel. If gain and offset adjusting is being performed on the MN7150-8, reference voltages should be applied to the (+) input of a given channel with the (−) input tied to analog ground.

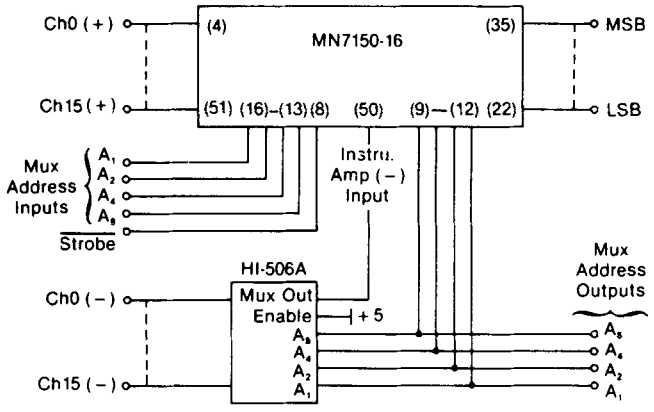
It is recommended that gain and offset adjusting be accomplished while the system is performing continuous or at least repeated conversions. If random addressing is used, the mux will have to be held on one channel during the process. If the continuous-converting sequential-address mode is used (Status output tied to Strobe input), the Clear line will have to be held low to keep the input multiplexer on channel 0. Alternatively, the voltages may be applied to all channels simultaneously.

OFFSET ADJUSTMENT—Connect the offset potentiometer as shown and apply an analog input voltage equivalent to + ½LSB if operating in a unipolar mode or −½ LSB if operating in a bipolar mode. Have the MN7150 performing repeated conversions, either by being in the continuous converting mode or by being under external control. For the unipolar mode, adjust the offset potentiometer "down" until all the output bits are "0". Then adjust "up" until the LSB just turns to a "1". For bipolar mode, adjust the potentiometer "down" until the bits are MSB 0111 1111 1111 LSB. Then adjust it "up" until the bits just turn to MSB 1000 0000 0000 LSB.

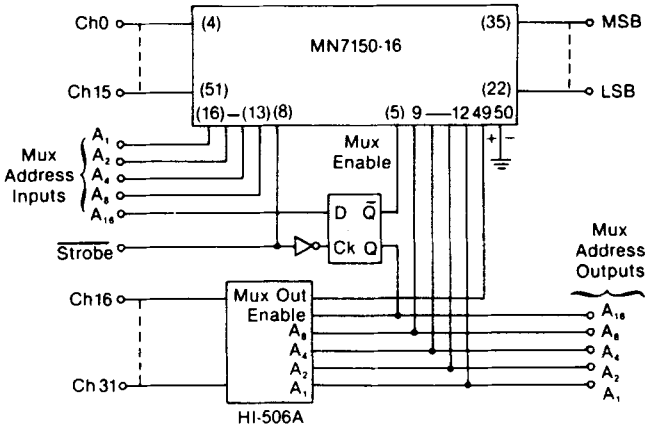
GAIN ADJUSTMENT—Connect the gain potentiometer as shown and apply an analog input voltage equivalent to +FS−1½ LSB. With MN7150 performing repeated conversions, adjust the gain potentiometer "up" until all the output bits are "1". Then adjust "down" until the LSB just turns to a "0".



MULTIPLEXER EXPANSION—The MN7150-16's input capabilities are easily expanded beyond 16 channels with the addition of external analog multiplexers. The diagrams below show the implementation of 32-channel single-ended and 16-channel differential systems. For further single-ended expansion, additional mux's can be tied to pin 49 (the noninverting input to the internal instrumentation amplifier) or cascaded in front of the MN7150's internal mux. Remember that for single-ended operation, pin 50 (the inverting input to the internal instrumentation amplifier) has to be grounded. For further differential expansion, additional multiplexers will have to be tied to both the inverting (pin 50) and noninverting (pin 49) inputs of the internal instrumentation amplifier.



Expansion to 16 Differential Channels



Expansion to 32 Single-ended Channels