Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (2K x 8 BIT)

IDT6116SA
IDT6116LA

FEATURES:

- High-speed access and chip select times
  - — Military: 20/25/35/45/55/70/90/120/150ns (max.)
  - — Commercial: 15/20/25/35/45ns (max.)
- Low-power consumption
- Battery backup operation
  - — 2V data retention voltage (LA version only)
- Produced with advanced CMOS high-performance technology
- CMOS process virtually eliminates alpha particle soft-error rates
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in ceramic and plastic 24-pin DIP, 24-pin Thin Dip and 24-pin SOIC and 24-pin SOJ
- Military product compliant to MIL-STD-833, Class B

DESCRIPTION:

The IDT6116SA/LA is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

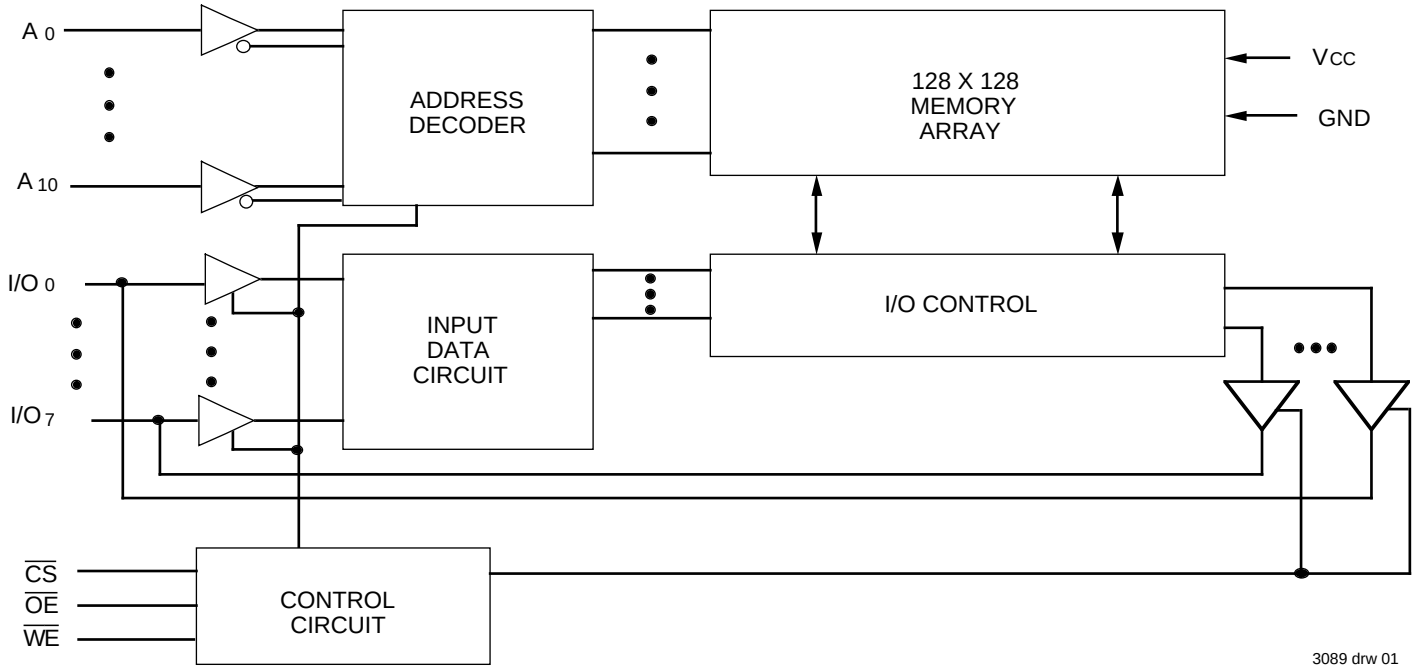
Access times as fast as 15ns are available. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, a standby power mode, as long as $\overline{CS}$ remains HIGH. This capability provides significant system level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW to 4µW operating off a 2V battery.

All inputs and outputs of the IDT6116SA/LA are TTL-compatible. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT6116SA/LA is packaged in 24-pin 600 and 300 mil plastic or ceramic DIP and a 24-lead gull-wing SOIC, and a 24 -lead J-bend SOJ providing high board-level packing densities.

Military grade product is manufactured in compliance to the latest version of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



3089 drw 01

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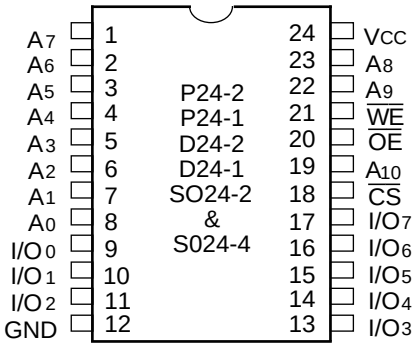
For latest information contact IDT's web site at www.idt.com or fax-on-demand at 408-492-8391.

PIN CONFIGURATIONS



3089 drw 02

DIP/SOIC/SOJ
TOP VIEW

PIN DESCRIPTIONS

A_0–A_{13}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground

3089 tbl 01

TRUTH TABLE(1)

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O
Standby	H	X	X	High-Z
Read	L	L	H	$DATA_{OUT}$
Read	L	H	H	High-Z
Write	L	X	L	$DATA_{IN}$

NOTE:
1. H = V_{IH}, L = V_{IL}, X = Don't Care.

3089 tbl 02

CAPACITANCE (T_A = +25°C, F = 1.0 MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

3089 tbl 03

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to + 7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to + 70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to + 125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to + 125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} +0.5V.

3089 tbl 04

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

3089 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5(2)	V
GND	Supply Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	V_{CC} +0.5	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTES: 3089 tbl 06

1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.
2. V_{IN} must not exceed V_{CC} +0.5V.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions		IDT6116SA Min.	IDT6116SA Max.	IDT6116LA Min.	IDT6116LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	2.4	—	V

3089 tbl 07

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Power	6116SA15(2) 6116LA15(2) Com'l.	6116SA15(2) 6116LA15(2) Mil.	6116SA20 6116LA20 Com'l.	6116SA20 6116LA20 Mil.	6116SA25 6116LA25 Com'l.	6116SA25 6116LA25 Mil.	6116SA35 6116LA35 Com'l.	6116SA35 6116LA35 Mil.	Unit
I_{CC1}	Operating Power Supply Current, $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = 0	SA	105	—	105	130	80	90	80	90	mA
		LA	95	—	95	120	75	85	75	85	
I_{CC2}	Dynamic Operating Current, $\overline{CS} \le V_{IL}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(4)	SA	150	—	130	150	120	135	100	115	mA
		LA	140	—	120	140	110	125	95	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(4)	SA	40	—	40	50	40	45	25	35	mA
		LA	35	—	35	45	35	40	25	30	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), $\overline{CS} \ge V_{HC}$, V_{CC} = Max., $V_{IN} \ge V_{HC}$ or $V_{IN} \le V_{LC}$, f = 0	SA	2	—	2	10	2	10	2	10	mA
		LA	0.1	—	0.1	0.9	0.1	0.9	0.1	0.9	

NOTES: 3089 tbl 08

1. All values are maximum guaranteed values.
2. 0°C to + 70°C temperature range only.
3. –55°C to + 125°C temperature range only.
4. f_{MAX} = 1/t_{RC}, only address inputs are cycling at f_{MAX}, f = 0 means address inputs are not changing.

DC ELECTRICAL CHARACTERISTICS (1) (Continued)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Power	6116SA45 6116LA45 Com'l.	6116SA45 6116LA45 Mil.	6116SA55(3) 6116LA55(3) Com'l.	6116SA55(3) 6116LA55(3) Mil.	6116SA70(3) 6116LA70(3) Com'l.	6116SA70(3) 6116LA70(3) Mil.	6116SA90(3) 6116LA90(3) Com'l.	6116SA90(3) 6116LA90(3) Mil.	6116SA120(3) 6116LA120(3) Com'l.	6116SA120(3) 6116LA120(3) Mil.	6116SA150(3) 6116LA150(3) Com'l.	6116SA150(3) 6116LA150(3) Mil.	Unit
I_{CC1}	Operating Power Supply Current, $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = 0	SA	80	90	—	90	—	90	—	90	—	90	—	90	mA
		LA	75	85	—	85	—	85	—	85	—	85	—	85	
I_{CC2}	Dynamic Operating Current, $\overline{CS} \le V_{IL}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(4)	SA	100	100	—	100	—	100	—	100	—	100	—	90	mA
		LA	90	95	—	90	—	90	—	85	—	85	—	85	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(4)	SA	25	25	—	25	—	25	—	25	—	25	—	25	mA
		LA	20	20	—	20	—	20	—	25	—	15	—	15	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), $\overline{CS} \ge V_{HC}$, V_{CC} = Max., $V_{IN} \ge V_{HC}$ or $V_{IN} \le V_{LC}$, f = 0	SA	2	10	—	10	—	10	—	10	—	10	—	10	mA
		LA	0.1	0.9	—	0.9	—	0.9	—	0.9	—	0.9	—	0.9	

NOTES:
3089 tbl 09

1. All values are maximum guaranteed values.
2. 0°C to + 70°C temperature range only.
3. –55°C to + 125°C temperature range only.
4. f_{MAX} = 1/t_{RC}, only address inouts are toggling at f_{MAX}, f = 0 means address inputs are not changing.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

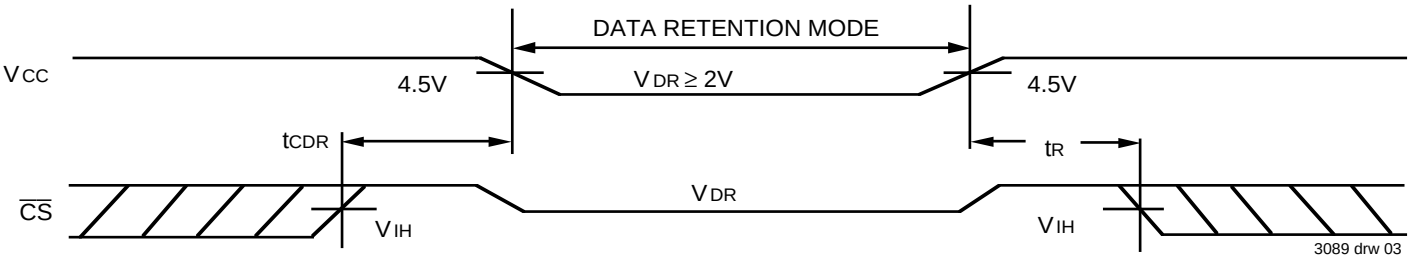
(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions		Min.	Typ.(1) Vcc 2.0V	Typ.(1) Vcc 3.0V	Max. Vcc 2.0V	Max. Vcc 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \ge V_{HC}$	MIL.	—	0.5	1.5	200	300	µA
			COM'L.	—	0.5	1.5	20	30	
t_{CDR}(3)	Data Deselect to Data Retention Time	$V_{IN} \ge V_{HC}$ or $\le V_{LC}$		—	0	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns
$\|I_{LI}\|$	Input Leakage Current			—	—	—	2	2	µA

NOTES:
3089 tbl 10

1. T_A = + 25°C
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3089 tbl 11

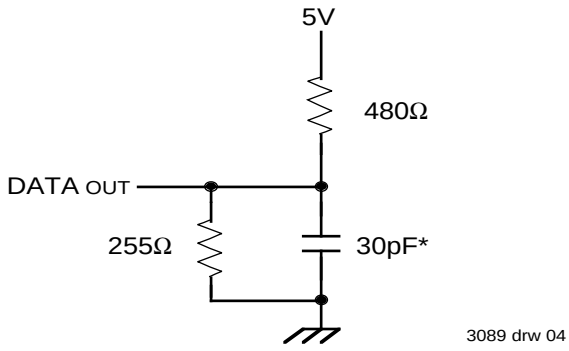


Figure 1. AC Test Load

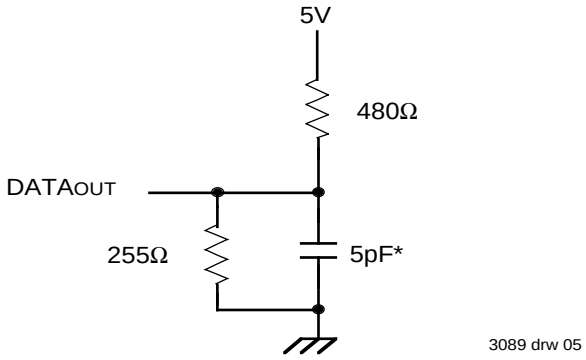


Figure 2. AC Test Load (for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ} & t_{OW})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

Symbol	Parameter	6116SA15[1] 6116LA15[1]		6116SA20 6116LA20		6116SA25 6116LA25		6116SA35 6116LA35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15	—	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	15	—	19	—	25	—	35	ns
t_{ACS}	Chip Select Access Time	—	15	—	20	—	25	—	35	ns
t_{CLZ}[3]	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	10	—	10	—	13	—	20	ns
t_{OLZ}[3]	Output Enable to Output in Low-Z	0	—	0	—	5	—	5	—	ns
t_{CHZ}[3]	Chip Deselect to Output in High-Z	—	10	—	11	—	12	—	15	ns
t_{OHZ}[3]	Output Disable to Output in High-Z	—	8	—	8	—	10	—	13	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{PU}[3]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[3]	Chip Deselect to Power-Down Time	—	15	—	20	—	25	—	35	ns

3089 tbl 12

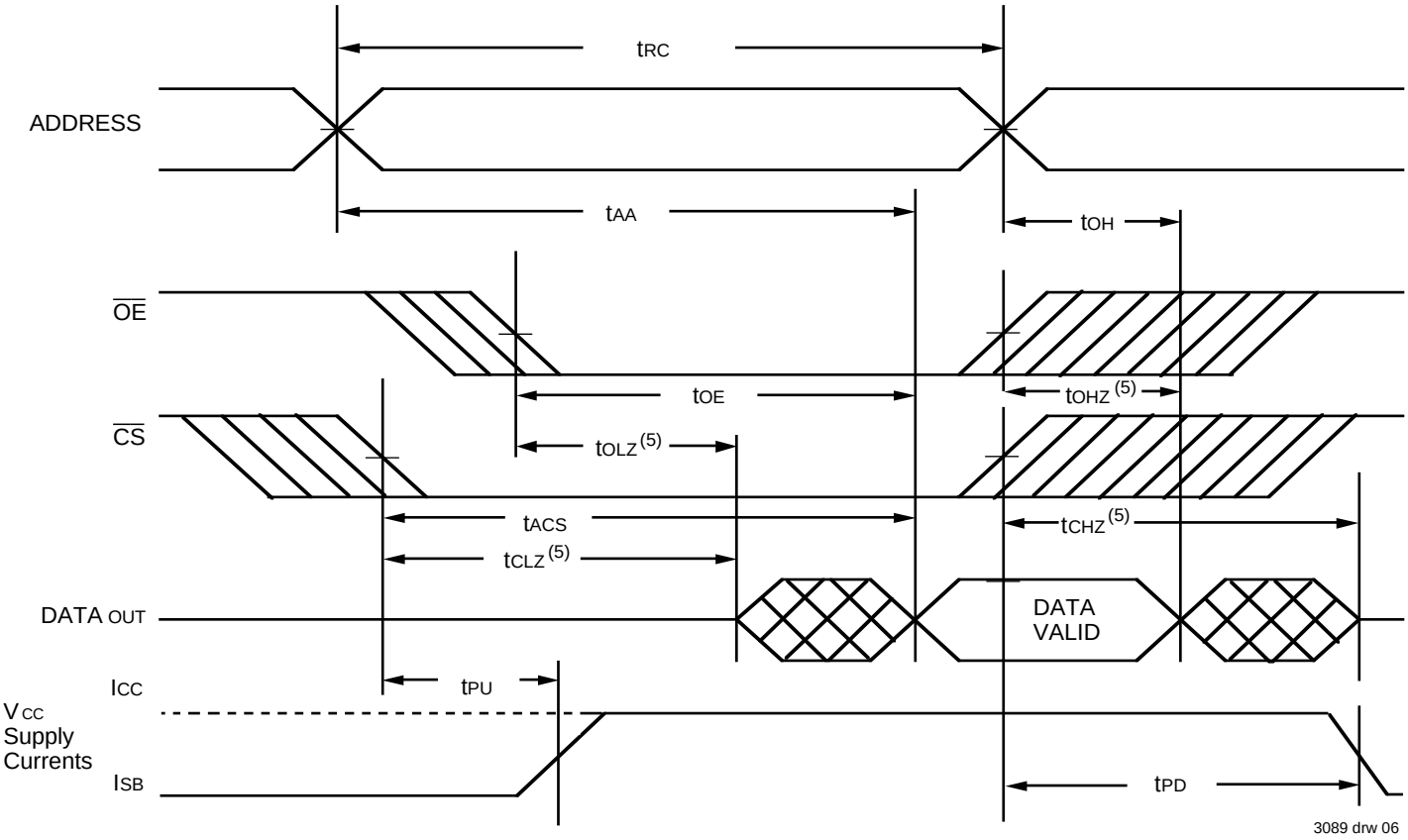
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges) (Continued)

Symbol	Parameter	6116SA45 6116LA45		6116SA55[2] 6116LA55[2]		6116SA70[2] 6116LA70[2]		6116SA90[2] 6116LA90[2]		6116SA120[2] 6116LA120[2]		6116SA150[2] 6116LA150[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{RC}	Read Cycle Time	45	—	55	—	70	—	90	—	120	—	150	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	—	90	—	120	—	150	ns
t_{ACS}	Chip Select Access Time	—	45	—	50	—	65	—	90	—	120	—	150	ns
t_{CLZ}[3]	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	25	—	40	—	50	—	60	—	80	—	100	ns
t_{OLZ}[3]	Output Enable to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[3]	Chip Deselect to Output in High-Z	—	20	—	30	—	35	—	40	—	40	—	40	ns
t_{OHZ}[3]	Output Disable to Output in High-Z	—	15	—	30	—	35	—	40	—	40	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns

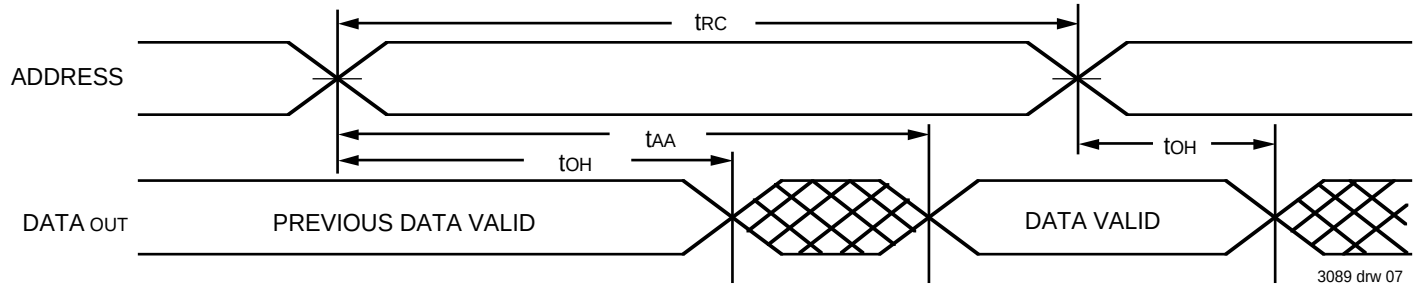
3089 tbl 13

NOTES:
1. 0°C to + 70°C temperature range only.
2. –55°C to + 125°C temperature range only.
3. This parameter guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

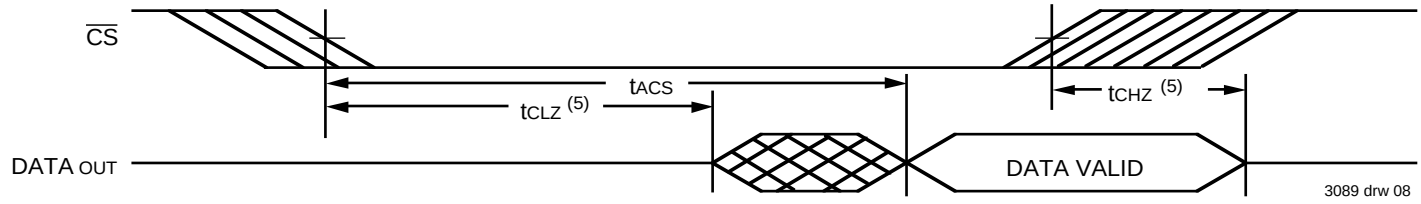
TIMING WAVEFORM OF READ CYCLE NO. 1 (1, 3)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:
1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±500mV from steady state.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

Symbol	Parameter	6116SA15[1] 6116LA15[1]		6116SA20 6116LA20		6116SA25 6116LA25		6116SA35 6116LA35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
t_{WC}	Write Cycle Time	15	—	20	—	25	—	35	—	ns
t_{CW}	Chip Select to End-of-Write	13	—	15	—	17	—	25	—	ns
t_{AW}	Address Valid to End-of-Write	14	—	15	—	17	—	25	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	12	—	15	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[3]	Write to Output in High-Z	—	7	—	8	—	16	—	20	ns
t_{DW}	Data to Write Time Overlap	12	—	12	—	13	—	15	—	ns
t_{DH}[4]	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW}[3,4]	Output Active from End-of-Write	0	—	0	—	0	—	0	—	ns

3089 tbl 14

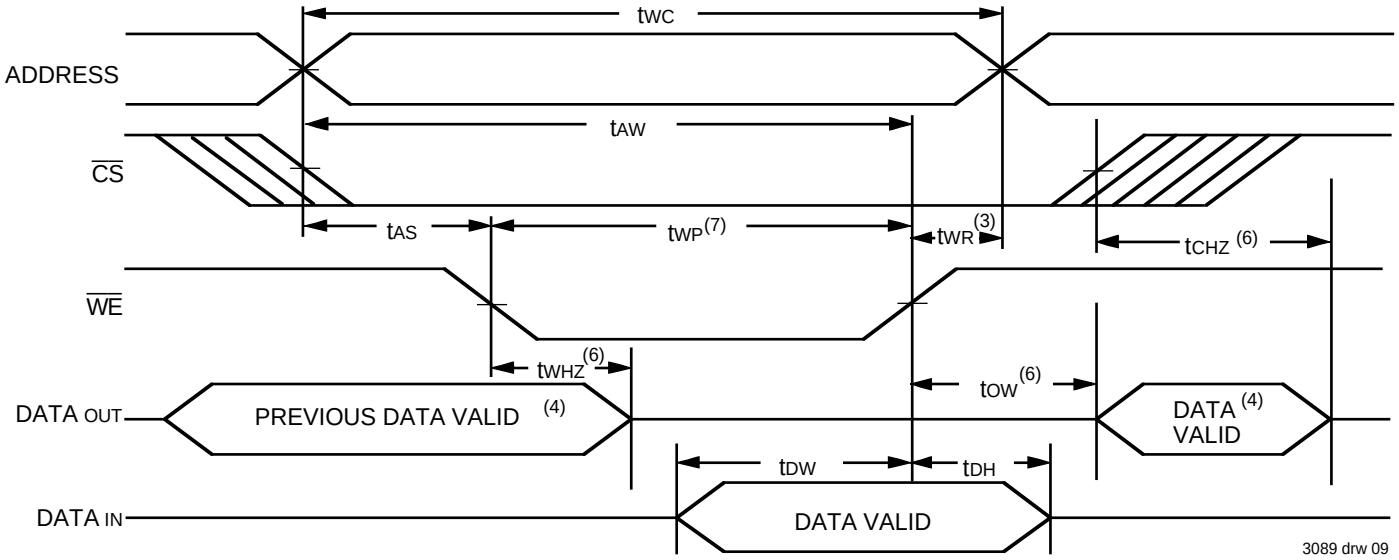
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

Symbol	Parameter	6116SA45 6116LA45		6116SA55[2] 6116LA55[2]		6116SA70[2] 6116LA70[2]		6116SA90[2] 6116LA90[2]		6116SA120[2] 6116LA120[2]		6116SA150[2] 6116LA150[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE														
t_{WC}	Write Cycle Time	45	—	55	—	70	—	90	—	120	—	150	—	ns
t_{CW}	Chip Select to End of Write	30	—	40	—	40	—	55	—	70	—	90	—	ns
t_{AW}	Address Valid to End of Write	30	—	45	—	65	—	80	—	105	—	120	—	ns
t_{AS}	Address Set-up Time	0	—	5	—	15	—	15	—	20	—	20	—	ns
t_{WP}	Write Pulse Width	25	—	40	—	40	—	55	—	70	—	90	—	ns
t_{WR}	Write Recovery Time	0	—	5	—	5	—	5	—	5	—	10	—	ns
t_{WHZ}[3]	Write to Output in High-Z	—	25	—	30	—	35	—	40	—	40	—	40	ns
t_{DW}	Data to Write Time Overlap	20	—	25	—	30	—	30	—	35	—	40	—	ns
t_{DH}[4]	Data Hold from Write Time	0	—	5	—	5	—	5	—	5	—	10	—	ns
t_{OW}[3,4]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	0	—	ns

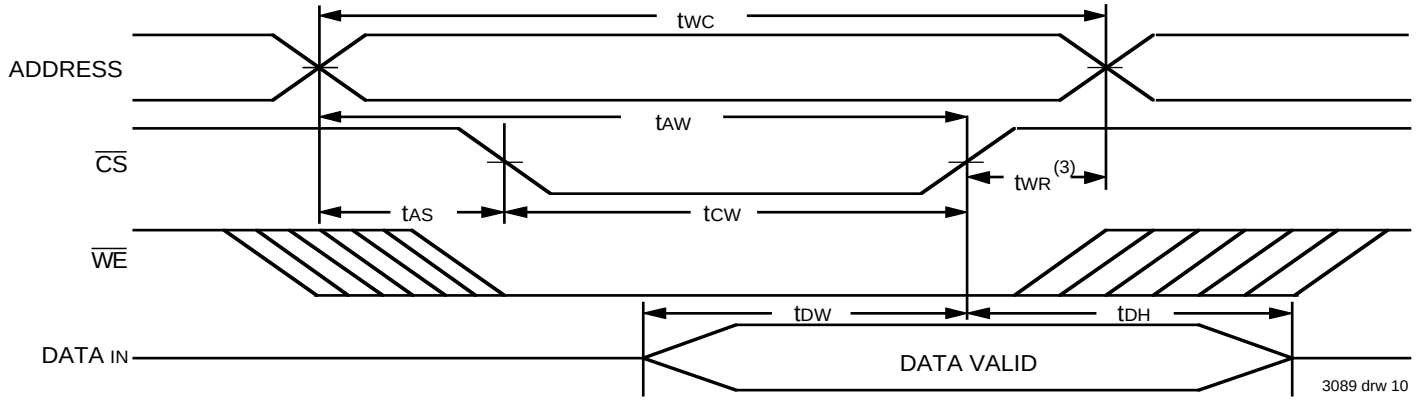
3089 tbl 15

NOTES:
1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operation conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 5, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 5, 7)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and the input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
6. Transition is measured ±500mV from steady state.
7. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse is the specified t_{WP}. For a $\overline{CS}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to t_{CW}.

ORDERING INFORMATION