

Integrated Device Technology, Inc.

## HIGH-PERFORMANCE CMOS BUS INTERFACE LATCHES

IDT54/74FCT841A/B/C

### FEATURES:

- Equivalent to AMD's Am29841-46 bipolar registers in pinout/function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT841A equivalent to FAST™ speed
- **IDT54/74FCT841B 25% faster than FAST**
- **IDT54/74FCT841C 40% faster than FAST**
- Buffered common latch enable, clear and preset inputs
- $I_{OL} = 48\text{mA}$  (commercial) and  $32\text{mA}$  (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels ( $1\text{mW}$  typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series ( $5\mu\text{A}$  max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

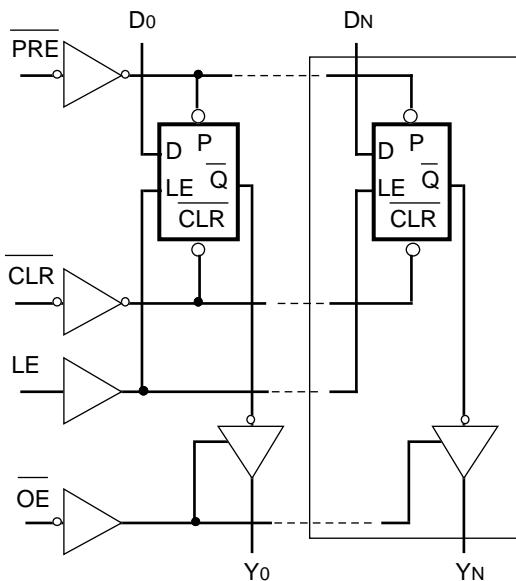
### DESCRIPTION:

The IDT54/74FCT800 series is built using an advanced dual metal CMOS technology.

The IDT54/74FCT840 series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT841 is a buffered, 10-bit wide version of the popular '373 function.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high-impedance state.

### FUNCTIONAL BLOCK DIAGRAM



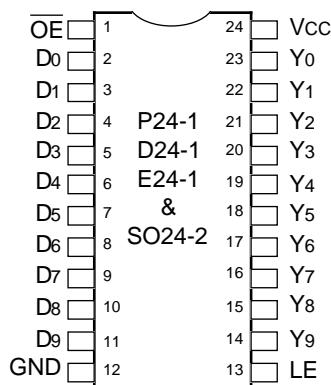
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FAST is a trademark of National Semiconductor Co.

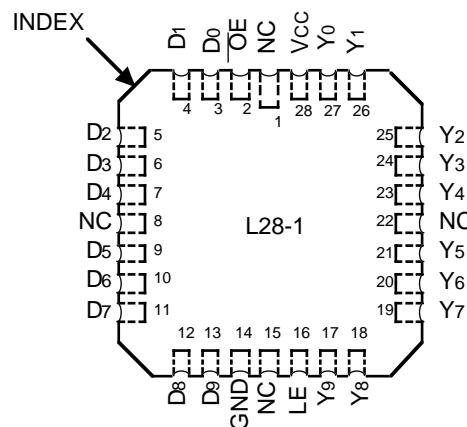
MILITARY AND COMMERCIAL TEMPERATURE RANGES

APRIL 1994

## PIN CONFIGURATIONS

DIP/CERPACk/SOIC  
TOP VIEW

2607 drw 02

LCC  
TOP VIEW

2607 drw 03

## PIN DESCRIPTION

Name	I/O	Description
CLR	I	When CLR is LOW, the outputs are LOW if OE is LOW. When CLR is HIGH, data can be entered into the latch.
DI	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
YI	O	The 3-state latch outputs.
OE	I	The output enable control. When OE is LOW, the outputs are enabled. When OE is HIGH, the outputs (YI) are in the high-impedance (off) state.
PRE	I	Preset line. When PRE is LOW, the outputs are HIGH if OE is LOW. Preset overrides CLR.

2607 tbl 01

FUNCTION TABLE<sup>(1)</sup>

Inputs						Internal	Outputs	Function
CLR	PRE	OE	LE	DI	QI	YI		
H	H	H	X	X	X	Z	High Z	
H	H	H	H	L	L	Z	High Z	
H	H	H	H	H	H	Z	High Z	
H	H	H	L	X	NC	Z	Latched (High Z)	
H	H	L	H	L	L	L	Transparent	
H	H	L	H	H	H	H	Transparent	
H	H	L	L	X	NC	NC	Latched	
H	L	L	X	X	H	H	Preset	
L	H	L	X	X	L	L	Clear	
L	L	L	X	X	H	H	Preset	
L	H	H	L	X	L	Z	Latched (High Z)	
H	L	H	L	X	H	Z	Latched (High Z)	

NOTE:

2607 tbl 02

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change,  
Z = High Impedance

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Commercial	Military	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to Vcc	-0.5 to Vcc	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

**NOTE:**

2607 tbl 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
- Input and Vcc terminals only.
- Outputs and I/O terminals only.

2607 tbl 04

1. This parameter is measured at characterization but not tested.

**CAPACITANCE (TA = +25°C, f = 1.0MHz)**

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
COUT	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Following Conditions Apply Unless Otherwise Specified: VLC = 0.2V; VHC = Vcc - 0.2V

Commercial: TA = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: TA = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
VIH	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
VIL	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
IIH	Input HIGH Current	Vcc = Max.	Vi = Vcc	—	—	5	µA
			Vi = 2.7V	—	—	5 <sup>(4)</sup>	
			Vi = 0.5V	—	—	-5 <sup>(4)</sup>	
			Vi = GND	—	—	-5	
IIL	Input LOW Current	Vcc = Max.	Vo = Vcc	—	—	10	µA
			Vo = 2.7V	—	—	10 <sup>(4)</sup>	
			Vo = 0.5V	—	—	-10 <sup>(4)</sup>	
			Vo = GND	—	—	-10	
IOZH	Off State (High Impedance) Output Current	Vcc = Max.	Vo = Vcc	—	—	10	µA
IOZL			Vo = 2.7V	—	—	10 <sup>(4)</sup>	
VIK	Clamp Diode Voltage	Vcc = Min., IN = -18mA		—	-0.7	-1.2	V
Ios	Short Circuit Current	Vcc = Max. <sup>(3)</sup> , Vo = GND		-75	-120	—	mA
VOH	Output HIGH Voltage	Vcc = 3V, VIN = VLC or VHC, IOH = -32µA	VHC	VCC	—	—	V
		Vcc = Min. VIN = VIH or VIL	IOH = -300µA	VHC	VCC	—	
			IOH = -15mA MIL.	2.4	4.3	—	
			IOH = -24mA COM'L.	2.4	4.3	—	
VOL	Output LOW Voltage	Vcc = 3V, VIN = VLC or VHC, IOL = 300µA	—	GND	VLC	—	V
		Vcc = Min. VIN = VIH or VIL	IOL = 300µA	—	GND	VLC <sup>(4)</sup>	
			IOL = 32mA MIL.	—	0.3	0.5	
			IOL = 48mA COM'L.	—	0.3	0.5	

**NOTES:**

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.

2607 tbl 05

**POWER SUPPLY CHARACTERISTICS**

VLC = 0.2V; VHC = Vcc – 0.2V

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max. V <sub>IN</sub> ≥ V <sub>H</sub> C; V <sub>IN</sub> ≤ V <sub>L</sub> C		—	0.2	1.5	mA
ΔI <sub>CC</sub>	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max. V <sub>IN</sub> = 3.4V <sup>(3)</sup>		—	0.5	2.0	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup>	V <sub>CC</sub> = Max. Outputs Open OĒ = GND LE = V <sub>CC</sub> One Input Toggling 50% Duty Cycle	V <sub>IN</sub> ≥ V <sub>H</sub> C V <sub>IN</sub> ≤ V <sub>L</sub> C	—	0.15	0.25	mA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max. Outputs Open f <sub>i</sub> = 10MHz 50% Duty Cycle OĒ = GND LE = V <sub>CC</sub> One Bit Toggling	V <sub>IN</sub> ≥ V <sub>H</sub> C V <sub>IN</sub> ≤ V <sub>L</sub> C (FCT)	—	1.7	4.0	mA
		V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	2.0	5.0		
		V <sub>IN</sub> ≥ V <sub>H</sub> C V <sub>IN</sub> ≤ V <sub>L</sub> C (FCT)	—	3.2	6.5 <sup>(5)</sup>		
		V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	5.2	14.5 <sup>(5)</sup>		

**NOTES:**

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient.3. Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.

4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

5. Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.6. I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>

$$I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I<sub>CC</sub> = Quiescent CurrentΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)D<sub>H</sub> = Duty Cycle for TTL Inputs HighN<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)f<sub>i</sub> = Input FrequencyN<sub>i</sub> = Number of Inputs at f<sub>i</sub>

All currents are in millamps and all frequencies are in megahertz.

2607 tbl 06

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions <sup>(1)</sup>	FCT841A				FCT841B				FCT841C				Unit	
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.			
			Min. <sup>(2)</sup>	Max.												
tPLH tPHL	Propagation Delay DI to YI (LE = HIGH)	CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns	
		CL = 300pF <sup>(4)</sup> RL = 500Ω	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0		
tPLH tPHL	Propagation Delay LE to YI	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	10.5	1.5	6.4	1.5	6.8	ns	
		CL = 300pF <sup>(4)</sup> RL = 500Ω	1.5	16.0	1.5	20.0	1.5	15.5	1.5	18.0	1.5	15.0	1.5	16.0		
tPLH	Propagation Delay, $\overline{PRE}$ to YI	CL = 50pF RL = 500Ω	1.5	12.0	1.5	14.0	1.5	8.0	1.5	10.0	1.5	7.0	1.5	9.0	ns	
tPHL			1.5	14.0	1.5	17.0	1.5	10.0	1.5	13.0	1.5	9.0	1.5	12.0		
tPHL	Propagation Delay, $\overline{CLR}$ to YI		1.5	13.0	1.5	14.0	1.5	10.0	1.5	11.0	1.5	9.0	1.5	10.0	ns	
tPLH			1.5	14.0	1.5	17.0	1.5	10.0	1.5	10.0	1.5	9.0	1.5	9.0		
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI	CL = 50pF RL = 500Ω	1.5	11.5	1.5	13.0	1.5	8.0	1.5	8.5	1.5	6.5	1.5	7.3	ns	
		CL = 300pF <sup>(4)</sup> RL = 500Ω	1.5	23.0	1.5	25.0	1.5	14.0	1.5	15.0	1.5	12.0	1.5	13.0		
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to YI	CL = 5pF <sup>(4)</sup> RL = 500Ω	1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	1.5	5.7	1.5	6.0	ns	
		CL = 50pF RL = 500Ω	1.5	8.0	1.5	10.0	1.5	7.0	1.5	7.5	1.5	6.0	1.5	6.3		
tsU	Data to LE Set-up Time	CL = 50pF RL = 500Ω	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns	
tH	Data to LE Hold Time		2.5	—	3.0	—	2.5	—	2.5	—	2.5	—	2.5	—	ns	
tw	LE Pulse Width <sup>(3)</sup>		4.0	—	5.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns	
tw	$\overline{PRE}$ Pulse Width <sup>(3)</sup>		5.0	—	7.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns	
tw	CLR Pulse Width <sup>(3)</sup>		4.0	—	5.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns	
tREM	Recovery Time $\overline{PRE}$ to LE		4.0	—	4.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns	
tREM	Recovery Time CLR to LE		3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns	

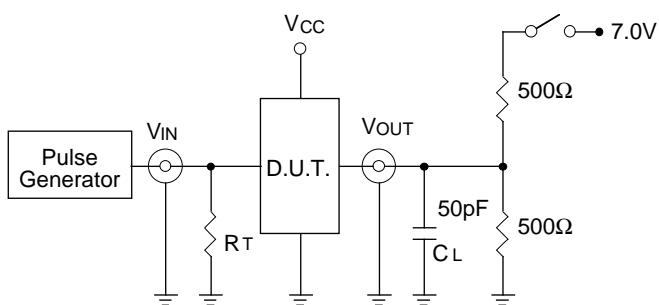
## NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.
4. These conditions are guaranteed but not tested.

2607 tbl 07

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



### SWITCH POSITION

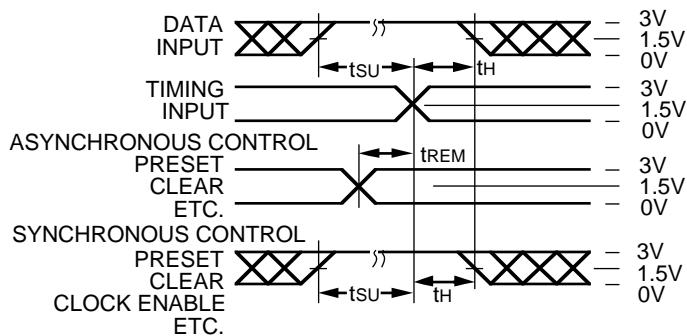
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

#### DEFINITIONS:

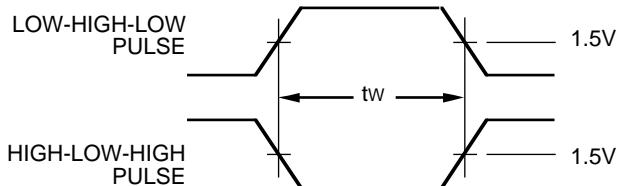
2607 tbl 08

 $C_L$  = Load capacitance: includes jig and probe capacitance. $R_T$  = Termination resistance: should be equal to  $Z_{out}$  of the Pulse Generator.

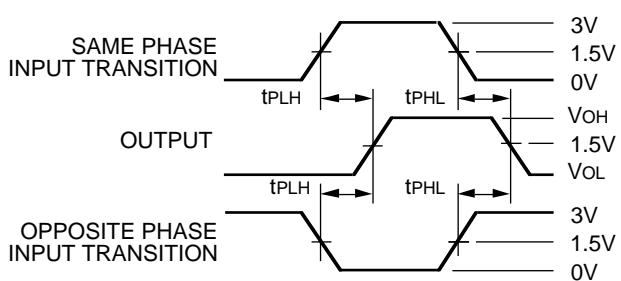
### SET-UP, HOLD AND RELEASE TIMES



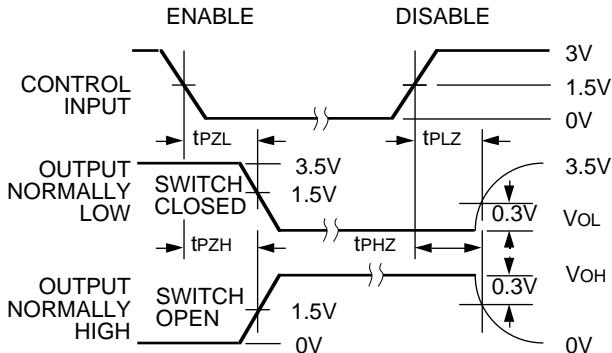
### PULSE WIDTH



### PROPAGATION DELAY



### ENABLE AND DISABLE TIMES

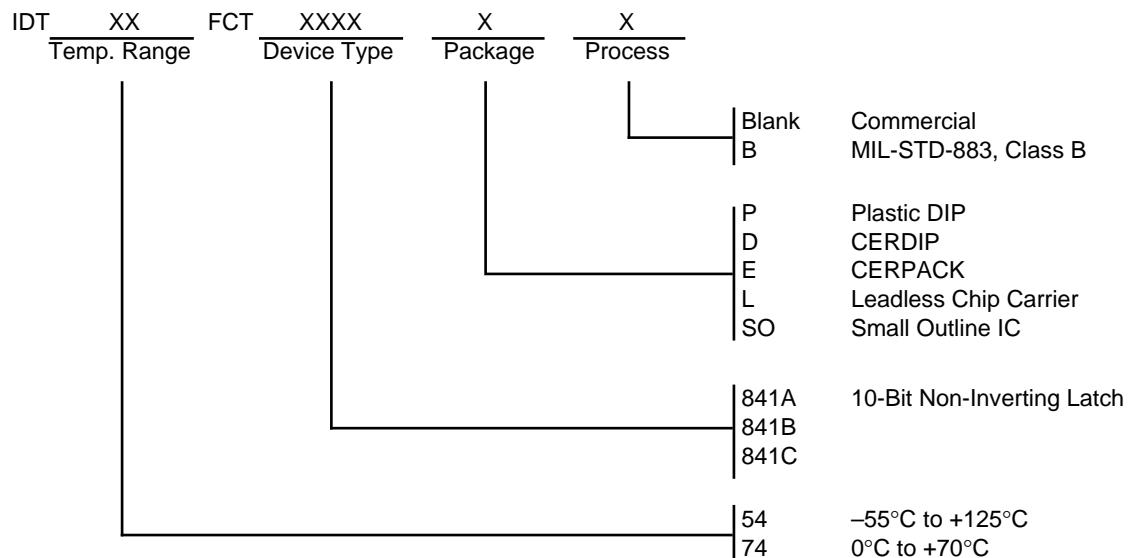


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#### NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_f \leq 2.5\text{ns}$ ;  $t_r \leq 2.5\text{ns}$

## ORDERING INFORMATION



2607 drw 05