



Integrated Device Technology, Inc.

FAST CMOS OCTAL BUFFER/LINE DRIVER

IDT54/74FCT240/A/C
IDT54/74FCT241/A/C
IDT54/74FCT244/A/C
IDT54/74FCT540/A/C
IDT54/74FCT541/A/C

FEATURES:

- IDT54/74FCT240/241/244/540/541 equivalent to FAST™ speed and drive
- **IDT54/74FCT240A/241A/244A/540A/541A 25% faster than FAST**
- **IDT54/74FCT240C/241C/244C/540C/541C up to 55% faster than FAST**
- $I_{OL} = 64\text{mA}$ (commercial) and 48mA (military)
- CMOS power levels (1mW typ. static)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Meets or exceeds JEDEC Standard 18 specifications

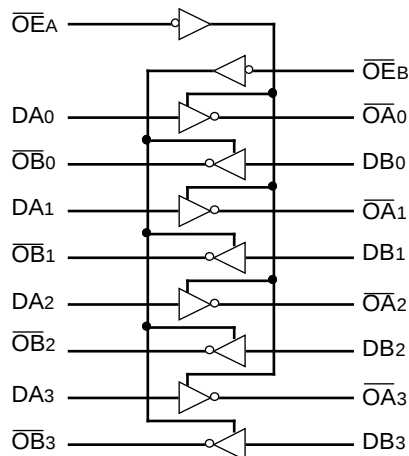
DESCRIPTION:

The IDT octal buffer/line drivers are built using an advanced dual metal CMOS technology. The IDT54/74FCT240/A/C, IDT54/74FCT241/A/C and IDT54/74FCT244/A/C are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitter/receivers which provide improved board density.

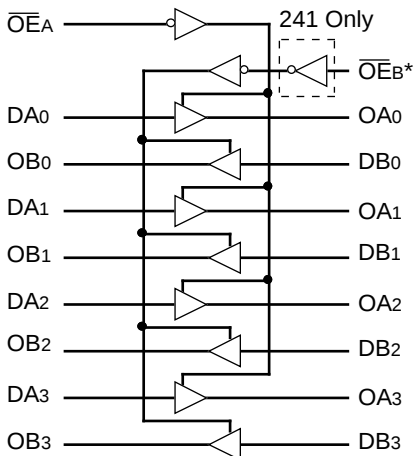
The IDT54/74FCT540/A/C and IDT54/74FCT541/A/C are similar in function to the IDT54/74FCT240/A/C and IDT54/74FCT244/A/C, respectively, except that the inputs and outputs are on opposite sides of the package. This pinout arrangement makes these devices especially useful as output ports for microprocessors and as backplane drivers, allowing ease of layout and greater board density.

FUNCTIONAL BLOCK DIAGRAMS

2529 cnv* 01-03

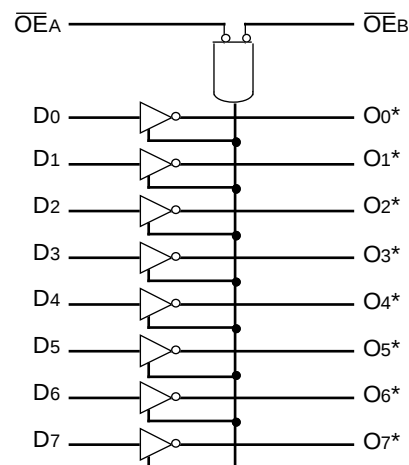


IDT54/74FCT240



IDT54/74FCT241/244

*OEb for 241, OEb for 244



IDT54/74FCT540/541

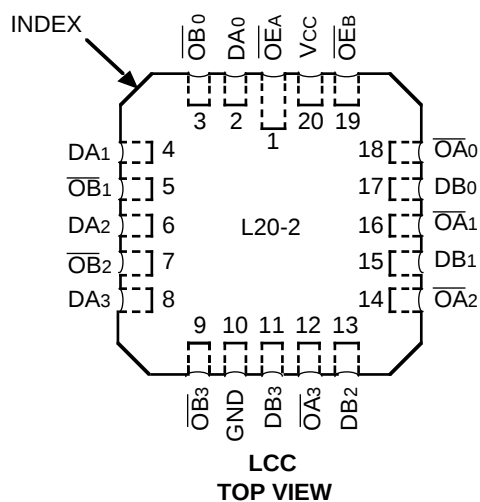
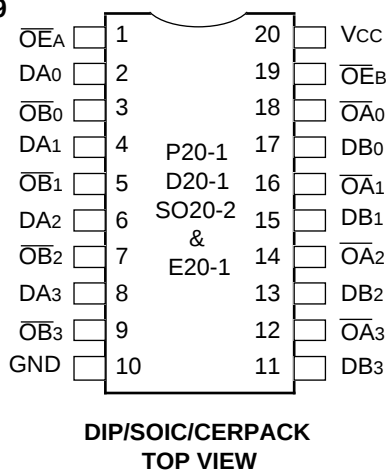
*Logic diagram shown for 'FCT540.
'FCT541 is the non-inverting option.

2606 dwg 01-03

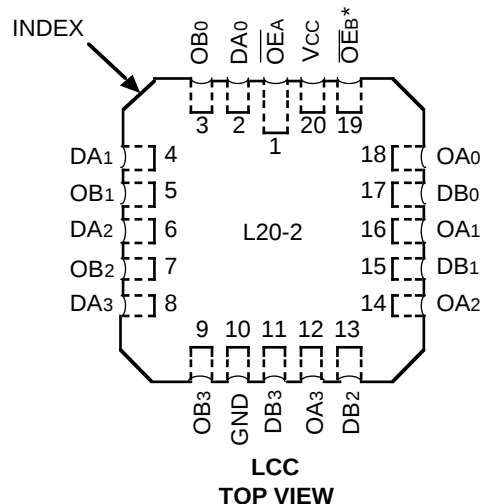
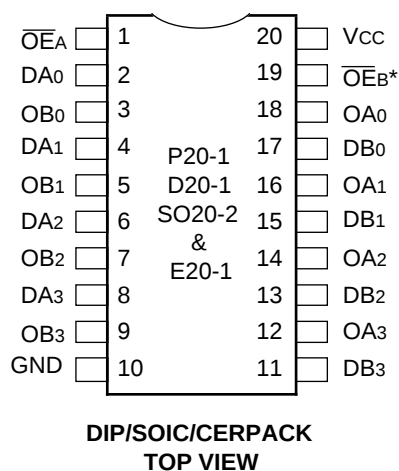
PIN CONFIGURATIONS

IDT54/74FCT240

2529 cnv* 04-09

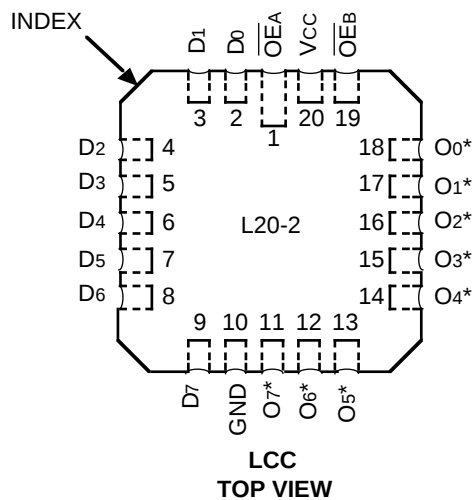
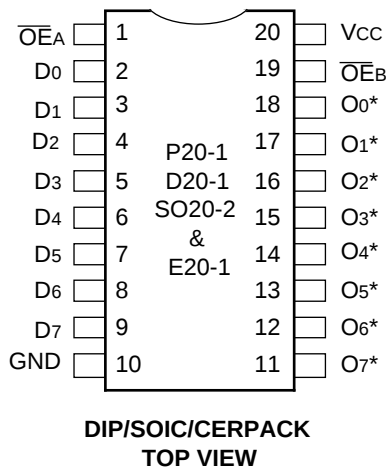


IDT54/74FCT241/244



* $\overline{OE}_B$ for 241, $\overline{OE}_B$ for 244

IDT54/74FCT540/541



* $\overline{O}_x$ for 540, O_x for 541

2606 cnv* 04-09

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A, \overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
$OE_B^{(1)}$	3-State Output Enable Input (Active HIGH)
Dxx	Inputs
Oxx	Outputs

NOTE:

1. OE_B for 241 only.

2606 tbl 04

FUNCTION TABLE

Inputs ⁽¹⁾				Outputs ⁽¹⁾				
$\overline{OE}_A$	$\overline{OE}_B$	$OE_B^{(2)}$	D	240	241	244	540	541
L	L	H	L	H	L	L	H	L
L	L	H	H	L	H	H	L	H
H	H	L	X	Z	Z	Z	Z	Z

NOTES:

1. H = High Voltage Level
X = Don't Care
L = Low Voltage Level
Z = High Impedance
2. OE_B for 241 only.

2606 tbl 05

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

2606 tbl 01

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

2606 tbl 02

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Commercial: $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55^\circ C$ to $+125^\circ C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	5	μA
			$V_I = 2.7V$	—	—	5 ⁽⁴⁾	
I_{IL}	Input LOW Current		$V_I = 0.5V$	—	—	-5 ⁽⁴⁾	
			$V_I = GND$	—	—	-5	
I_{OZH}	Off State (High Impedance) Output Current	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$	—	—	10	μA
			$V_O = 2.7V$	—	—	10 ⁽⁴⁾	
I_{OZL}			$V_O = 0.5V$	—	—	-10 ⁽⁴⁾	
			$V_O = GND$	—	—	-10	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_N = -18mA$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$ ⁽³⁾ , $V_O = GND$		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = 3V$, $V_{IN} = V_{LC}$ or V_{HC} , $I_{OH} = -32\mu A$		V_{HC}	V_{CC}	—	V
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -300\mu A$	V_{HC}	V_{CC}	—	
			$I_{OH} = -12mA \text{ MIL.}$	2.4	4.3	—	
			$I_{OH} = -15mA \text{ COM'L.}$	2.4	4.3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 3V$, $V_{IN} = V_{LC}$ or V_{HC} , $I_{OL} = 300\mu A$		—	GND	V_{LC}	V
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 300\mu A$	—	GND	V_{LC} ⁽⁴⁾	
			$I_{OL} = 48mA \text{ MIL.}$	—	0.3	0.55	
			$I_{OL} = 64mA \text{ COM'L.}$	—	0.3	0.55	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.

2606 tbl 03

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE}_A = \overline{OE}_B = \text{GND}$ or $\overline{OE}_A = \text{GND}$, $OE_B = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B = \text{GND}$ or $\overline{OE}_A = \text{GND}$, $OE_B = V_{CC}$ One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2.0	5.0	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 5\text{MHz}$ 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B = \text{GND}$ or $\overline{OE}_A = \text{GND}$, $OE_B = V_{CC}$ Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	5.2	14.5 ⁽⁵⁾	

NOTES:

2606 tbl 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
All currents are in milliamperes and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT240^(1,2)

Symbol	Parameter	Condition	54/74FCT240				54/74FCT240A				54/74FCT240C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay DN to $\overline{\text{ON}}$	CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.7	ns
tPZH tPZL	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns

2606 tbl 07

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT241 AND FCT244^(1,2)

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT241 AND FCT244^(1,2)

Symbol	Parameter	Condition	54/74FCT241/244				54/74FCT241A/244A				54/74FCT241C/244C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay DN to ON	CL = 50pF RL = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	1.5	4.1	1.5	4.6	ns
tPZH tPZL	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns

2606 tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT540 AND FCT541^(1,2)

Symbol	Parameter	Condition	54/74FCT540/541				54/74FCT540A/541A				54/74FCT540C/541C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay DN to $\overline{\text{ON}}$ IDT54/74FCT540	CL = 50pF RL = 500Ω	1.5	8.5	1.5	9.5	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.7	ns
tPLH tPHL	Propagation Delay DN to ON IDT54/74FCT541		1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	1.5	4.1	1.5	4.6	ns
tPZH tPZL	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns

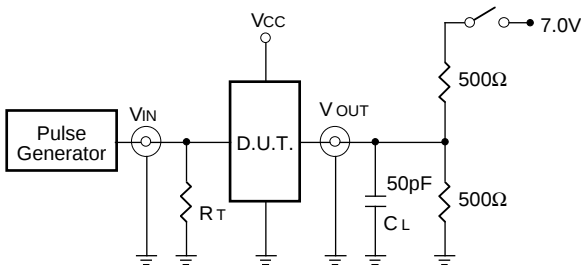
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2606 tbl 09

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS

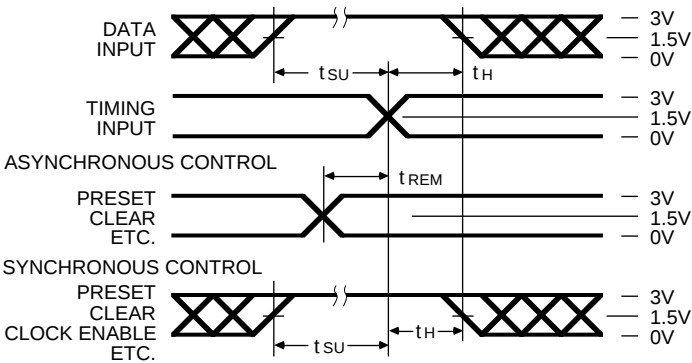


SWITCH POSITION

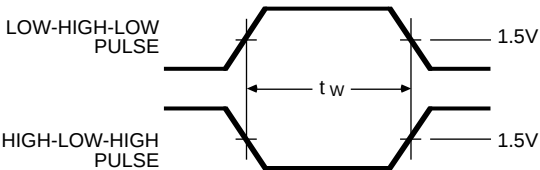
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS: 2606 tbl 10
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

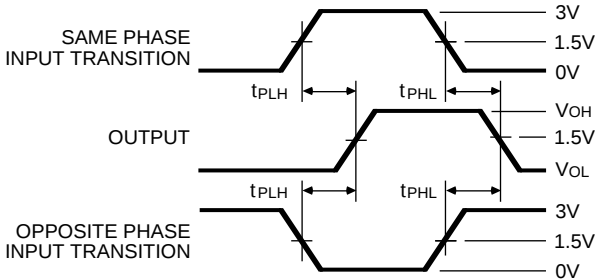
SET-UP, HOLD AND RELEASE TIMES



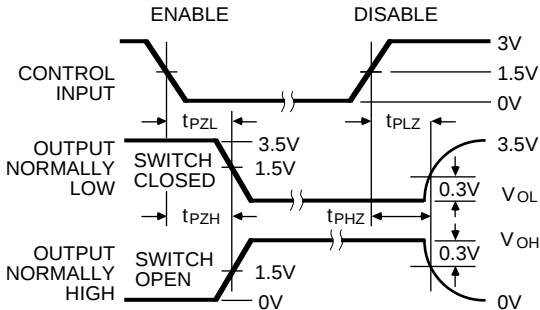
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES 2606 drw 10
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; tr ≤ 2.5ns; tr ≤ 2.5ns.

ORDERING INFORMATION

IDT	XX	FCT	XXXX	X	X		
Temp. Range		Device Type		Package	Process		
						Blank	Commercial
						B	MIL-STD-883, Class B
						P	Plastic DIP
						D	CERDIP
						SO	Small Outline IC
						L	Leadless Chip Carrier
						E	CERPACK
						240	Inverting Octal Buffer/Line Driver
						241	Non-Inverting Octal Buffer/Line Driver
						244	Non-Inverting Octal Buffer/Line Driver
						540	Inverting Octal Buffer/Line Driver
						541	Non-Inverting Octal Buffer/Line Driver
						240A	Fast Inverting Octal Buffer/Line Driver
						241A	Fast Non-Inverting Octal Buffer/Line Driver
						244A	Fast Non-Inverting Octal Buffer/Line Driver
						540A	Fast Inverting Octal Buffer/Line Driver
						541A	Fast Non-Inverting Octal Buffer/Line Driver
						240C	Super Fast Inverting Octal Buffer/Line Driver
						241C	Super Fast Non-Inverting Octal Buffer/Line Driver
						244C	Super Fast Non-Inverting Octal Buffer/Line Driver
						540C	Super Fast Inverting Octal Buffer/Line Driver
						541C	Super Fast Non-Inverting Octal Buffer/Line Driver
						54	−55°C to +125°C
						74	0°C to +70°C

2606 cnv* 15