Military & Space Products

128K x 8 STATIC RAM—SOI HX6228

FEATURES

RADIATION

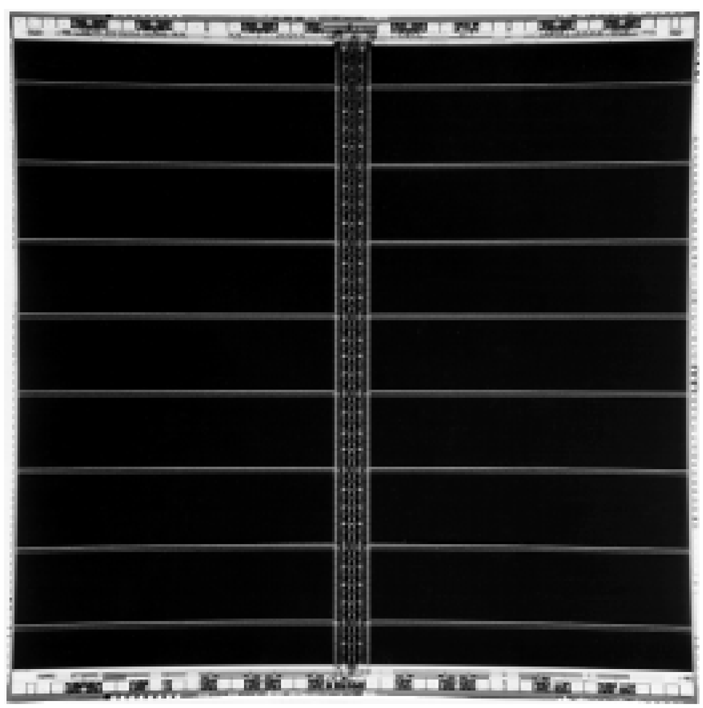
- Fabricated with RICMOS™ IV Silicon on Insulator (SOI) 0.7 µm Process (L_{eff} = 0.55 µm)
- Total Dose Hardness through 1x10^6 rad(SiO_2)
- Neutron Hardness through 1x10^{14} cm^{-2}
- Dynamic and Static Transient Upset Hardness through 1x10^{11} rad (Si)/s
- Dose Rate Survivability through <1x10^{12} rad(Si)/s
- Soft Error Rate of <1x10^{-10} upsets/bit-day in Geosynchronous Orbit
- No Latchup

OTHER

- Read/Write Cycle Times
  ≤ 16 ns (Typical)
  ≤ 25 ns (-55 to 125°C)
- Typical Operating Power <25 mW/MHz
- Asynchronous Operation
- CMOS or TTL Compatible I/O
- Single 5 V ± 10% Power Supply
- Packaging Options
  - 32-Lead Flat Pack (0.820 in. x 0.600 in.)
  - 40-Lead Flat Pack (0.775 in. x 0.710 in.)

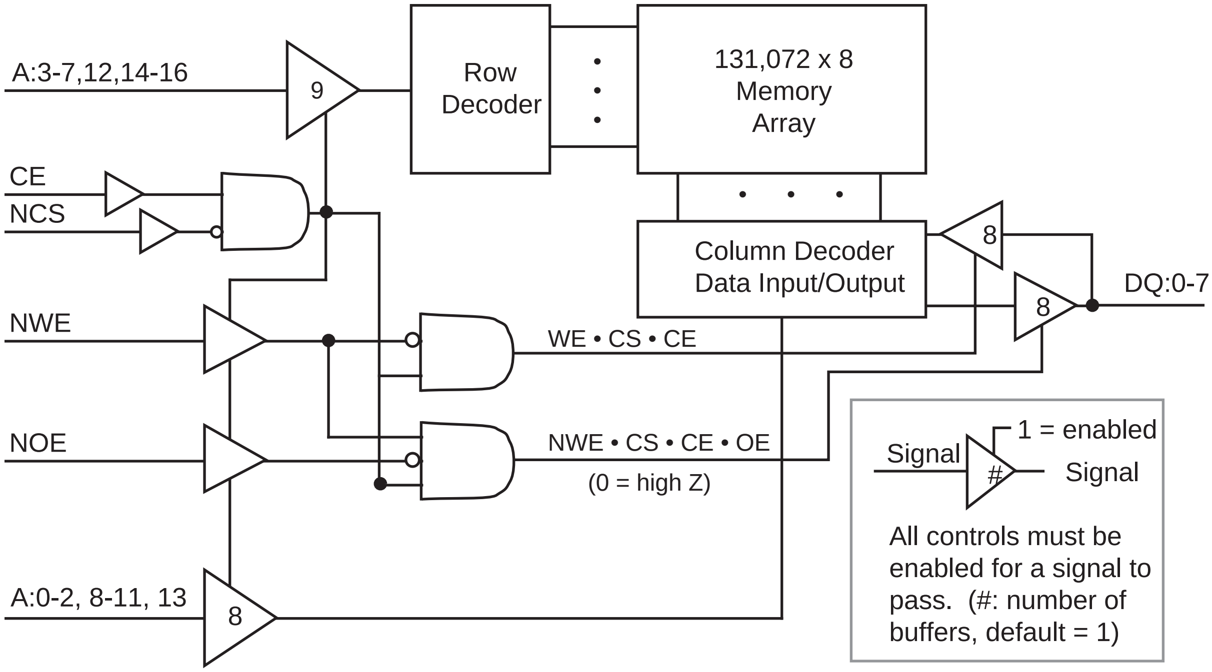
GENERAL DESCRIPTION

The 128K x 8 Radiation Hardened Static RAM is a high performance 131,072 word x 8-bit static random access memory with industry-standard functionality. It is fabricated with Honeywell's radiation hardened technology, and is designed for use in systems operating in radiation environments. The RAM operates over the full military temperature range and requires only a single 5 V ± 10% power supply. The RAM is wire bond programmable for either TTL or CMOS compatible I/O. Power consumption is typically less than 25 mW/MHz in operation, and less than 5 mW in the low power disabled mode. The RAM read operation is fully asynchronous, with an associated typical access time of 15 ns at 5V.



Honeywell's enhancedSOI RICMOS™ IV (Radiation Insensitive CMOS) technology is radiation hardened through the use of advanced and proprietary design, layout and process hardening techniques. The RICMOS™ IV process is an advanced 5-volt, SIMOX CMOS technology with a 150 Å gate oxide and a minimum feature size of 0.7 µm (0.55 µm effective gate length—L_{eff}). Additional features include Honeywell's proprietary SHARP planarization process, and a lightly doped drain (LDD) structure for improved short channel reliability. A 7 transistor (7T) memory cell is used for superior single event upset hardening, while three layer metal power bussing and the low collection volume SIMOX substrate provide improved dose rate hardening.

FUNCTIONAL DIAGRAM



SIGNAL DEFINITIONS

A: 0-16 — Address input pins which select a particular eight-bit word within the memory array.

DQ: 0-7 — Bidirectional data pins which serve as data outputs during a read operation and as data inputs during a write operation.

NCS — Not chip select, when at a low level allows normal operation. When at a high level NCS forces the SRAM to a precharge condition, holds the data output drivers in a high impedance state and disables all the input buffers except CE. If this signal is not used it must be connected to VSS.

NWE — Negative write enable, when at a low level activates a write operation and holds the data output drivers in a high impedance state. When at a high level NWE allows normal read operation.

NOE — Negative output enable, when at a high level holds the data output drivers in a high impedance state. When at a low level, the data output driver state is defined by NCS, NWE and CE. If this signal is not used it must be connected to VSS.

CE — Chip enable, when at a high level allows normal operation. When at a low level CE forces the SRAM to a precharge condition, holds the data output drivers in a high impedance state and disables all the input buffers except the NCS input buffer. If this signal is not used it must be connected to VDD.

TRUTH TABLE

CE	NCS	NWE	NOE	MODE	DQ
H	L	H	L	Read	Data Out
H	L	L	X	Write	Data In
X	H	XX	XX	Deselected	High Z
L	X	XX	XX	Disabled	High Z

Notes:
X: VI=VIH or VIL
XX: VSS≤VI≤VDD
NOE=H: High Z output state maintained for NCS=X, CE=X, NWE=X

RADIATION CHARACTERISTICS

Total Ionizing Radiation Dose

The SRAM will meet all stated functional and electrical specifications over the entire operating temperature range after the specified total ionizing radiation dose. All electrical and timing performance parameters will remain within specifications after rebound at VDD = 5.5 V and T =125°C extrapolated to ten years of operation. Total dose hardness is assured by wafer level testing of process monitor transistors and RAM product using 10 KeV X-ray and Co60 radiation sources. Transistor gate threshold shift correlations have been made between 10 KeV X-rays applied at a dose rate of $1x10^5$ rad(SiO_2)/min at T = 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

Transient Pulse Ionizing Radiation

The SRAM is capable of writing, reading, and retaining stored data during and after exposure to a transient ionizing radiation pulse up to the specified transient dost rate upset specification, when applied under recommended operating conditions. To ensure validity of all specified performance parameters before, during, and after radiation (timing degradation during transient pulse radiation is ≤20%), it is suggested that stiffening capacitance be placed on or near the package VDD and VSS, with a maximum inductance between the package (chip) and stiffening capacitance of 0.7 nH per part. If there are no operate-through or valid stored data requirements, typical circuit board mounted de-coupling capacitors are recommended.

The SRAM will meet any functional or electrical specification after exposure to a radiation pulse up to the transient dose survivability specification, when applied under recommended operating conditions. Note that the current conducted during the pulse by the RAM inputs, outputs, and power supply may significantly exceed the normal operating levels. The application design must accommodate these effects.

Neutron Radiation

The SRAM will meet any functional or timing specification after exposure to the specified neutron fluence under recommended operating or storage conditions. This assumes an equivalent neutron energy of 1 MeV.

Soft Error Rate

The SRAM is capable of meeting the specified Soft Error Rate (SER), under recommended operating conditions. This hardness level is defined by the Adams 90% worst case cosmic ray environment for geosynchronous orbits.

Latchup

The SRAM will not latch up due to any of the above radiation exposure conditions when applied under recommended operating conditions. Fabrication with the SIMOX substrate material provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures. Sufficient transistor body tie connections to the p- and n-channel substrates are made to ensure no source/drain snapback occurs.

RADIATION HARDNESS RATINGS (1)

Parameter	Limits (2)	Units	Test Conditions
Total Dose	$\geq 1x10^6$	rad(SiO_2)	T_A=25°C
Transient Dose Rate Upset (3)	$\geq 1x10^{11}$	rad(Si)/s	Pulse width ≤1 µs
Transient Dose Rate Survivability	$\geq 1x10^{12}$	rad(Si)/s	Pulse width ≤50 ns, X-ray, VDD=6.0 V, T_A=25°C
Soft Error Rate	$<1x10^{-10}$	upsets/bit-day	T_A=125°C, Adams 90% worst case environment
Neutron Fluence	$\geq 1x10^{14}$	N/cm^2	1 MeV equivalent energy, Unbiased, T_A=25°C

(1) Device will not latch up due to any of the specified radiation exposure conditions.
(2) Operating conditions (unless otherwise specified): VDD=4.5 V to 5.5 V, -55°C to 125°C.
(3) Applies to 40-lead flat pack only. Assume $\geq 1x100^9$ rad(Si))/s for 32-lead flat pack. Stiffening capacitance is suggested for optimum expected dose rate upset performance as stated above.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating		Units
		Min	Max	
VDD	Supply Voltage Range (2)	-0.5	6.5	V
VPIN	Voltage on Any Pin (2)	-0.5	VDD+0.5	V
TSTORE	Storage Temperature (Zero Bias)	-65	150	°C
TSOLDER	Soldering Temperature (5 Seconds)		270	°C
PD	Maximum Power Power Dissipation (3)		2.5	W
IOUT	DC or Average Output Current		25	mA
VPROT	ESD Input Protection Voltage (4)	1500		V
ΘJC	Thermal Resistance (Jct-to-Case)		2	°C/W
TJ	Junction Temperature		175	°C

(1) Stresses in excess of those listed above may result in permanent damage. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Voltage referenced to VSS.
(3) RAM power dissipation (IDDSB + IDDOP) plus RAM output driver power dissipation due to external loading must not exceed this specification.
(4) Class 1 electrostatic discharge (ESD) input protection. Tested per MIL-STD-883, Method 3015 by DESC certified lab.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Description			Units
		Min	Typ	Max	
VDD	Supply Voltage (referenced to VSS)	4.5	5.0	5.5	V
TA	Ambient Temperature	-55	25	125	°C
VPIN	Voltage on Any Pin (referenced to VSS)	-0.3		VDD+0.3	V

CAPACITANCE (1)

Symbol	Parameter	Typical	Worst Case		Units	Test Conditions
			Min	Max		
CI	Input Capacitance	6		7	pF	VI=VDD or VSS, f=1 MHz
CO	Output Capacitance	8		9	pF	VIO=VDD or VSS, f=1 MHz

(1) This parameter is tested during initial design characterization only.

DATA RETENTION CHARACTERISTICS

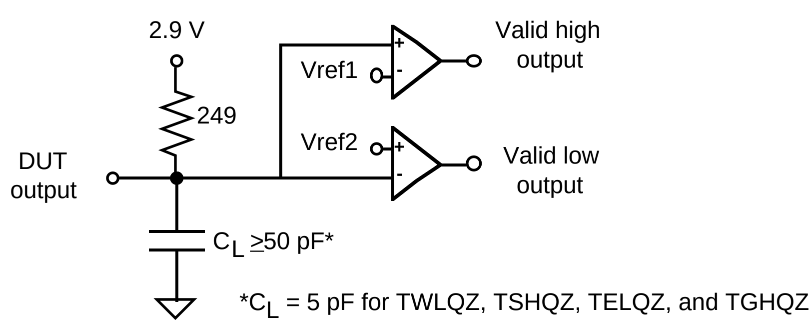
Symbol	Parameter	Typical (1)	Worst Case (2)		Units	Test Conditions
			Min	Max		
VDR	Data Retention Voltage (3)		2.5		V	NCS=VDR VI=VDR or VSS
IDR	Data Retention Current	200		1.0	mA	NCS=VDD=VDR VI=VDR or VSS

(1) Typical operating conditions: TA= 25°C, pre-radiation.
(2) Worst case operating conditions: TA= -55°C to +125°C, past total dose at 25°C.
(3) To maintain valid data storage during transient radiation, VDD must be held within the recommended operating range.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Typical (1)	Worst Case (2)		Units	Test Conditions
				Min	Max		
IDDSB	Static Supply Current		0.4		2.0	mA	VIH=VDD, IO=0, VIL=VSS, f=0MHz
IDDSBMF	Standby Supply Current - Deselected		0.4		2.0	mA	NCS=VDD, IO=0, f=40 MHz,
IDDOPW	Dynamic Supply Current, Selected (Write)		4.5		6.0	mA	f=1 MHz, IO=0, CE=VIH=VDD NCS=VIL=VSS (3)
IDDOPR	Dynamic Supply Current, Selected (Read)		2.8		4.5	mA	f=1 MHz, IO=0, CE=VIH=VDD NCS=VIL=VSS (3)
II	Input Leakage Current			-5	+5	µA	VSS≤VI≤VDD
IOZ	Output Leakage Current			-10	+10	µA	VSS≤VIO≤VDD Output=high Z
VIL	Low-Level Input Voltage	CMOS TTL	1.7		0.3xVDD 0.8	V V	March Pattern VDD = 4.5V
VIH	High-Level Input Voltage	CMOS TTL	3.2	0.7xVDD 2.2		V V	March Pattern VDD = 5.5V
VOL	Low-Level Output Voltage		0.3 0.005		0.4 0.1	V V	VDD = 4.5V, IOL = 10 mA VDD = 4.5V, IOL = 200 µA
VOH	High-Level Output Voltage		4.3 4.5	4.2 VDD-0.1		V V	VDD = 4.5V, IOH = -5 mA VDD = 4.5V, IOH = -200 µA

(1) Typical operating conditions: VDD= 5.0 V,TA=25°C, pre-radiation.
(2) Worst case operating conditions: VDD=4.5 V to 5.5 V, -55°C to +125°C, post total dose at 25°C.
(3) All inputs switching. DC average current.

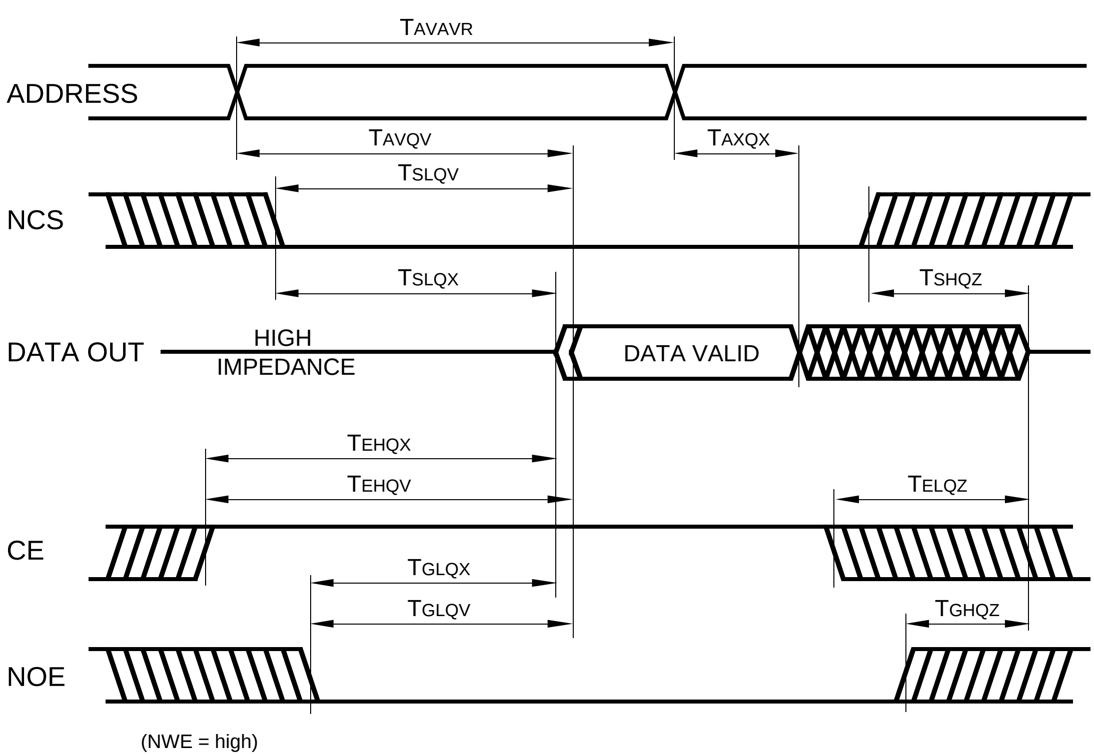


Tester Equivalent Load Circuit

READ CYCLE AC TIMING CHARACTERISTICS (1)

Symbol	Parameter	Typical (2)	Worst Case (3) -55 to 125°C Min	Worst Case (3) -55 to 125°C Max	Units
TAVAVR	Address Read Cycle Time	16	25		ns
TAVQV	Address Access Time	15		25	ns
TAXQX	Address Change to Output Invalid Time	12	3		ns
TSLQV	Chip Select Access Time	16		25	ns
TSLQX	Chip Select Output Enable Time	12	5		ns
TSHQZ	Chip Select Output Disable Time	5		10	ns
TEHQV	Chip Enable Access Time	16		25	ns
TEHQX	Chip Enable Output Enable Time	12	5		ns
TELQZ	Chip Enable Output Disable Time	6		10	ns
TGLQV	Output Enable Access Time	4		9	ns
TGLQX	Output Enable Output Enable Time	4	2		ns
TGHQZ	Output Enable Output Disable Time	4		9	ns

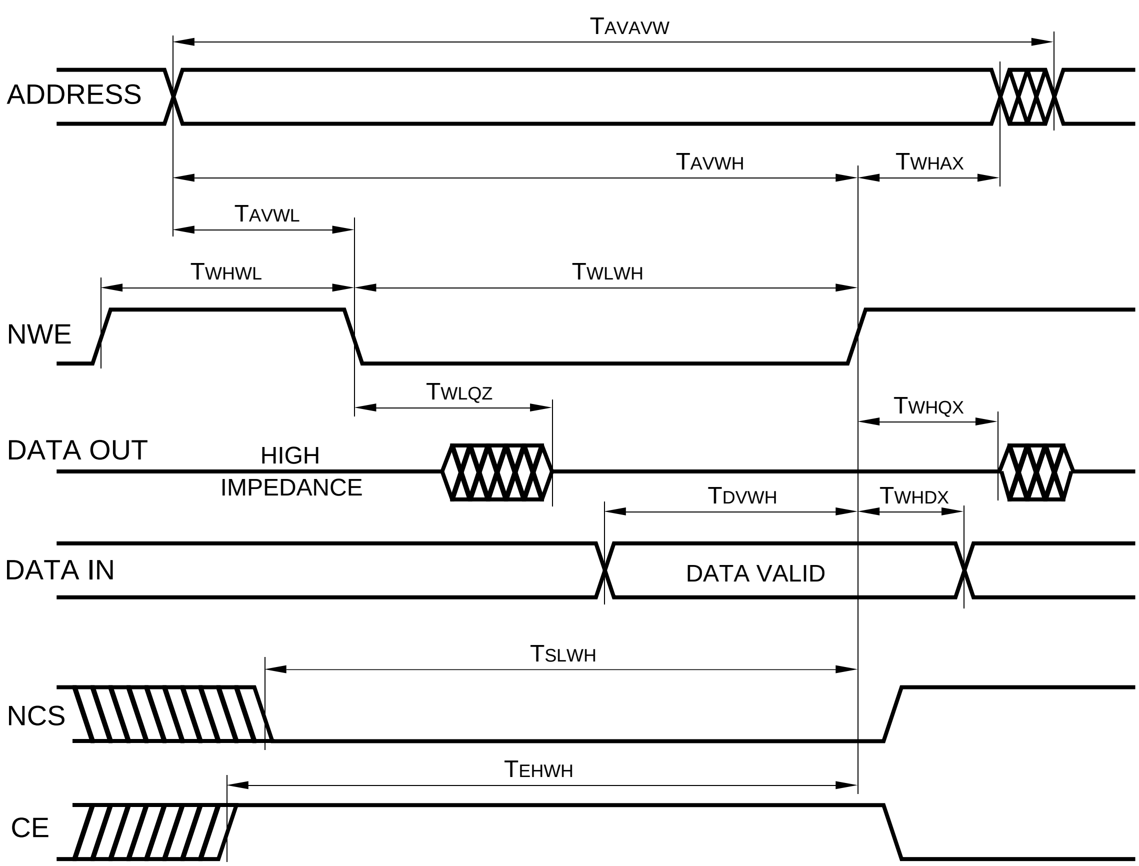
(1) Test conditions: input switching levels VIL/VIH=0.5V/VDD-0.5V (CMOS), VIL/VIH=0V/3V (TTL), input rise and fall times <1 ns/V, input and output timing reference levels shown in the Tester AC Timing Characteristics table, capacitive output loading $C_L \geq 50$ pF, or equivalent capacitive output loading C_L=5 pF for TSHQZ, TELQZ TGHQZ. For C_L >50 pF, derate access times by 0.02 ns/pF (typical).
(2) Typical operating conditions: VDD=5.0 V, TA=25°C, pre-radiation.
(3) Worst case operating conditions: VDD=4.5 V to 5.5 V, -55°C to 125°C, post total dose at 25°C.



WRITE CYCLE AC TIMING CHARACTERISTICS (1)

Symbol	Parameter	Typical (2)	Worst Case (3) -55 to 125°C Min	Worst Case (3) -55 to 125°C Max	Units
TAVAVW	Write Cycle Time (4)	13	25		ns
TWLWH	Write Enable Write Pulse Width	9	20		ns
TSLWH	Chip Select to End of Write Time	12	20		ns
TDVWH	Data Valid to End of Write Time	9	15		ns
TAVWH	Address Valid to End of Write Time	10	20		ns
TWHDX	Data Hold Time after End of Write Time	0	0		ns
TAVWL	Address Valid Setup to Start of Write Time	0	0		ns
TWHAX	Address Valid Hold after End of Write Time	0	0		ns
TWLQZ	Write Enable to Output Disable Time	5	0	9	ns
TWHQX	Write Disable to Output Enable Time	12	5		ns
TWHWL	Write Recovery Time	4	5		ns
TEHWH	Chip Enable to End of Write Time	11	20		ns

(1) Test conditions: input switching levels VIL/VIH=0.5V/VDD-0.5V (CMOS), VIL/VIH=0V/3V (TTL), input rise and fall times <1 ns/V, input and output timing reference levels shown in the Tester AC Timing Characteristics table, capacitive output loading $\geq$50 pF, or equivalent capacitive load of 5 pF for TWLQZ.
(2) Typical operating conditions: VDD=5.0 V, TA=25°C, pre-radiation.
(3) Worst case operating conditions: VDD=4.5 V to 5.5 V, -55 to 125°C, post total dose at 25°C.
(4) TAVAVW = TWLWH + TWHWL.



DYNAMIC ELECTRICAL CHARACTERISTICS

Read Cycle

The RAM is asynchronous in operation, allowing the read cycle to be controlled by address, chip select (NCS), or chip enable (CE) (refer to Read Cycle timing diagram). To perform a valid read operation, both chip select and output enable (NOE) must be low and chip enable and write enable (NWE) must be high. The output drivers can be controlled independently by the NOE signal. Consecutive read cycles can be executed with NCS held continuously low, and with CE held continuously high, and toggling the addresses.

For an address activated read cycle, NCS and CE must be valid prior to or coincident with the activating address edge transition(s). Any amount of toggling or skew between address edge transitions is permissible; however, data outputs will become valid TAVQV time following the latest occurring address edge transition. The minimum address activated read cycle time is TAVAV. When the RAM is operated at the minimum address activated read cycle time, the data outputs will remain valid on the RAM I/O until TAXQX time following the next sequential address transition.

To control a read cycle with NCS, all addresses and CE must be valid prior to or coincident with the enabling NCS edge transition. Address or CE edge transitions can occur later than the specified setup times to NCS, however, the valid data access time will be delayed. Any address edge transition, which occurs during the time when NCS is low, will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TSHQZ time following a disabling NCS edge transition.

To control a read cycle with CE, all addresses and NCS must be valid prior to or coincident with the enabling CE edge transition. Address or NCS edge transitions can occur later than the specified setup times to CE; however, the valid data access time will be delayed. Any address edge transition which occurs during the time when CE is high will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TELQZ time following a disabling CE edge transition.

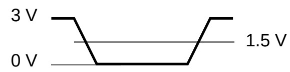
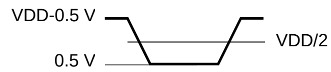
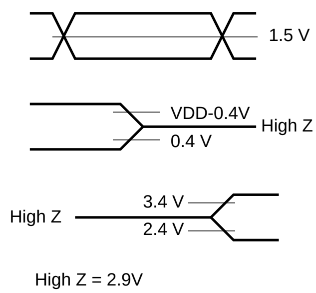
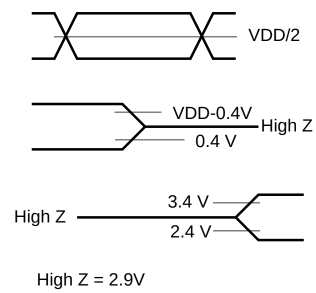
Write Cycle

The write operation is synchronous with respect to the address bits, and control is governed by write enable (NWE), chip select (NCS), or chip enable (CE) edge transitions (refer to Write Cycle timing diagrams). To perform a write operation, both NWE and NCS must be low, and CE must be high. Consecutive write cycles can be performed with NWE or NCS held continuously low, or CE held continuously high. At least one of the control signals must transition to the opposite state between consecutive write operations.

The write mode can be controlled via three different control signals: NWE, NCS, and CE. All three modes of control are similar except the NCS and CE controlled modes actually disable the RAM during the write recovery pulse. Both CE and NCS fully disable the RAM decode logic and input buffers for power savings. Only the NWE controlled mode is shown in the table and diagram on the previous page for simplicity; however, each mode of control provides the same write cycle timing characteristics. Thus, some of the parameter names referenced below are not shown in the write cycle table or diagram, but indicate which control pin is in control as it switches high or low.

To write data into the RAM, NWE and NCS must be held low and CE must be held high for at least TWLWH/TSLSH/TEHEL time. Any amount of edge skew between the signals can be tolerated, and any one of the control signals can initiate or terminate the write operation. For consecutive write operations, write pulses must be separated by the minimum specified TWHWL/TSHSL/TELEH time. Address inputs must be valid at least TAVWL/TAVSL/TAVEH time before the enabling NWE/NCS/CE edge transition, and must remain valid during the entire write time. A valid data overlap of write pulse width time of TDVWH/TDVSH/TDVEL, and an address valid to end of write time of TAVWH/TAVSH/TAVEL also must be provided for during the write operation. Hold times for address inputs and data inputs with respect to the disabling NWE/NCS/CE edge transition must be a minimum of TWHAX/TSHAX/TELAX time and TWHDX/TSHDX/TELDX time, respectively. The minimum write cycle time is TAVAV.

TESTER AC TIMING CHARACTERISTICS

	TTL I/O Configuration	CMOS I/O Configuration
Input Levels*		
Output Sense Levels		

* Input rise and fall times <1 ns/V

QUALITY AND RADIATIONHARDNESS ASSURANCE

Honeywell maintains a high level of product integrity through process control, utilizing statistical process control, a complete "Total Quality Assurance System," a computer data base process performance tracking system, and a radiation hardness assurance strategy.

The radiation hardness assurance strategy starts with a technology that is resistant to the effects of radiation. Radiation hardness is assured on every wafer by irradiating test structures as well as SRAM product, and then monitoring key parameters which are sensitive to ionizing radiation. Conventional MIL-STD-883 TM 5005 Group E testing, which includes total dose exposure with Cobalt 60, may also be performed as required. This Total Quality approach ensures our customers of a reliable product by engineering in reliability, starting with process development and continuing through product qualification and screening.

SCREENING LEVELS

Honeywell offers several levels of device screening to meet your system needs. "Engineering Devices" are available with limited performance and screening for breadboarding and/or evaluation testing. Hi-Rel Level B and S devices undergo additional screening per the requirements of MIL-STD-883. As a QML supplier, Honeywell also offers QML Class Q and V devices per MIL-PRF-38535 and are available per the applicable Standard Microcircuits Drawing (SMD). QML devices offer ease of procurement by eliminating the need to create detailed specifications and offer benefits of improved quality and cost savings through standardization.

RELIABILITY

Honeywell understands the stringent reliability requirements that space and defense systems require and has extensive experience in reliability testing on programs of this nature. This experience is derived from comprehensive testing of VLSI processes. Reliability attributes of the RICMOS™ process were characterized by testing specially designed irradiated and non-irradiated test structures from which specific failure mechanisms were evaluated. These specific mechanisms included, but were not limited to, hot carriers, electromigration and time dependent dielectric breakdown. This data was then used to make changes to the design models and process to ensure more reliable products.

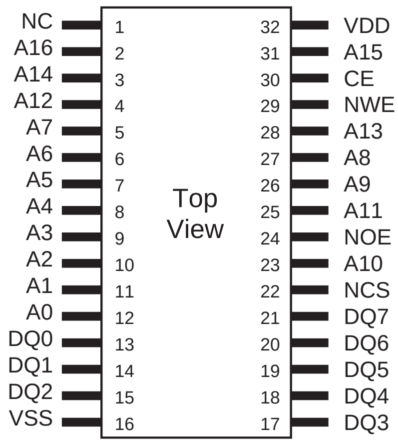
In addition, the reliability of the RICMOS™ process and product in a military environment was monitored by testing irradiated and non-irradiated circuits in accelerated dynamic life test conditions. Packages are qualified for product use after undergoing Groups B & D testing as outlined in MIL-STD-883, TM 5005, Class S. The product is qualified by following a screening and testing flow to meet the customer's requirements. Quality conformance testing is performed as an option on all production lots to ensure the ongoing reliability of the product.

PACKAGING

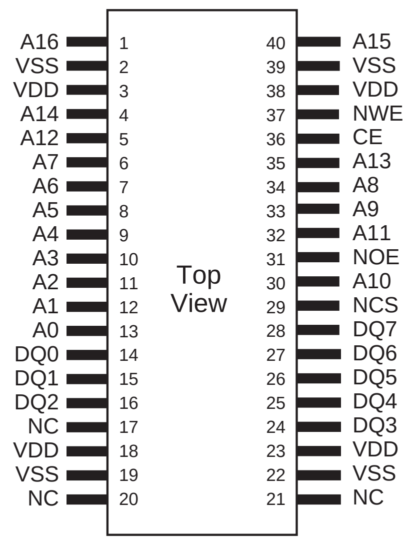
The 128K x 8 SOI SRAM is offered in a custom 32-lead or 40-lead Flat Pack. The package is constructed of multilayer ceramic (Al_2O_3) and features internal power and ground planes.

Ceramic chip capacitors can be mounted to the package by the user to maximize supply noise decoupling and increase board packing density. These capacitors effectively attach to the internal package power and ground planes. This design minimizes resistance and inductance of the bond wire and package, both of which are critical in a transient radiation environment. All NC (no connect) pins should be connected to VSS to prevent charge build up in the radiation environment.

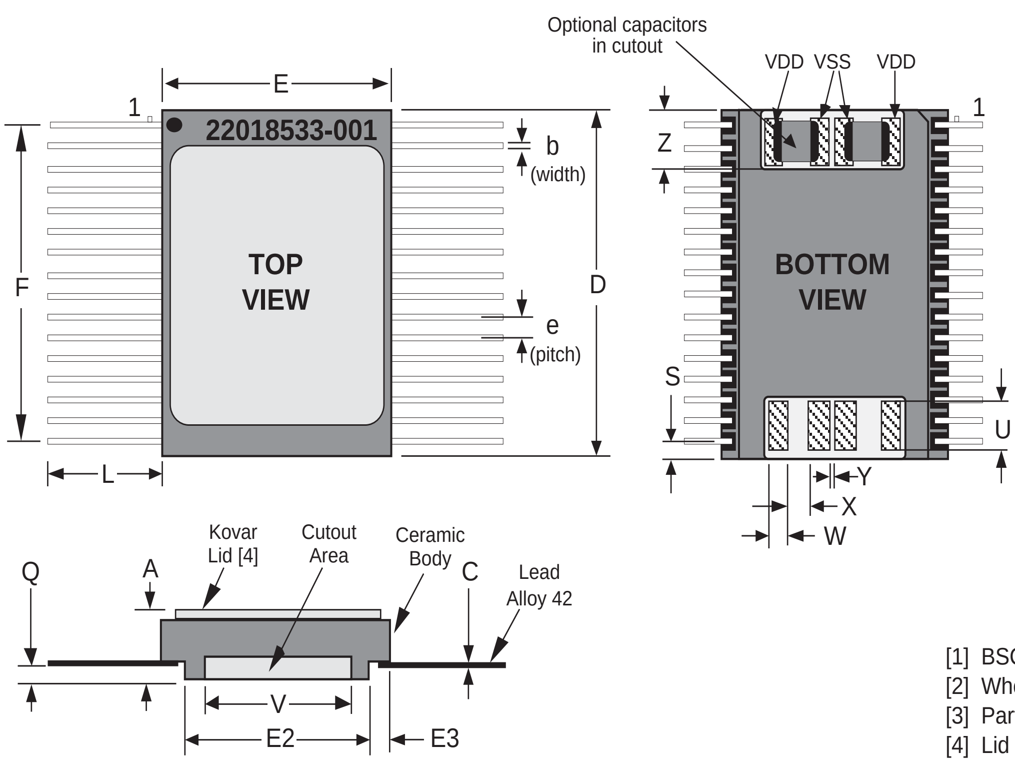
32-LEAD FLAT PACK PINOUT



40-LEAD FLAT PACK PINOUT



32-LEAD FLAT PACK

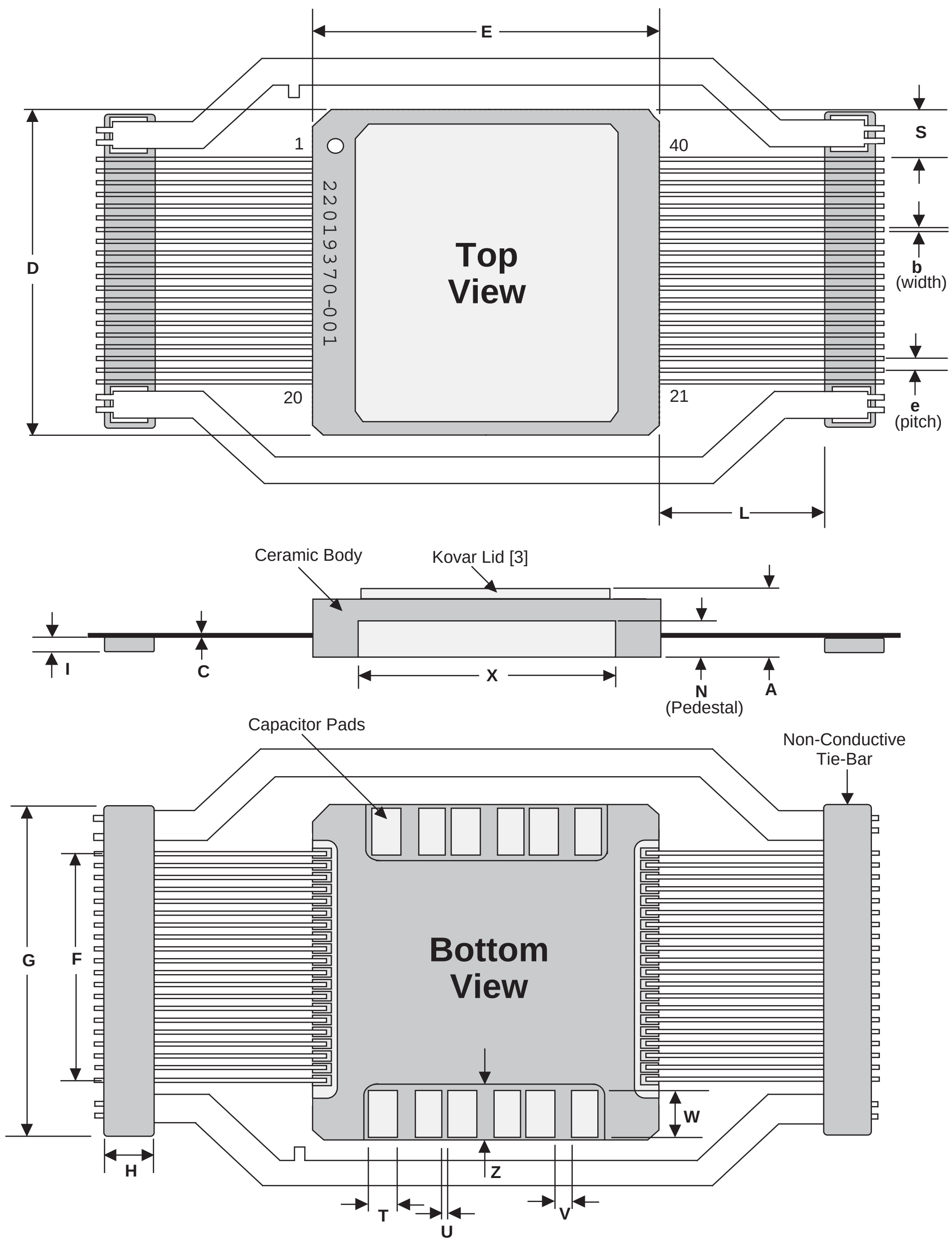


All dimensions in inches

A	0.135 ± 0.015
b	0.017 ± 0.002
C	0.004 to 0.009
D	0.820 ± 0.008
e	0.050 ± 0.005 [1]
E	0.600 ± 0.008
E2	0.500 ± 0.008
E3	0.040 ref
F	0.750 ± 0.005 [2]
L	0.295 min [3]
Q	0.026 to 0.045
S	0.035 ± 0.010
U	0.080 ref
V	0.380 ref
W	0.050 ref
X	0.075 ref
Y	0.010 ref
Z	0.135 ref

[1] BSC - Basic lead spacing between centers
[2] Where lead is brazed to package
[3] Parts delivered with leads unformed
[4] Lid connected to VSS

40-LEAD FLAT PACK

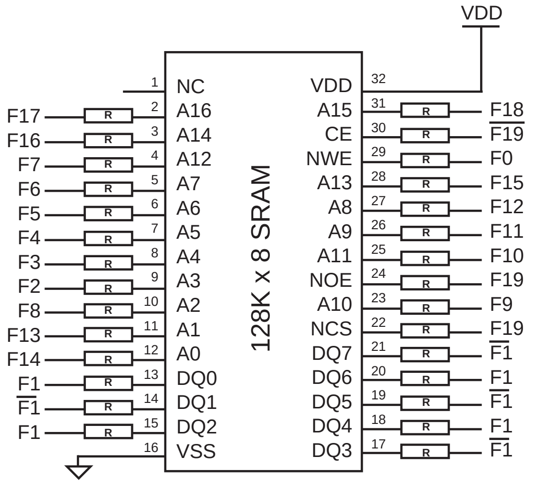


All dimensions are in inches

A	0.131 ± .015
b	0.008 ± 0.002
c	0.006 ± 0.0015
D	0.710 ±0.010
E	0.775 ± 0.007
e	0.025 ± 0.004
F	0.475 ± 0.005
G	0.760 ± 0.008
H	0.135 ± 0.005
I	0.030 ± 0.005
L	0.285 ± 0.015
N	0.050 ± 0.004
S	0.1175 ref
T	0.064 ref
U	0.006 ref
V	0.028 ref
W	0.125 ref
X	0.500 ± 0.005
Z	0.140 ref

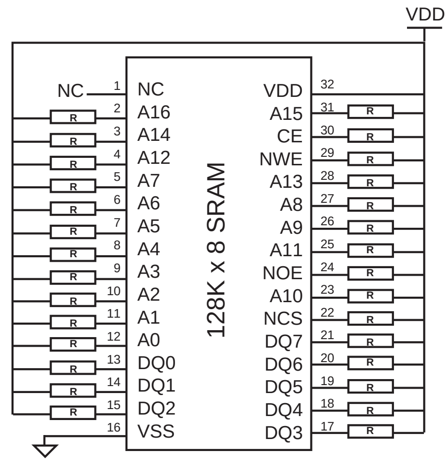
[1] Parts delivered with leads unformed
[2] At tie bar
[3] Lid tied to VSS

DYNAMIC BURN-IN DIAGRAM*



VDD = 5.6V, R ≤ 10 KΩ, VIH = VDD, VIL = VSS
Ambient Temperature ≥ 125 °C, F0 ≥ 100 KHz Sq Wave
Frequency of F1 = F0/2, F2 = F0/4, F3 = F0/8, etc.

STATIC BURN-IN DIAGRAM*



VDD = 5.5V, R ≤ 10 KΩ
Ambient Temperature ≥ 125 °C

*40-Lead Flat Pack burn-in diagrams have similar connections and are available upon request.

ORDERING INFORMATION (1)

H X 6228 T S R C

PART NUMBER (6228)

SCREEN LEVEL (S)
V=QML Class V
Q=QML Class Q
S=Level S
B=Level B
E=Engr Device (2)

PROCESS (X)
X=SOI

SOURCE (H)
H=HONEYWELL

PACKAGE DESIGNATION (T)
T=32-Lead FP
A=40-Lead FP
K=Known Good Die
- =Bare die (No Package)

TOTAL DOSE HARDNESS (R)
R=1x10^5 rad(SiO_2)
F=3x10^5 rad(SiO_2)
H=1x10^6 rad(SiO_2)
N=No Level Guaranteed

INPUT BUFFER TYPE (C)
C=CMOS Level
T=TTL Level

(1) Orders may be faxed to 612-954-2051. For technical assistance, contact our Customer Logistics Department at 612-954-2888.
(2) Engineering Device description: Parameters are tested from -55 to 125°C, 24 hr burn-in, IDDSB = 10mA, no radiation guaranteed.
Contact Factory with other needs.

To learn more about Honeywell Solid State Electronics Center, visit our web site at http://www.ssec.honeywell.com

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