
HM628512C Series

4 M SRAM (512-kword \times 8-bit)

HITACHI

ADE-203-1212B (Z)

Rev. 2.0

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Description

The Hitachi HM628512C is a 4-Mbit static RAM organized 512-kword \times 8-bit. It realizes higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). The device, packaged in a 525-mil SOP (foot print pitch width) or 400-mil TSOP TYPE II or 600-mil plastic DIP, is available for high density mounting. The HM628512C is suitable for battery backup system.

Features

- Single 5 V supply
- Access time: 55/70 ns (max)
- Power dissipation
 - Active: 10 mW/MHz (typ)
 - Standby: 4 μ W (typ)
- Completely static memory. No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Battery backup operation

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Ordering Information

Type No.	Access time	Package
HM628512CLP-5	55 ns	600-mil 32-pin plastic DIP (DP-32)
HM628512CLP-7	70 ns	
HM628512CLP-5SL	55 ns	
HM628512CLFP-5	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM628512CLFP-7	70 ns	
HM628512CLFP-5SL	55 ns	
HM628512CLTT-5	55 ns	400-mil 32-pin plastic TSOP II (TTP-32D)
HM628512CLTT-7	70 ns	
HM628512CLTT-5SL	55 ns	
HM628512CLRR-5	55 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)
HM628512CLRR-7	70 ns	
HM628512CLRR-5SL	55 ns	