Data Sheet July 1999 File Number 3404.4

70A, 30V, 0.010 Ohm, N-Channel Power MOSFETs

These N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49025.

Ordering Information

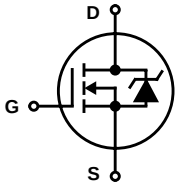
PART NUMBER	PACKAGE	BRAND
RFP70N03	TO-220AB	RFP70N03
RF1S70N03SM	TO-263AB	F1S70N03

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, e.g., RF1S70N03SM9A

Features

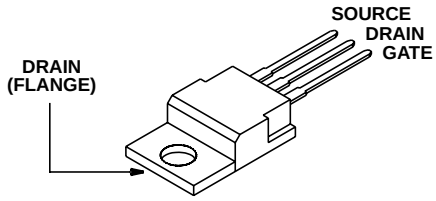
- 70A, 30V
- $r_{DS(ON)} = 0.010\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve (Single Pulse)
- $175^{o}C$ Operating Temperature
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

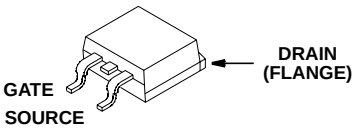


Packaging

JEDEC TO-220AB



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	30	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	30	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current			
Continuous (Figure 2)	I_D	70	A
Pulsed Drain Current	I_{DM}	200	A
Pulsed Avalanche Rating	E_{AS}	Figures 5, 13, 14	
Power Dissipation	P_D	150	W
Derate Above 25^oC		1.0	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from case for 10s	T_L	300	^oC
Package Body for 10s, see Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 10)		30	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA (Figure 9)		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V		-	-	1	μA
		V_{DS} = 30V, V_{GS} = 0V, $T_C = 150^oC$		-	-	50	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 70A, V_{GS} = 10V (Figure 8)		-	-	0.010	Ω
Turn-On Time	t_{ON}	V_{DD} = 15V, $I_D \cong$ 70A, R_L = 0.214Ω, V_{GS} = 10V, R_{GS} = 2.5Ω		-	-	80	ns
Turn-On Delay Time	$t_{d(ON)}$			-	20	-	ns
Rise Time	t_r			-	20	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	40	-	ns
Fall Time	t_f			-	25	-	ns
Turn-Off Time	t_{OFF}			-	-	125	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 24V, $I_D \cong$ 70A, R_L = 0.343Ω, $I_{g(REF)}$ = 1.0mA (Figure 12)	-	215	260	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V		-	120	145	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 2V		-	6.5	8.0	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 11)		-	3300	-	pF
Output Capacitance	C_{OSS}			-	1750	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	750	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)		-	-	1.0	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220, TO-263		-	-	62	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 70A	-	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 70A, dI_{SD}/dt = 100A/μs	-	-	125	ns

Typical Performance Curves

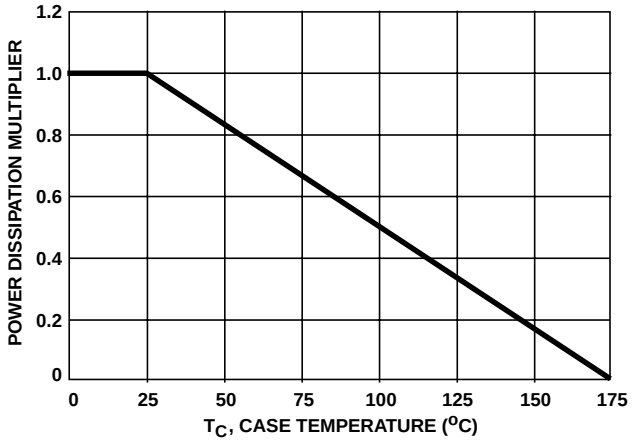


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

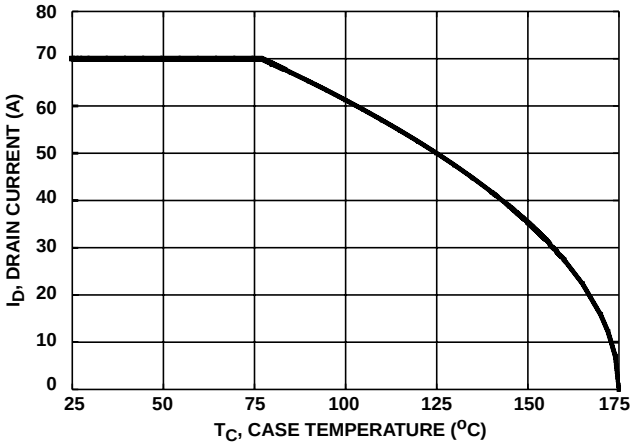


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

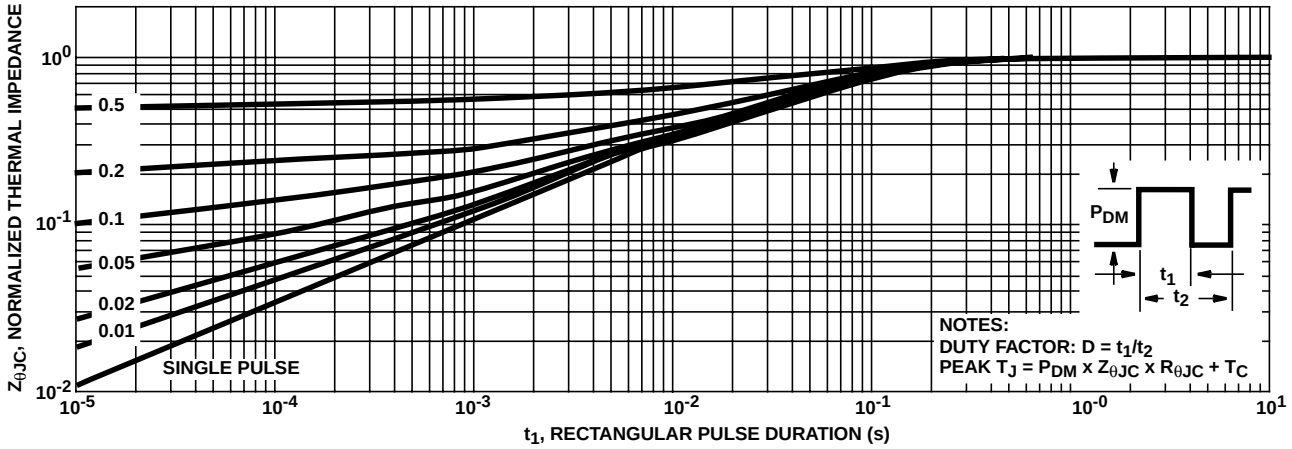


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

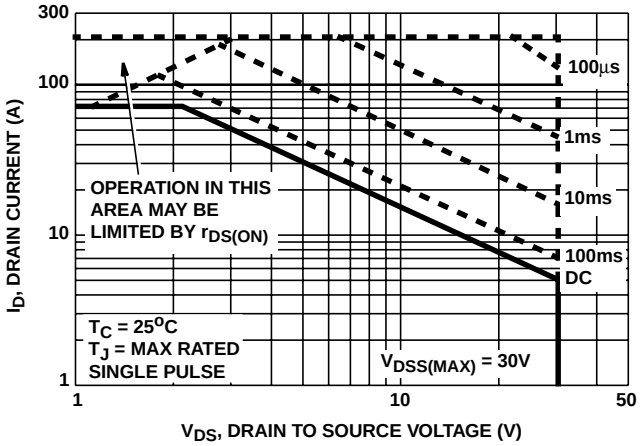
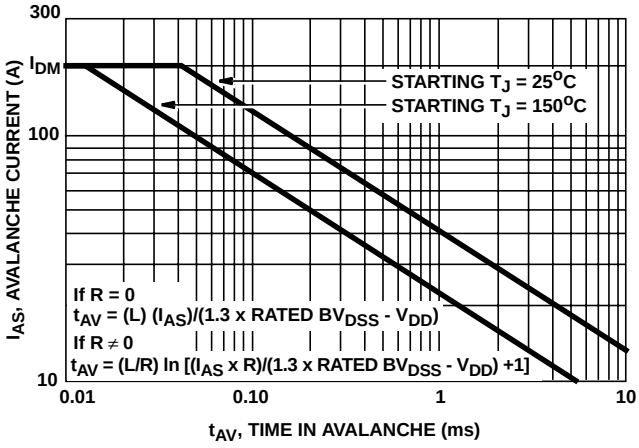


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 5. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

Typical Performance Curves (Continued)

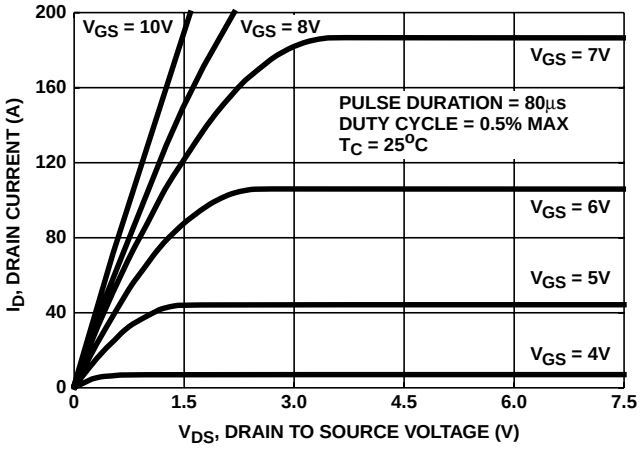


FIGURE 6. SATURATION CHARACTERISTICS

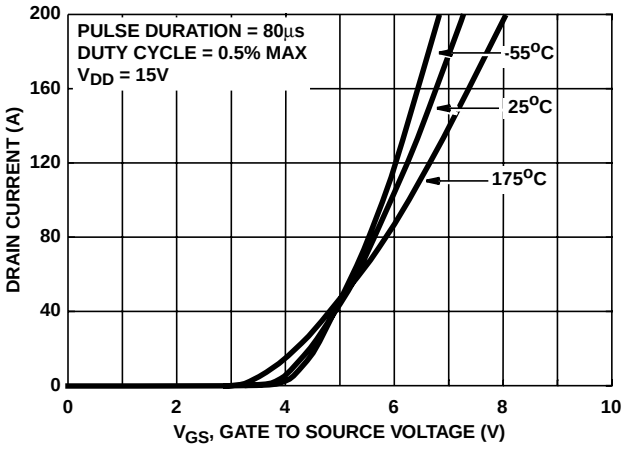


FIGURE 7. TRANSFER CHARACTERISTICS

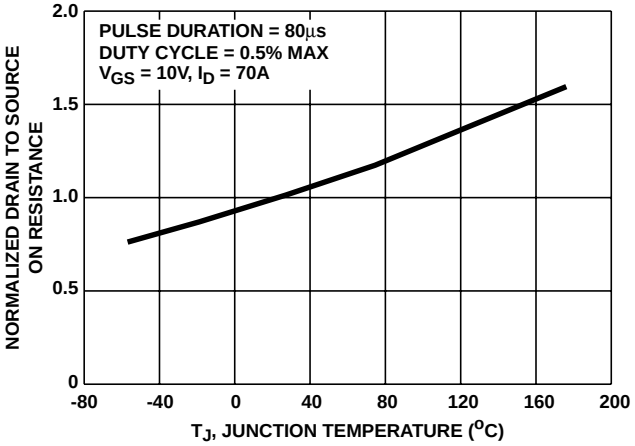


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

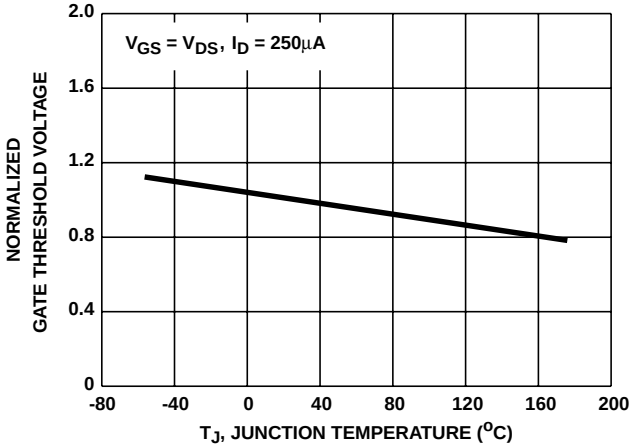


FIGURE 9. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

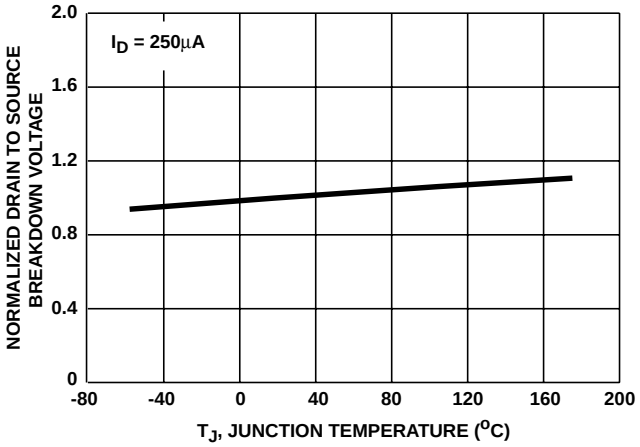


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

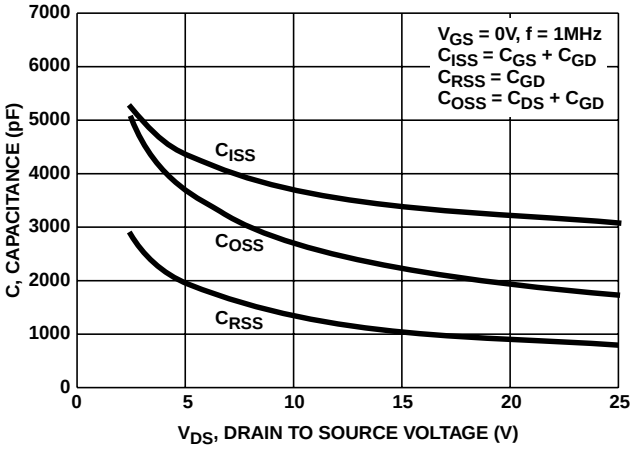
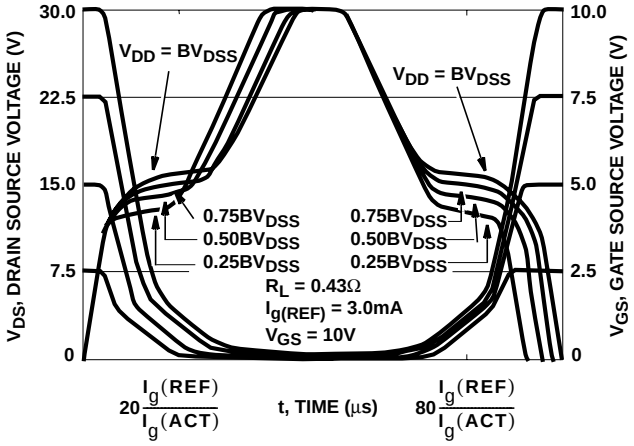


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves (Continued)



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 12. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

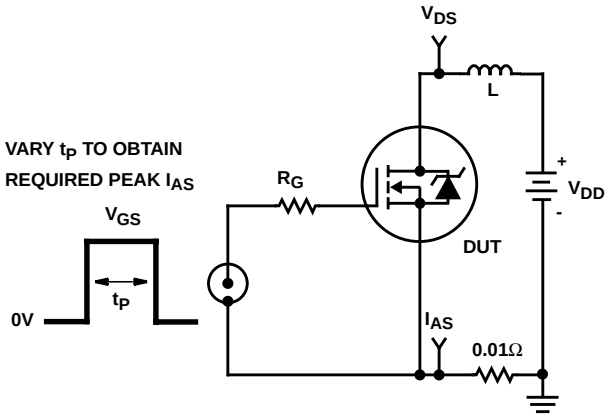


FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

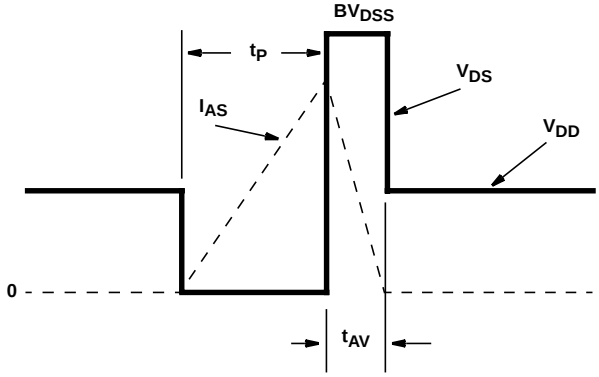


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

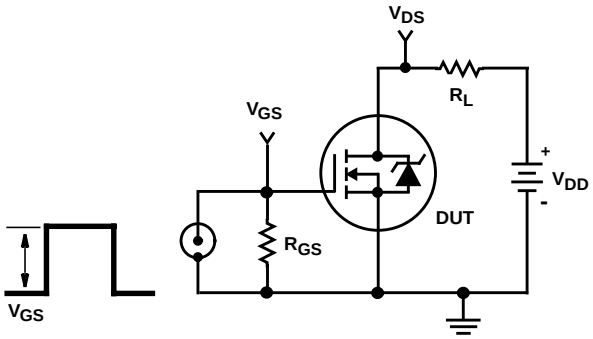


FIGURE 15. SWITCHING TIME TEST CIRCUIT

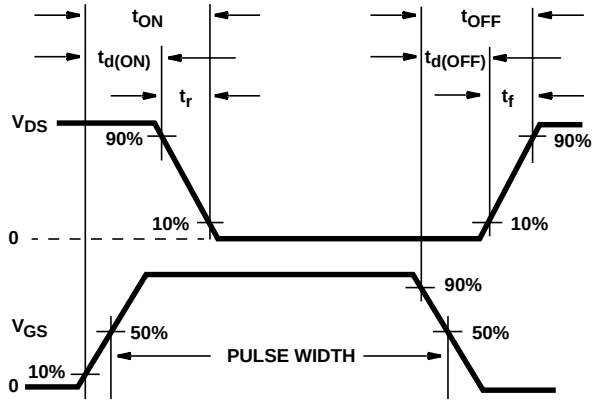


FIGURE 16. SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

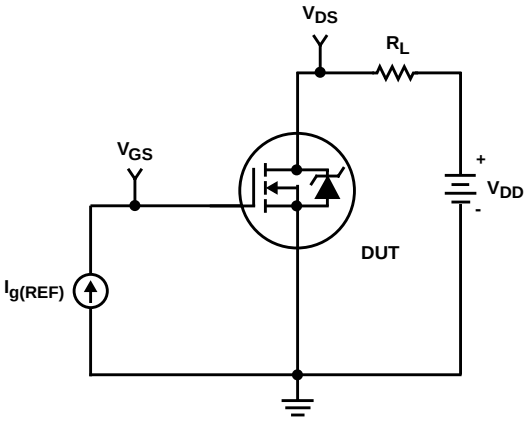


FIGURE 17. GATE CHARGE TEST CIRCUIT

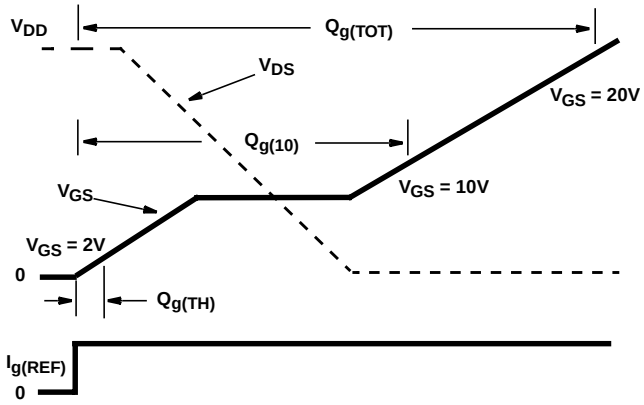
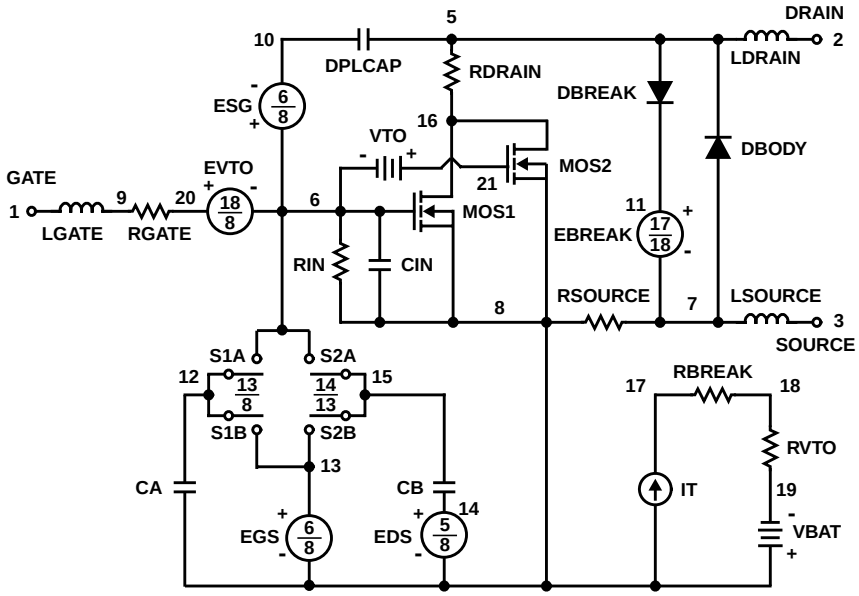


FIGURE 18. GATE CHARGE WAVEFORM

PSPICE Electrical Model

```
.SUBCKT RFP70N03 2 1 3 ;          rev 9/16/92
*NOM TEMP = 25OC


CA 12 8 6.09e-9
CB 15 14 6.05e-9
CIN 6 8 3.40e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 35.4
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 3.10e-9
LSOURCE 3 7 1.82e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 30.7e-6
RGATE 9 20 0.890
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 3.92e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.605
```



NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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FAX: (886) 2 2715 3029

Data Sheet July 1999 File Number 3404.4

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NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, e.g., RF1S70N03SM9A

Features

- 70A, 30V
- $r_{DS(ON)} = 0.010\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve (Single Pulse)
- $175^{o}C$ Operating Temperature
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

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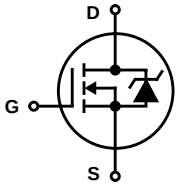
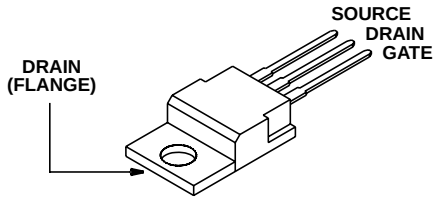
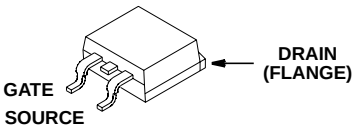


Packaging

JEDEC TO-220AB



JEDEC TO-263AB



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			UNITS
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Gate to Source Voltage	V_{GS}	±20	V
Drain Current			
Continuous (Figure 2)	I_D	70	A
Pulsed Drain Current	I_{DM}	200	A
Pulsed Avalanche Rating	E_{AS}	Figures 5, 13, 14	
Power Dissipation	P_D	150	W
Derate Above 25^oC		1.0	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from case for 10s	T_L	300	^oC
Package Body for 10s, see Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

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Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

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Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA (Figure 9)		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V		-	-	1	μA
		V_{DS} = 30V, V_{GS} = 0V, $T_C = 150^oC$		-	-	50	μA
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Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 70A, V_{GS} = 10V (Figure 8)		-	-	0.010	Ω
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Fall Time	t_f			-	25	-	ns
Turn-Off Time	t_{OFF}			-	-	125	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 24V, $I_D \cong$ 70A, R_L = 0.343Ω, $I_{g(REF)}$ = 1.0mA (Figure 12)	-	215	260	nC
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Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 11)		-	3300	-	pF
Output Capacitance	C_{OSS}			-	1750	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	750	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)		-	-	1.0	$^oC/W$
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Source to Drain Diode Specifications

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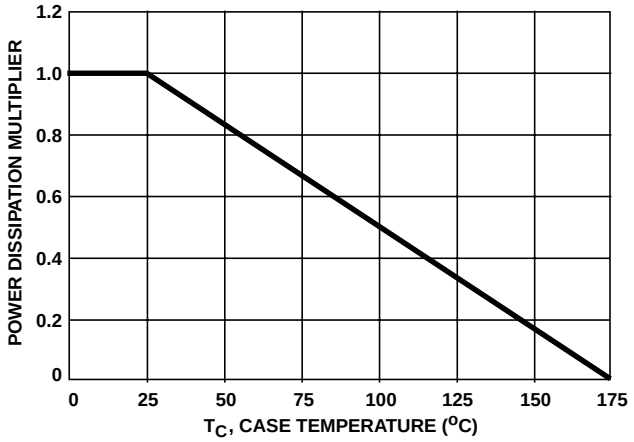
Typical Performance Curves



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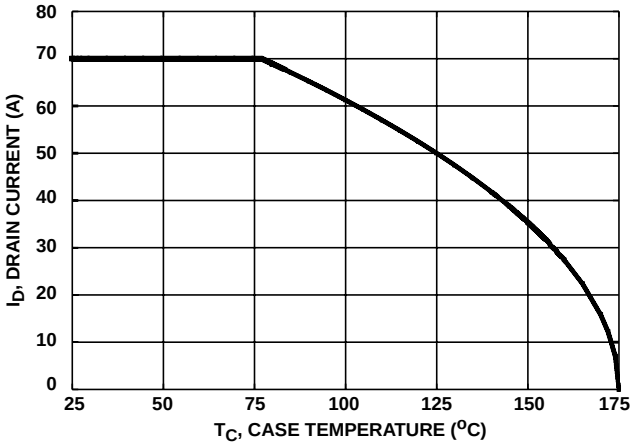

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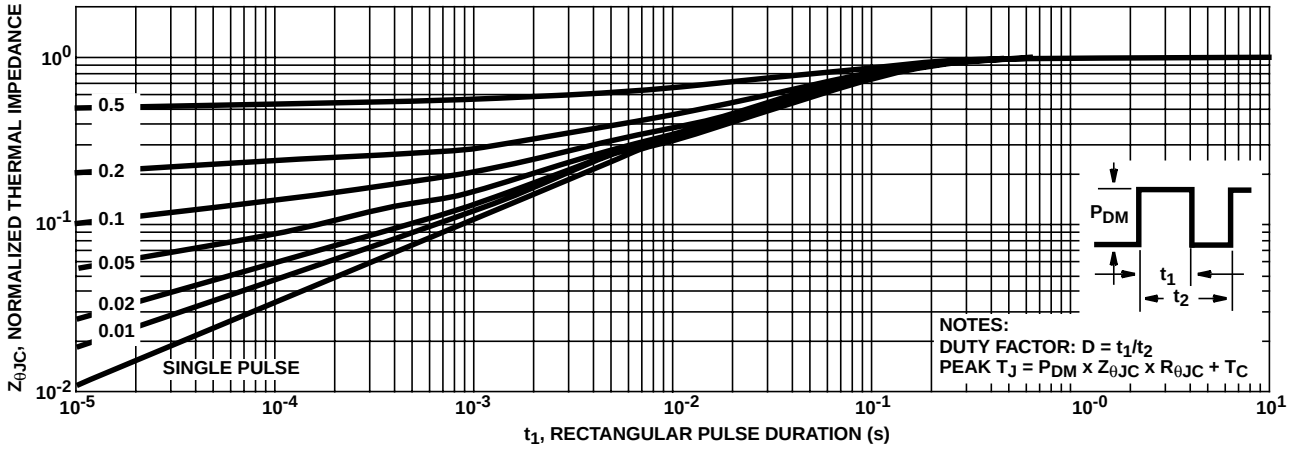

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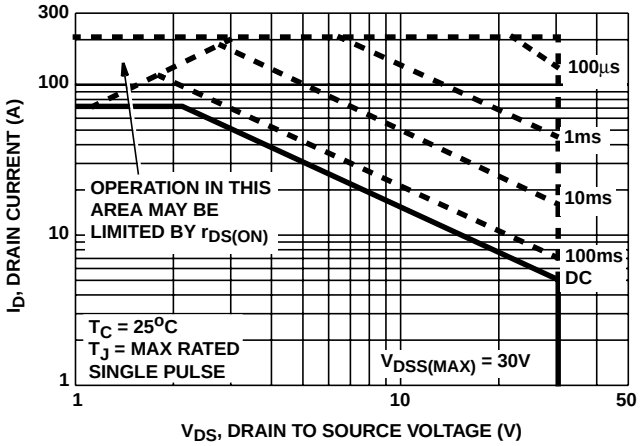
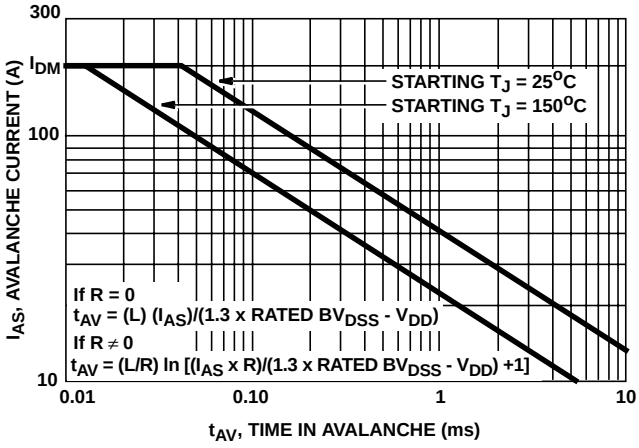


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 5. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

Typical Performance Curves (Continued)

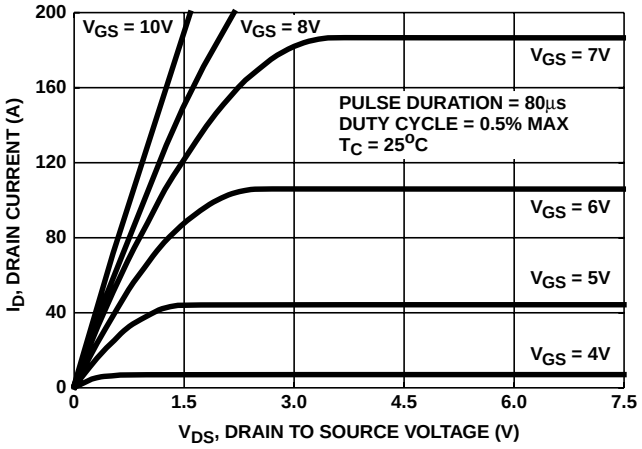


FIGURE 6. SATURATION CHARACTERISTICS

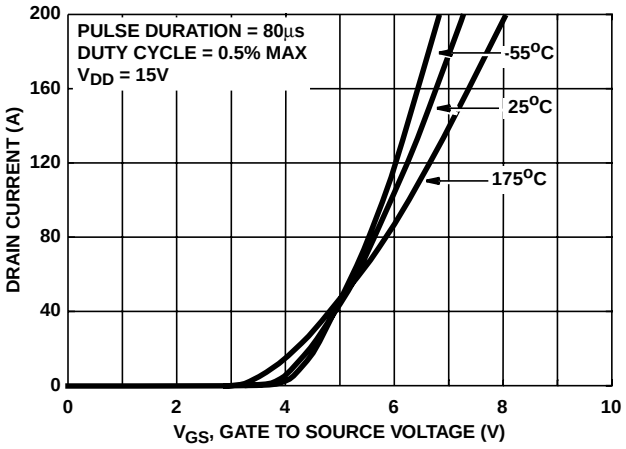


FIGURE 7. TRANSFER CHARACTERISTICS

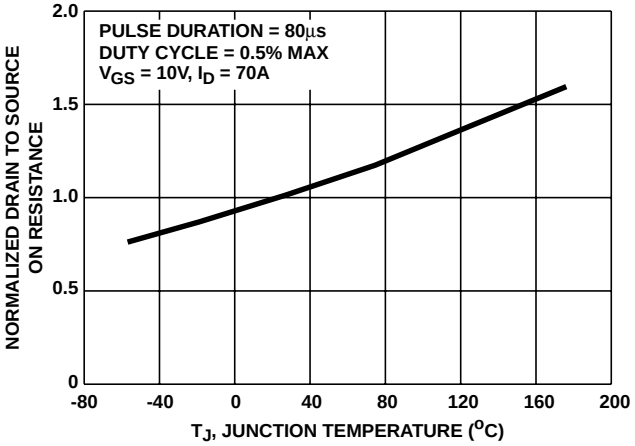


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

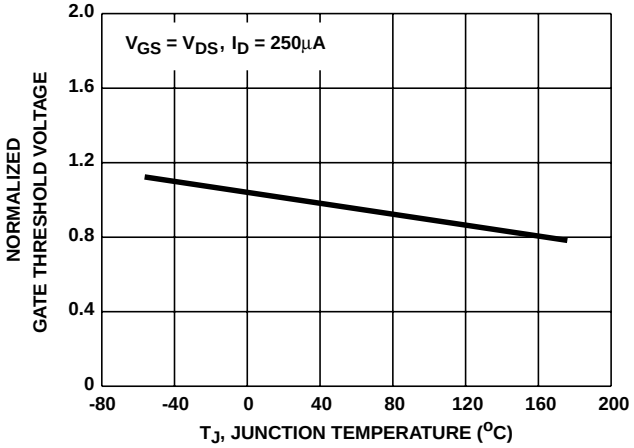


FIGURE 9. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

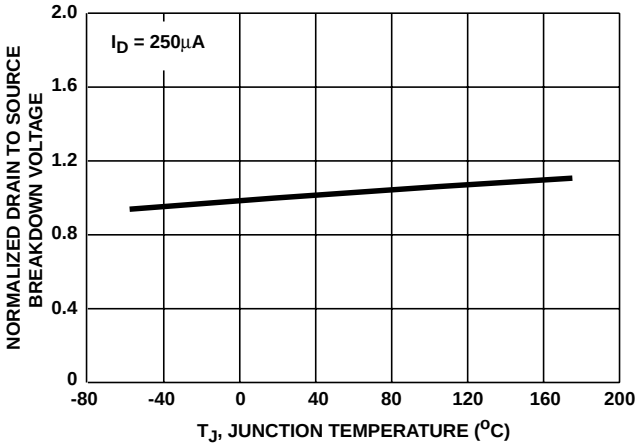


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

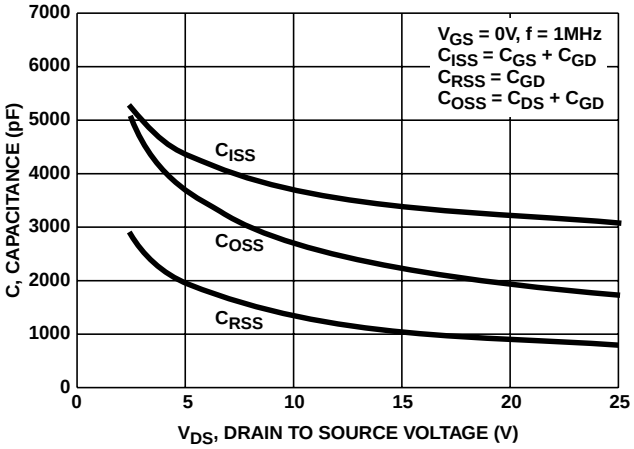
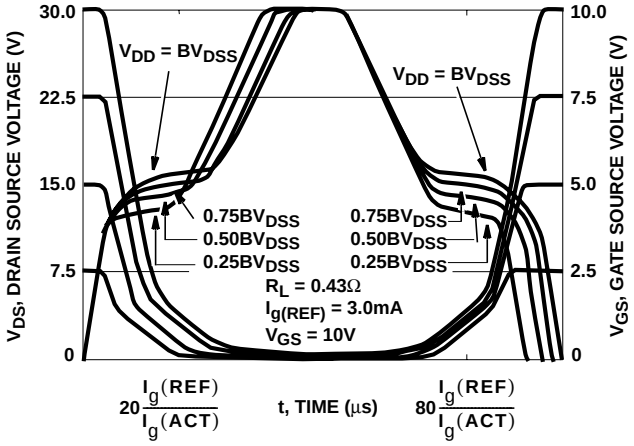


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves (Continued)



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 12. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

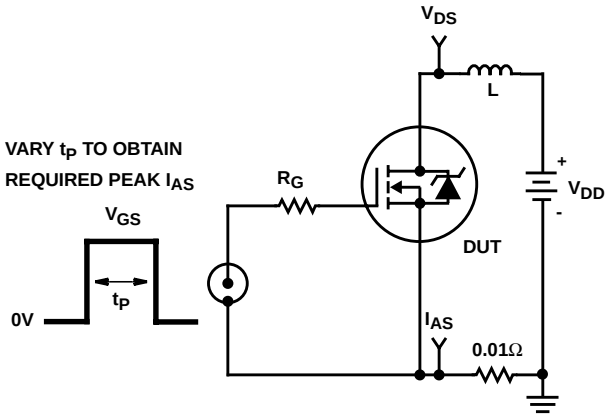


FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

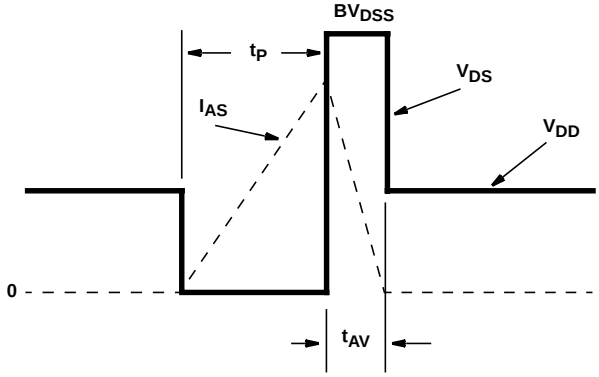


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

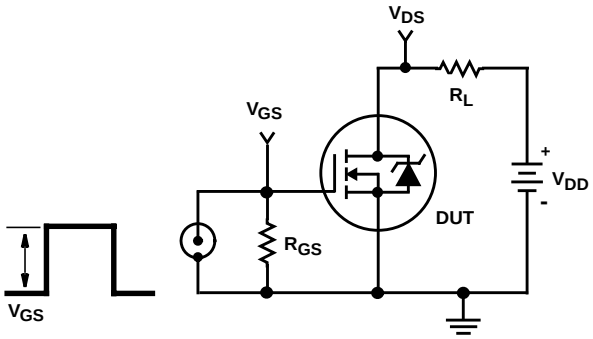


FIGURE 15. SWITCHING TIME TEST CIRCUIT

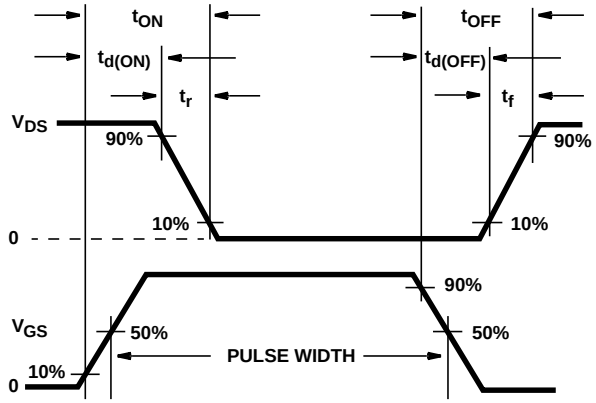


FIGURE 16. SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

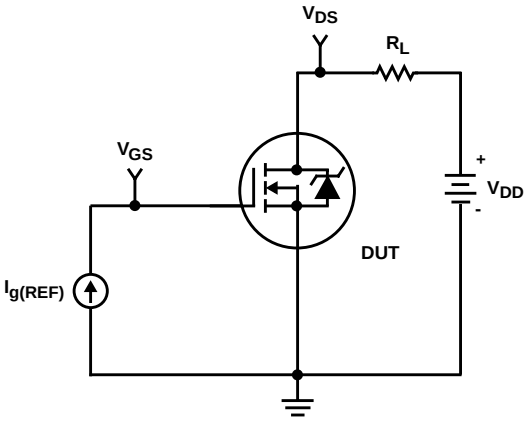


FIGURE 17. GATE CHARGE TEST CIRCUIT

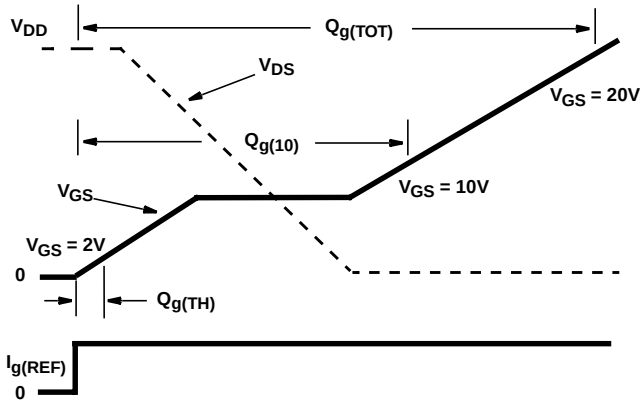
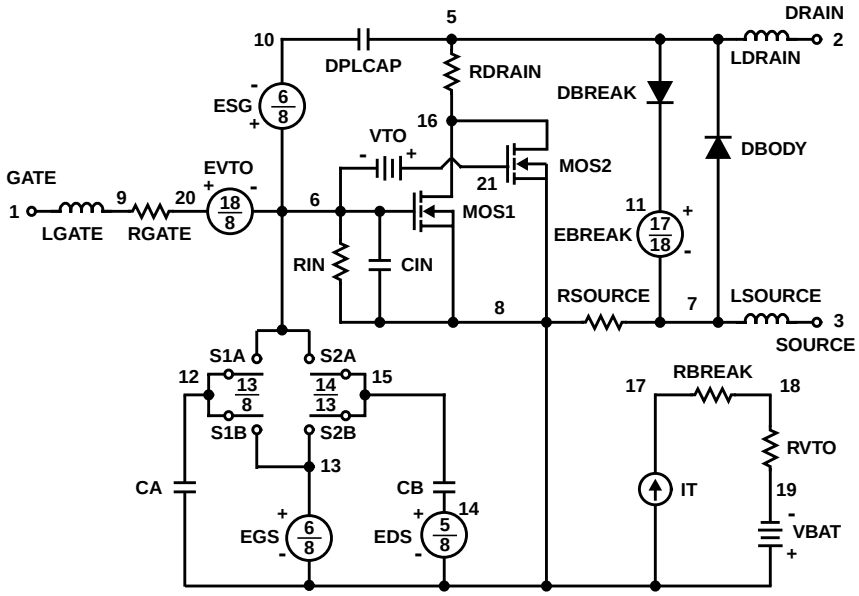


FIGURE 18. GATE CHARGE WAVEFORM

PSPICE Electrical Model

```
.SUBCKT RFP70N03 2 1 3 ;          rev 9/16/92
*NOM TEMP = 25OC


CA 12 8 6.09e-9
CB 15 14 6.05e-9
CIN 6 8 3.40e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 35.4
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 3.10e-9
LSOURCE 3 7 1.82e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 30.7e-6
RGATE 9 20 0.890
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 3.92e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.605
```



NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

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