

011521
9024

DUAL J $\bar{K}$ (OR D) FLIP-FLOP

DESCRIPTION — The 9024 consists of two high speed, clocked J $\bar{K}$ flip-flops. The Clocking operation is independent of rise and fall times of the clock waveform. The J $\bar{K}$ design allows operation as a D flip-flop by simply connecting the J and $\bar{K}$ pins together.

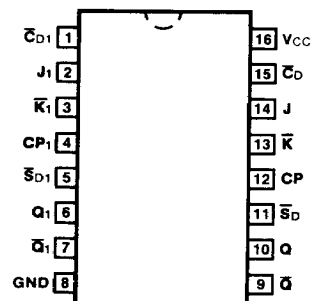
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V $\pm$ 5%, T _A = 0°C to +75°C	V _{CC} = +5.0 V $\pm$ 10%, T _A = -55°C to +125°C	
Ceramic DIP (D)	A	9024DC	9024DM	6B
Flatpak (F)	A	9024FC	9024FM	4L

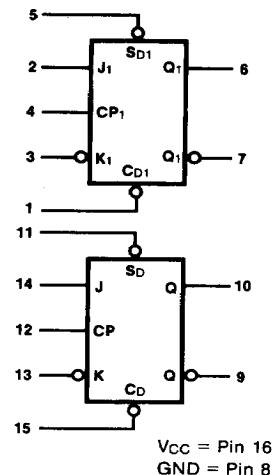
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	9XXX (U.L.) HIGH/LOW
J, $\bar{K}$ Inputs	1.5/1.0
Clock, $\bar{S}_D$ Inputs	3.0/2.0
$\bar{C}_D$ Input	6.0/3.0
Outputs	30/8.8 (7.8)

CONNECTION DIAGRAM PINOUT A



LOGIC SYMBOL



SYNCHRONOUS ENTRY J- $\bar{K}$ MODE OPERATION

INPUTS @ t _n	OUTPUTS @ t _n + 1
J $\bar{K}$	Q $\bar{Q}$
L H	No Change
L L	L H
H H	H L
H L	Toggles

SYNCHRONOUS ENTRY D MODE OPERATION

INPUTS @ t _n	OUTPUTS @ t _n + 1
D	Q $\bar{Q}$
L H	L H
H L	H L

H = HIGH Voltage Level
L = LOW Voltage Level
t_n, t_{n+1} = time before and
after rising edge of CP.

ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

INPUTS	OUTPUTS
$\bar{S}_D$ $\bar{C}_D$	Q $\bar{Q}$
5(11) 1(15)	6(10) 7(9)
L L	H H
L H	H L
H L	L H
H H	No Change

9XXX Series

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DC CHARACTERISTICS OVER COMMERCIAL TEMPERATURE RANGE: $V_{CC} = +5.0 \text{ V} \pm 5\%$

SYMBOL	PARAMETER	0°C		25°C		75°C		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
V_{IH}	Input HIGH Voltage	1.9		1.8		1.6		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage	0.85		0.85		0.85		V	Guaranteed Input LOW Threshold
V_{OL}	Output LOW Voltage	0.45		0.45		0.45		V	$V_{CC} = 4.75 \text{ V}$, $I_{OL} = 14.1 \text{ mA}$ $V_{CC} = 5.25 \text{ V}$, $I_{OL} = 16 \text{ mA}$
I_{IH}	Input HIGH Current J, $\bar{K}$ Clock Input, $\bar{S}_D$ $\bar{C}_D$			60 120 240		60 120 240		μA	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 4.5 \text{ V}$ Gnd on Other Inputs
I_{IL}	Input LOW Current J, $\bar{K}$ Clock Input, $\bar{S}_D$ $\bar{C}_D^*$	-1.6 -3.2 -4.8		-1.6 -3.2 -4.8		-1.6 -3.2 -4.8		mA	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = .45 \text{ V}$ 4.5 V on Other Inputs
	J, $\bar{K}$ Clock Input, $\bar{S}_D$ $\bar{C}_D^*$	-1.41 -2.82 -4.23		-1.41 -2.82 -4.23		-1.41 -2.82 -4.23		mA	$V_{CC} = 4.75 \text{ V}$, $V_{IN} = .45 \text{ V}$ 4.5 V on Other Inputs
I_{OS}	Output Short Circuit Current	-30	-100	-30	-100	-30	-100	mA	$V_{CC} = 5.25 \text{ V}$, $V_{OUT} = 0 \text{ V}$
I_{CC}	Power Supply Current			14				mA	Per Flip-Flop in Worst Logic State

*Denotes maximum current under normal operation. These currents may increase up to 4 I_{IL} if J, K = HIGH and $\bar{S}_D$ = LOW.

9XXX Series

DC CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE: $V_{CC} = +5.0 \pm 10\%$

SYMBOL	PARAMETER	-55°C		25°C		125°C		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
V_{IH}	Input HIGH Voltage	2.0		1.7		1.4		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage	0.8		0.9		0.8		V	Guaranteed Input LOW Threshold
V_{OL}	Output LOW Voltage	0.4		0.4		0.4		V	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 12.4 \text{ mA}$ $V_{CC} = 5.5 \text{ V}$, $I_{OL} = 16 \text{ mA}$
I_{IH}	Input HIGH Current J, $\bar{K}$ Clock Input, $\bar{S}_D$ $\bar{C}_D$			60 120 240		60 120 240		μA	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 4.5 \text{ V}$ Gnd on Other Inputs
I_{IL}	Input LOW Current J, $\bar{K}$ Clock Input, $\bar{S}_D$ $\bar{C}_D$ (Note 4)	-1.6 -3.2 -4.8		-1.6 -3.2 -4.8		-1.6 -3.2 -4.8		mA	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0.4 \text{ V}$ 4.5 V on Other Inputs
	J, $\bar{K}$ Clock Input, $\bar{S}_D$ $\bar{C}_D^*$	-1.24 -2.48 -3.72		-1.24 -2.48 -3.72		-1.24 -2.48 -3.72		mA	$V_{CC} = 4.5 \text{ V}$, $V_{IN} = 0.4 \text{ V}$ 4.5 V on Other Inputs
I_{OS}	Output Short Circuit Current	-30	-100	-30	-100	-30	-100	mA	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 0 \text{ V}$
I_{CC}	Power Supply Current			14				mA	Per Flip-Flop in Worst Logic State

* Denotes maximum current under normal operation. These currents may increase up to 4 I_{IL} if J, K = HIGH and $\bar{S}_D$ = LOW.

SWITCHING CHARACTERISTICS: $T_A = 25^\circ\text{C}$, $V_{CC} = +5.0 \text{ V}$, $C_L = 15 \text{ pF}$

SYMBOL	PARAMETER	9XXX		UNITS	TEST CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CP to Q or $\bar{Q}$		20 33	ns	Figs. 3-1, 3-8
t_h (H) t_h (L)	Hold Time HIGH or LOW J, $\bar{K}$ to CP	0		ns	Figs. 3-1, 3-6
t_s (H) t_s (L)	Setup Time HIGH or LOW J, $\bar{K}$ to CP	20	1.0	ns	
t_{PLH}	Propagation Delay $\bar{S}_D$ to Q, $\bar{C}_D$ to $\bar{Q}$		12	ns	Figs. 3-1, 3-16
t_{PHL}	Propagation Delay $\bar{S}_D$ to $\bar{Q}$, $\bar{C}_D$ to Q		25	ns	
f_{max}	Maximum Toggle Frequency	25		MHz	Figs. 3-1, 3-8