ADC4320/ADC4322/ ADC4325

Very High Speed 16-Bit, Sampling A/D Converters

in a Space-Saving 46-Pin Hybrid Package

Introduction

The ADC4320, ADC4322, and ADC4325 are complete 16-bit, 1 MHz, 2 MHz, and 500 kHz A/D converter subsystems with a built-in sample-and-hold amplifier in a space-saving 46-pin hybrid package. They offer pin-programmable input voltage ranges of ±2.5V, ±5V, ±10V and 0 to +10V, and have been designed for use in applications, such as ATE, digital oscilloscopes, medical imaging, radar, sonar, and analytical instrumentation, requiring high speed and high resolution front ends. The ADC4322 is capable of digitizing a 1 MHz signal at a 2 MHz sampling rate with a guarantee of no missing codes from 0°C to +70°C, or in an extended temperature range version, from –25°C to +85°C. Equally impressive in frequency domain applications, the ADC4325 features 91 dB minimum signal-to-noise ratio with input signals from DC to 100 kHz.

The ADC432X Series utilizes the latest semiconductor technologies to produce a cost-effective, high performance part in a 46-pin hybrid package. They are designed around a two-pass, sub-ranging architecture that integrates a low distortion sample-and-hold amplifier, precision voltage reference, ultra-stable 16-bit linear reference D/A converter, all necessary timing circuitry, and tri-state CMOS/TTL compatible output lines for ease of system integration.

Superior performance and ease-of-use make the ADC432X Series the ideal solution for those applications requiring a sample-and-hold amplifier directly at the input to the A/D converter. Having the S/H amplifier integrated with the A/D converter benefits the system designer in two ways. First, the S/H has been designed specifically to complement the performance of the A/D converter; for example, the acquisition time, hold mode settling and droop rate have been optimized for the A/D converter, resulting in exceptional overall performance. Second, the designer achieves

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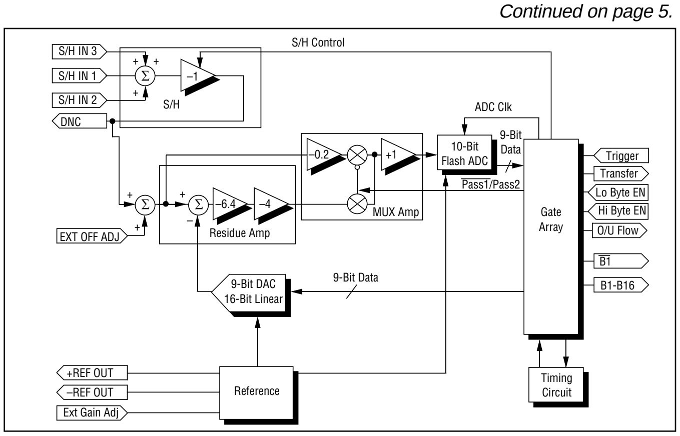


Figure 1. Functional Block Diagram.

Features

- ❑ 2 MHz, 1 MHz, and 500 kHz Conversion Rates
- ❑ 16-Bit Resolution
- ❑ 0.003% Maximum Integral Nonlinearity
- ❑ No Missing Codes
- ❑ Peak Distortion: –92 dB Max. (100 kHz Input)
- ❑ Signal to Noise Ratio:
  86 dB (ADC4322) Min.
  89 dB (ADC4320) Min.
  91 dB (ADC4325) Min.
- ❑ Total Harmonic Distortion:
  (100 kHz Input)
  –86 dB (ADC4320) Max.
  –90 dB (ADC4325) Max.
- ❑ TTL/CMOS Compatibility
- ❑ Low Noise
- ❑ Electromagnetic/Electrostatic Shielding

Applications

- ❑ Digital Signal Processing
- ❑ Sampling Oscilloscopes
- ❑ Automatic Test Equipment
- ❑ High-Resolution Imaging
- ❑ Analytical Instrumentation
- ❑ Medical Instrumentation
- ❑ CCD Detectors
- ❑ IR Imaging
- ❑ Sonar/Radar

ADC4320/ADC4322/ ADC4325

Specifications[1]

SPECIFICATION	ADC4325	ADC4320	ADC4322
ANALOG INPUT			
Input Voltage Range			
Bipolar	±2.5V, ±5V, ±10V	±2.5V, ±5V, ±10V	±2.5V, ±5V, ±10V
Unipolar	0 to +10V	0 to +10V	0 to +10V
Max. Input Without Damage	±15.5V	±15.5V	±15.5V
Input Impedance			
±2.5V	750Ω	750Ω	750 Ω
±5.0V, 0-10V	1.5 KΩ	1.5 KΩ	1.5 KΩ
±10V	3 kΩ	3 kΩ	3 kΩ
Offset/Gain Adj. Sensitivity	300 ppm FSR/V	300 ppm FSR/V	300 ppm FSR/V
DIGITAL INPUTS			
Compatibility	TTL, HCT, and ACT	TTL, HCT, and ACT	TTL, HCT, and ACT
Logic “0”	+0.8V Max.	+0.8V Max.	+0.8V Max.
Logic “1”	+2.0V Min.	+2.0V Min.	+2.0V Min.
Trigger	Negative Edge Triggered	Negative Edge Triggered	Negative Edge Triggered
Loading	2 HCT Loads	2 HCT Loads	2 HCT Loads
TriggerPulse Width	100 ns Min.	100 ns Min.	50 ns Min.
High Byte $\overline{\text{Enable}}$	Active Low, B1-B8, $\overline{\text{B1}}$	Active Low, B1-B8, $\overline{\text{B1}}$	Active Low, B1-B8, $\overline{\text{B1}}$
Low Byte $\overline{\text{Enable}}$	Active Low, B9-B16	Active Low, B9-B16	Active Low, B9-B16
DIGITAL OUTPUTS			
Fan-Out	1 TTL Load	1 TTL Load	1 TTL Load
Logic “0”	+0.4V	+0.4V	+0.4V
Logic “1”	+2.4V	+2.4V	+2.4V
Output Coding	Binary, Offset Binary, Two’s Complement	Binary, Offset Binary, Two’s Complement	Binary, Offset Binary, Two’s Complement
Transfer Pulse	Data valid on positive edge	Data valid on positive edge	Data valid on positive edge
Over/Under Flow	Valid = logic “0” (occurs only when ±FS have been exc’d.)	Valid = logic “0” (occurs only when ±FS have been exc’d)	Valid = logic “0” (occurs only when ±FS have been exc’d)
DYNAMIC CHARACTERISTICS[2]			
Maximum Throughput Rate	500 kHz	1.0 MHz	2.0 MHz
A/D Conversion Time	1.1 µs Typ.	620 ns Typ.	300 ns Typ.
S/H Acquisition Time	900 ns Typ.	380 ns Typ.	200 ns Typ.
S/H Aperture Delay	15 ns Max.	15 ns Max.	15 ns Max.
S/H Aperture Jitter	5 ps RMS Max.	5 ps RMS Max.	5 ps RMS Max.
S/H Feedthrough[3]	–90 dB Max.; –96 dB Typ.	–90 dB Max.; –96 dB Typ.	–90 dB Max.; –96 dB Typ.
Full Power Bandwidth	2.6 MHz Min.	3 MHz Min.	6 MHz Min.
Small Signal Bandwidth	2.6 MHz Min.	6 MHz Min.	8 MHz Min.
Signal to Noise Ratio[4]			
100 kHz Input @ 0 dB	91 dB Min.;93 dB Typ.	89 dB Min.; 92 dB Typ.	86 dB Min.; 88 dB Typ.
495 kHz Input @ –10 dB	–	79 dB Min.; 82 dB Typ.	76 dB Min.; 78 dB Typ.
980 kHz Input @ –10 dB	–	–	75 dB Min.; 78 dB Typ.
Peak Distortion[4]			
100 kHz Input @ 0 dB	–92 dB Max.; –97 dB Typ.	–92 dB Max.; –97 dB Typ.	–92 dB Max.; 97 dB Typ.
495 kHz Input @ –10 dB	–	–84 dB Max.; –95 dB Typ.	–84 dB Max.; –95 dB Typ.
980 kHz Input @ –10 dB	–	–	–81 dB Max.; –88 dB Typ.
Total Harmonic Distortion[4]			
100 kHz Input @ 0 dB	–90 dB Max.; –95 dB Typ.	–86 dB Max.; –94 dB Typ.	–86 dB Max. –94 dB Typ.
495 kHz Input @ –10 dB	–	–79 dB Max.; –86 dB Typ.	–80 dB Max.; –88 dB Typ.
980 kHz Input @ –10 dB	–	–	–80 dB Max.; –85 dB Typ.
THD + Noise[5]			
100 kHz Input @ 0 dB	88 dB Min.; 91 dB Typ.	84 dB Min.; 91 dB Typ.	83 dB Min.; 87 dB Typ.
495 kHz Input @ –10 dB	–	76 dB Min.; 81 dB Typ.	75 dB Min.; 77 dB Typ.
980 kHz Input @ –10 dB	–	–	74 dB Min.; 77dB Typ.

SPECIFICATION (CONT.)	ADC4325	ADC4320	ADC4322
Step Response[6]	800 ns Max. to 1 LSB	500 ns Max. to 1 LSB	250 ns Max. to 2 LSBs
INTERNAL REFERENCE[9]			
Voltage	+5V, ±0.5% Max.	+5V, ±0.5% Max.	+5V, ±0.5% Max.
Stability	15 ppm/°C Max.	15 ppm/°C Max.	15 ppm/°C Max.
Available Current[7]	1.0 mA Max.	1.0 mA Max.	1.0 mA Max.
TRANSFER CHARACTERISTICS			
Resolution	16 bits	16 bits	16 bits
Integral Nonlinearity	±0.003% FSR Max.; ±0.001% Typ.	±0.003% FSR Max.; ±0.001% Typ.	±0.003% FSR Max.; ±0.001% Typ
Differential Nonlinearity	±0.75 LSB; ±0.5 LSB Typ.	±0.75 LSB; ±0.5 LSB Typ.	±0.75 LSB Max.; ±0.5 LSB Typ.
Monotonicity	Guaranteed	Guaranteed	Guaranteed
No Missing Codes	Guaranteed over the Specified Temperature Range	Guaranteed over the Specified Temperature Range	Guaranteed over the Specified Temperature Range
Offset Error	±0.1% FSR Max. (Adj. to Zero)	±0.1% FSR Max. (Adj. to Zero)	±0.1% FSR Max. (Adj. to Zero)
Gain Error	±0.1% FSR Max. (Adj. to Zero)	±0.1% FSR Max. (Adj. to Zero)	±0.1% FSR Max. (Adj. to Zero)
Noise[8]			
10V p-p FSR	55 µV RMS Typ.; 70 µV RMS Max.	65 µV RMS Typ.; 80 µV RMS Max.	90 µV RMS Typ.; 110 µV Max.
5V p-p FSR	45 µV RMS Typ.; 55 µV RMS Max.	50 µV RMS Typ.; 60 µV RMS Max.	65 µV RMS Typ., 80 µV Max.
STABILITY			
Differential Nonlinearity TC	±1 PPM/°C MAX.	±1 PPM/°C MAX	.±1 PPM/°C MAX.
Offset TC	±15 ppm/°C Max.	±15 ppm/°C Max.	±15 ppm/°C Max.
Gain TC	±15 ppm/°C Max.	±15 ppm/°C Max.	±15 ppm/°C Max.
Warm-Up Time	5 Min. Max.	5 Min. Max.	5 Min. Max.
Supply Rejection per % change in any supply Offset & Gain	±10 ppm/% Max.	±10 ppm/% Max.	±10 ppm/% Max.
POWER REQUIREMENTS			
±15V Supplies[9]	14.55V Min., 15.45V Max.	14.55V Min., 15.45V Max.	14.55V Min., 15.45V Max.
+5V Supplies	+4.75V Min., +5.25V Max.	+4.75V Min., +5.25V Max.	+4.75V Min., +5.25V Max.
+15V Current Drain	63 mA Typ.	63 mA Typ.	71 mA Typ.
–15V Current Drain	54 mA Typ.	54 mA Typ.	61 mA Typ.
+5V Current Drain	67 mA Typ.	67 mA Typ.	67 mA Typ.
Total Power Consumption	2.1W Typ.	2.1W Typ.	2.3W Typ.
ENVIRONMENTAL & MECHANICAL			
Specified Temp. Range[10]			
A Version	0°C to +70°C	0°C to +70°C	0°C to +70°C
B Version	–25°C to +85°C	–25°C to +85°C	–25°C to +85°C
Storage Temp. Range	–25°C to 125°C	–25°C to 125°C	–25°C to 125°C
Dimensions	1.58" x 2.38" x 0.225" (40.13 mm x 60.45 mm x 5.7 mm)	1.58" x 2.38" x 0.225" (40.13 mm x 60.45 mm x 5.7 mm)	1.58" x 2.38" x 0.225" (40.13 mm x 60.45 mm x 5.7 mm)
Case Potential	Ground	Ground	Ground

NOTES:

1. All specifications guaranteed at 25°C unless otherwise noted and supplies at ±15V and +5V.
2. All dynamic characteristics measured on the ±5V input range except the 980 kHz distortion test are performed at the ±2.5V input range.
3. Measured with a full scale step input.
4. See performance testing.
5. THD + noise represents the ratio of the RMS value of the signal to the total RMS noise below the Nyquist plus the total harmonic distortion up to the 100th harmonic with an analysis bandwidth of DC to the converters' Nyquist frequency.
6. Step response represents the time required to achieve the specified accuracies after an input full scale step change.
7. Reference Load to remain stable.
8. Includes noise from S/H and A/D converter.
9. Both ±15V analog supply voltages and both ±reference voltages, Pins 2, 3, 16, and 17 must be by-passed with low ESR tantalum capacitors (see Figure 20).
10. The specified temperature range is guaranteed for the case temperature.

Specifications subject to change without notice.

TYPICAL PERFORMANCE CHARACTERISTICS

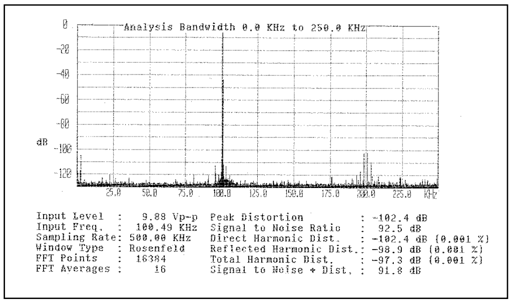


Fig. 2. ADC4325 Dynamic Characteristics at 100 kHz and 0 dB

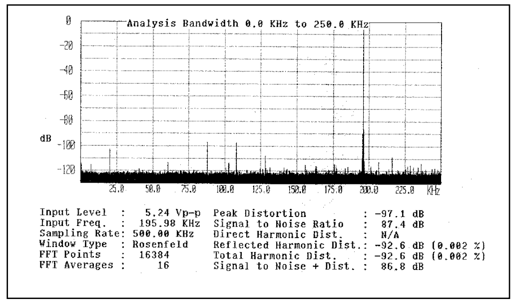


Fig. 6. ADC4325 Dynamic Characteristics at 195 kHz and –6 dB (±5V Range)

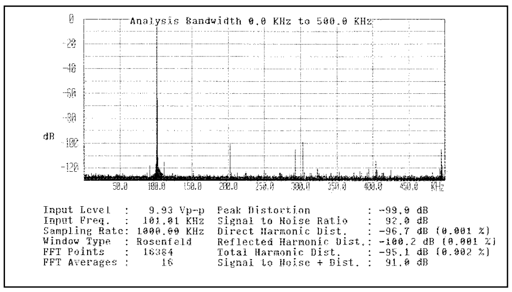


Fig. 3. ADC4320 Dynamic Characteristics at 100 kHz and 0 dB

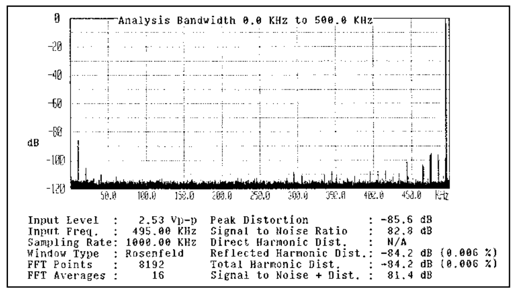


Fig. 7. ADC4320 Dynamic Characteristics at 495 kHz and –6 dB Range.

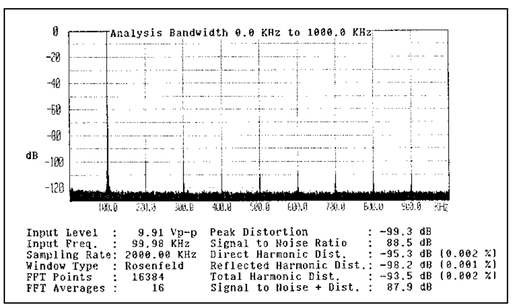


Fig. 4. ADC4322 Dynamic Characteristics at 100 kHz and 0 dB

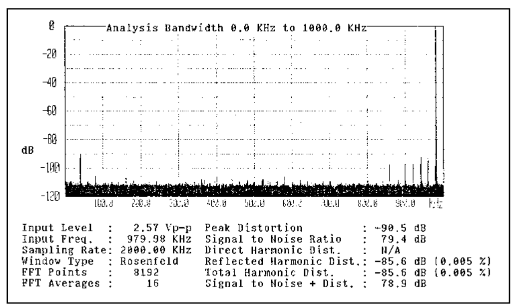


Fig. 8. ADC4322 Dynamic Characteristics at 980 kHz and –6 dB (±2.5V Range)

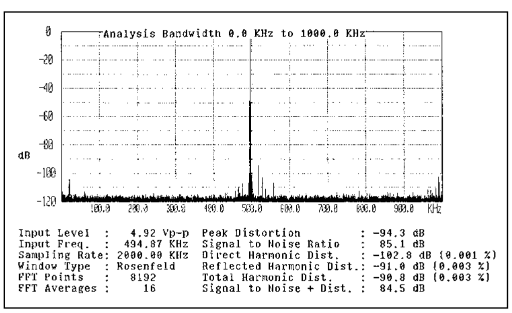


Fig. 5. ADC4322 Dynamic Characteristics at 495 kHz and 0 dB (±2.5V Range)

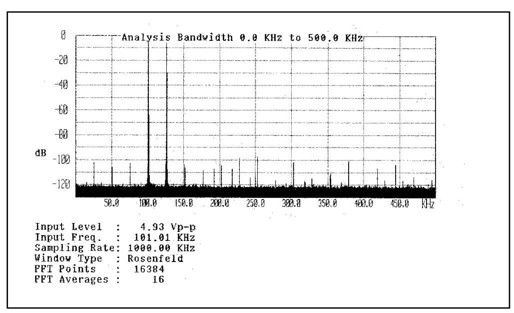


Fig. 9. ADC4320 Intermodulation Distortion at 100 kHz, 125 kHz and –6 dB

SPECIFICATIONS

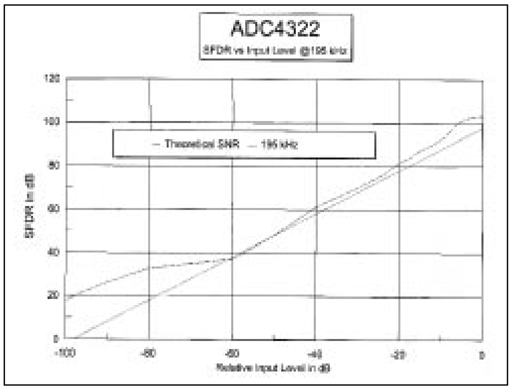


Figure 10. ADC4322 SFDR vs Input Level @ 195 kHz ±2.5V Range

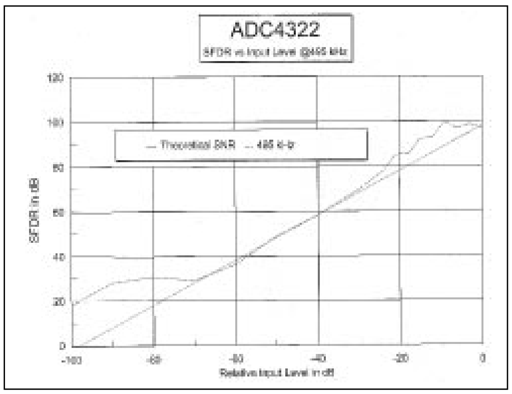


Figure 11. ADC4322 SFDR vs Input Level @ 495 kHz ±2.5V Range

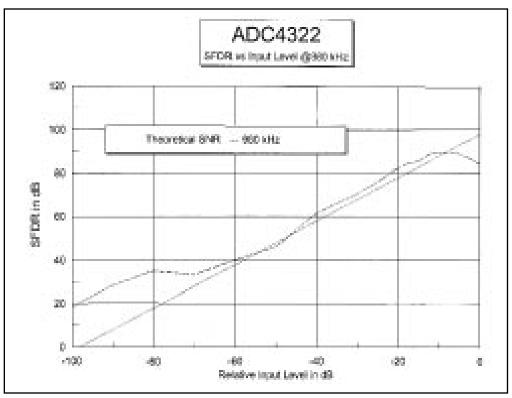


Figure 12. ADC4322 SFDR vs Input Level @ 980 kHz ±2.5V Range

PIN #	4	5	6
RANGE	S/H IN 1	S/H IN2	S/H IN 3
0V to +10V	Input	Input	–5V Ref
±5V	Input	Input	SIG RTN
±2.5V	Input	Input	Input
±10V	Input	SIG RTN	SIG RTN

Figure 13. Input Scaling Connections.

Continued from page 1.

true 16-bit performance, avoiding degradation due to ground loops, signal coupling, jitter and digital noise introduced when separate S/H and A/D converters are interconnected. Furthermore, the accuracy, speed, and quality of the ADC432X Series are fully ensured by thorough, computer-controlled factory tests of each unit.

INTERFACING

Input Scaling

The converters can be configured for four input voltage ranges: 0 to +10V; ±2.5V; ±5V; and ±10V. The analog input range should be scaled as close as possible to the maximum input to utilize the full dynamic range of the converter. Figure 13 describes the input connections.

Coding and Trim Procedure

Figure 15 shows the output coding and trim calibration voltages of the converter. For two's complement operation, simply use the available $\overline{B1}$ $\overline{(MSB)}$ instead of B1 (MSB). Refer to Figure 14 for use of external offset and gain trim potentiometers. Voltage DACs with a ±5V output can be utilized easily when digital control is required. The input sensitivity of the external offset and gain control pins is 300 ppm FSR/V. If Offset and Gain adjusts are not used, connect them to Pin 14, Analog Returns.

To trim the offset of the converter, apply the offset voltage shown in Figure 15 for the appropriate voltage range. Adjust the offset trim potentiometer such that the 15 MSBs are "0" and the LSB alternates equally between "0" and "1" for the unipolar ranges or all 16 bits are in transition for the bipolar ranges.

To trim the gain of the converter, apply the range (+FS) voltage shown in Figure 15 for the appropriate range. Adjust the gain trim potentiometer such that the 15 MSBs are "1" and the LSB alternates equally between "0" and "1".

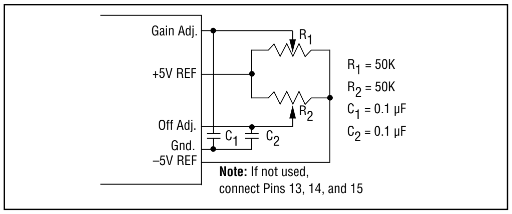


Figure 14. Offset and Gain Adjustment Circuit.

UNIPOLAR BINARY		0V TO +10V	
	MSB LSB		
+FS	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 *	= +9.99977V	
1/2 FS	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	= +5.00000V	
Offset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 *	= +0.00000V	
OFFSET BINARY		**±2.5V Input**	**±5V Input**
	MSB LSB		
+FS	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 *	= +2.49989V	+4.99977V
Offset	* * * * * * * * * * * * * * * *	= –0.00004V	–0.00008V
–FS	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 *	= –2.49996V	–4.99992V
2'S COMPLEMENT		**±2.5V Input**	**±5V Input**
	MSB LSB		
+FS	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 *	= +2.49989V	+4.99977V
Offset	* * * * * * * * * * * * * * * *	= –0.00004V	–0.00008V
–FS	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 *	= –2.49996V	–4.99992V

* denotes a 0/1 or 1/0 transition

Figure 15. Coding and Trim Calibration Table.

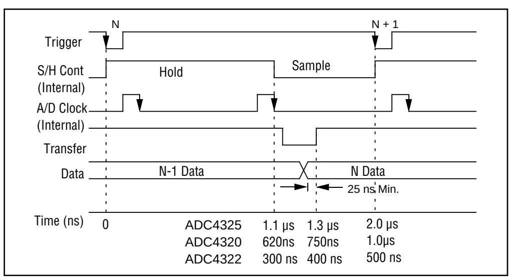


Figure 16. Timing Diagram.

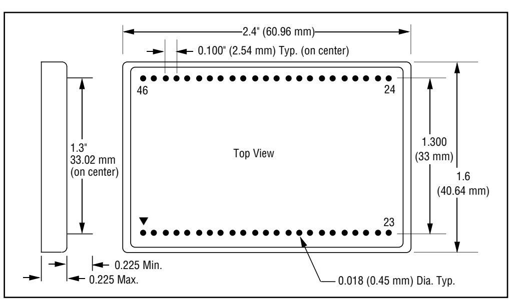


Figure 17. ADC432X Series Mechanical Diagram.

PIN #		PIN#	
1	ANA RTN	46	+5V
2	+15V	45	DIG RTN
3	–15V	44	O/U FLOW
4	S/H IN 1	43	BIT 1N
5	S/H IN 2	42	BIT 1
6	S/H IN 3	41	BIT 2
7	SIG RTN	40	BIT 3
8	DNC*	39	BIT 4
9	ANA RTN	38	BIT 5
10	+15V	37	BIT 6
11	–15V	36	BIT 7
12	DNC	35	BIT 8
13	EXT OFFSET ADJ	34	BIT 9
14	ANA RTN	33	BIT 10
15	EXT GAIN ADJ	32	BIT 11
16	+REF OUT	31	BIT 12
17	–REF OUT	30	BIT 13
18	ANA RTN	29	BIT 14
19	TRIGGER	28	BIT 15
20	DIG RTN	27	BIT 16
21	DIG RTN	26	TRANSFER
22	HI BYTE EN	25	+5V
23	LO BYTE EN	24	DIG RTN

* DNC– Do Not Connect

Figure 18. Pin Assignment.

To check the trim procedure, apply 1/2 full scale voltage for a unipolar range or –full scale voltage for the bipolar ranges and check that the digital code is ±1 LSB of the stated code.

PRINCIPLE OF OPERATION

The ADC432X Series converters are 16-bit sampling A/D converters with throughput rates of up to 2 MHz. These converters are available in three externally configured full scale ranges of 5V p-p, 10V p-p and 20V p-p. Options are externally or user-programmable for bipolar and unipolar inputs of ±2.5V, ±5V, ±10V and 0 to +10V. Two's complement format can be obtained by utilizing $\overline{\text{B1}}$ instead of B1.

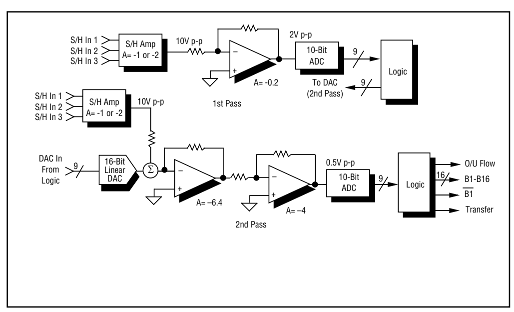


Figure 19. Operating Principle.

To understand the operating principles of the A/D converters, refer to the timing diagram of Figure 16 and the simplified block diagram of Figure 19. The simplified block diagram illustrates the two successive passes in the sub-ranging scheme of the converters.

The A/D converter is factory-trimmed and optimized to operate with a 10V p-p input voltage range. Scaling resistors at the S/H inputs configure the three input ranges and provide a S/H output voltage to the A/D converter of 10V p-p.

The first pass starts with a high-to-low transition of the trigger pulse. This signal places the S/H into the Hold mode and starts the timing logic. The path of the 10V p-p input signal during the first pass is through a 5:1 attenuator circuit to the 10-bit ADC with an input range of 2V p-p. At 35 ns, the ADC converts the signal and the 9 bits are latched both into the logic as the MSBs and into the 16-bit accurate DAC for the second pass.

The second pass subtracts the S/H output and the 9-bit, 16-bit accurate DAC output with the result equal to the 9-bit quantization error of the DAC, or 19.5 mV p-p. The “error” voltage is then amplified by a gain of 25.6 and is now 0.5V p-p or 1/4 the full scale range of the ADC, allowing a 2-bit overlap safety margin. When the DAC and the “error” amplifier have had sufficient time to settle to 16-bit accuracy, the amplified “error” voltage is then digitized by the ADC with the 9-bit second pass result latched into the logic. At this time the S/H returns to the sample mode to begin acquiring the next sample.

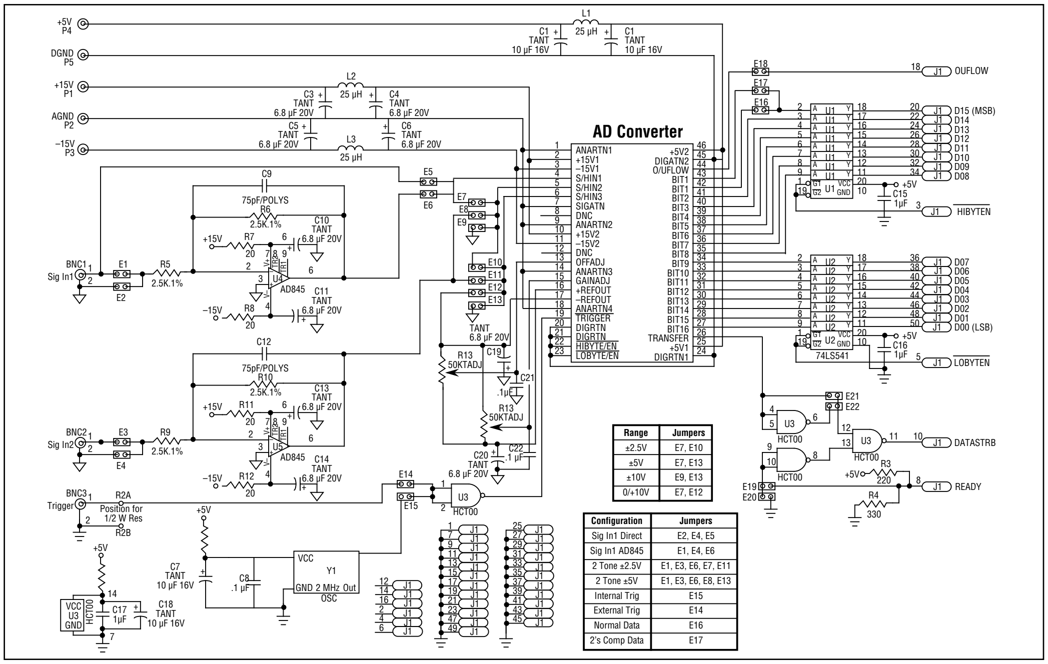
The 1/4 full scale range in the second pass produces a 2-bit overlap of the two passes. This provides an output word that is accurate and linear to 16 bits. This method corrects for any gain and linearity errors in the amplifying circuitry, as well as the 10-bit flash A/D converter. Without the use of this overlapping correction scheme, it would be necessary that all the components in the converters be accurate to the 16-bit level. While such a design might be possible to realize on a laboratory benchtop, it would be clearly impractical to achieve on a production basis. The key to the conversion technique used in the converters is the 16-bit accurate and 16-bit linear D/A converter which serves as the reference element for the conversion’s second pass. The use of proprietary sub-ranging architecture in the converters results in a sampling A/D converter that offers unprecedented speed and transfer characteristics at the 16-bit level.

The converter has a 3-state output structure. Users can enable the eight MSBs and B1 with $\overline{\text{HIBYTEN}}$ and the eight LSBs with $\overline{\text{LOBYTEN}}$ (both are active low). This feature makes it possible to transfer data from the converter to an 8-bit microprocessor bus. However, to prevent the coupling of high frequency noise from the microprocessor bus into the A/D converter, the output data must be buffered.

Layout Considerations

Because of the high resolution of the A/D converters, it is necessary to pay careful attention to the printed-circuit layout for the device. It is, for example, important to keep analog and digital grounds separate at the power supplies. Digital grounds are often noisy or “glitchy,” and these glitches can have adverse effects on the performance of the converters if they are introduced to the analog portions of the A/D converter’s circuitry. At 16-bit resolution, the size of the voltage step between one code transition and the succeeding one for a 5V full scale range is only 76 µV. It is evident that any noise in the analog ground return can result in erroneous or missing codes. It is important in the design of the PC board to configure a low-impedance ground-plane return on the printed-circuit board. It is only at this point where the analog and digital power returns should be made common.

The Analogic ADC4322 EB-1 evaluation board has been designed and laid out for optimum performance with the converter series. The board layout and schematic are shown in figures 20-22 as examples of decoupling and layout techniques.



Range	Jumpers
±2.5V	E7, E10
±5V	E7, E13
±10V	E9, E13
0/+10V	E7, E12

Configuration	Jumpers
Sig In1 Direct	E2, E4, E5
Sig In1 AD845	E1, E4, E6
2 Tone ±2.5V	E1, E3, E6, E7, E11
2 Tone ±5V	E1, E3, E6, E8, E13
Internal Trig	E15
External Trig	E14
Normal Data	E16
2's Comp Data	E17

Figure 20. ADC4322-EB1 Block Diagram

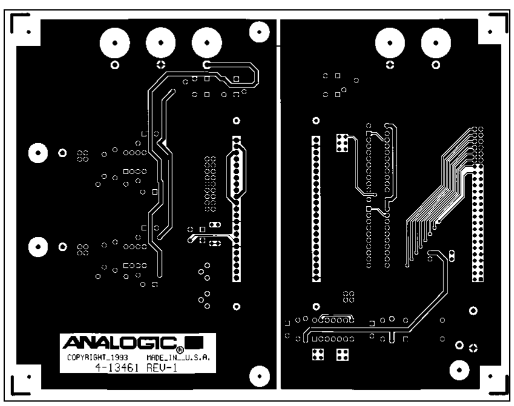


Figure 21. Primary Side

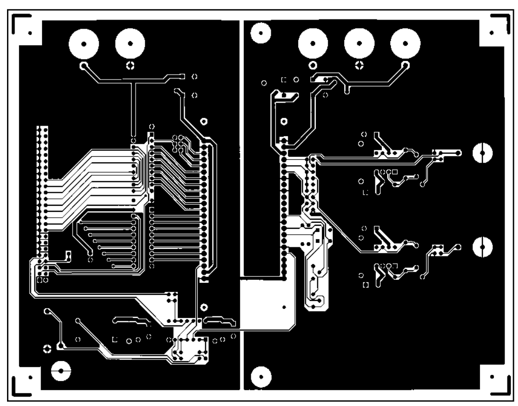


Figure 22. Secondary Side

Ordering Guide

Model	Sampling Rate
Specified Temperature Range: 0°C to +70°C	
ADC4325A	500 kHz
ADC4320A	1 MHz
ADC4322A	2 MHz
Specified Temperature Range: –25°C to +85°C	
ADC4325B	500 kHz
ADC4320B	1 MHz
ADC4322B	2 MHz
Evaluation Board	
ADC4322 EB-1	