ALPHA & OMEGA SEMICONDUCTOR, LTD

AO4447AL
P-Channel Enhancement Mode Field Effect Transistor

General Description

The AO4447AL uses advanced trench technology to provide excellent $R_{DS(ON)}$ with low gate charge.This device is ideal for load switch and battery protection applications.

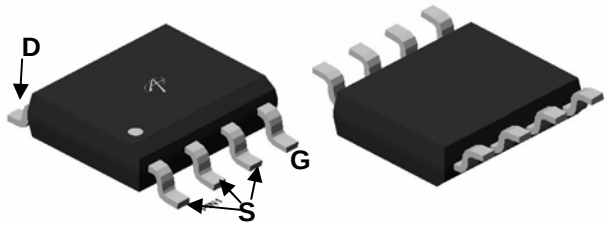
-RoHS Compliant
-Halogen Free

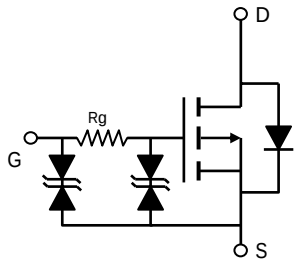
Features

V_{DS} (V) = -30V
I_D = -17A (V_{GS} = -10V)
$R_{DS(ON)}$ < 7mΩ (V_{GS} = -10V)
$R_{DS(ON)}$ < 8mΩ (V_{GS} = -4.5V)
$R_{DS(ON)}$ < 9mΩ (V_{GS} = -4V)

ESD Protected!

SOIC-8





Absolute Maximum Ratings T_J=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A=25°C	I_D	-17	A
	T_A=70°C		-13	
Pulsed Drain Current [C]		I_{DM}	-160	
Power Dissipation [B]	T_A=25°C	P_D	3.1	W
	T_A=70°C		2.0	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	31	40	°C/W
Maximum Junction-to-Ambient [AD]	Steady State		59	75	°C/W
Maximum Junction-to-Lead	Steady State	$R_{\theta JL}$	16	24	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D =-250µA, V_{GS} = 0V	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =-30V, V_{GS} = 0V			-1	µA
		T_J = 55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS} = 0V, V_{GS} =±16V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} =V_{GS} I_D =-250µA	-0.8	-1.3	-1.6	V
$I_{D(ON)}$	On state drain current	V_{GS} =-10V, V_{DS} =-5V	-160			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} =-10V, I_D =-17A		5.5	7	mΩ
		T_J=125°C		7	8.5	
		V_{GS} =-4.5V, I_D =-15A		6.5	8	
		V_{GS} =-4V, I_D =-13A		6.9	9	
g_{FS}	Forward Transconductance	V_{DS} =-5V, I_D =-17A		70		S
V_{SD}	Diode Forward Voltage	I_S =-1A,V_{GS} = 0V		-0.62	-1	V
I_S	Maximum Body-Diode Continuous Current				-3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz		4580	5500	pF
C_{oss}	Output Capacitance			755		pF
C_{rss}	Reverse Transfer Capacitance			564		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		160	210	Ω
SWITCHING PARAMETERS						
Q_g (-10V)	Total Gate Charge	V_{GS}=-10V, V_{DS}=-15V, I_D=-17A		87	105	nC
Q_g (-4.5V)	Total Gate Charge			41		nC
Q_{gs}	Gate Source Charge			12.8		nC
Q_{gd}	Gate Drain Charge			17		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-15V, R_L=-0.9Ω, R_{GEN}=3Ω		180		ns
t_r	Turn-On Rise Time			260		ns
$t_{D(off)}$	Turn-Off DelayTime			1.2		µs
t_f	Turn-Off Fall Time			9.7		µs
t_{rr}	Body Diode Reverse Recovery Time	I_F=-17A, dI/dt=300A/µs		32	40	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-17A, dI/dt=300A/µs		77		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

Rev 0: Aug 2008

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

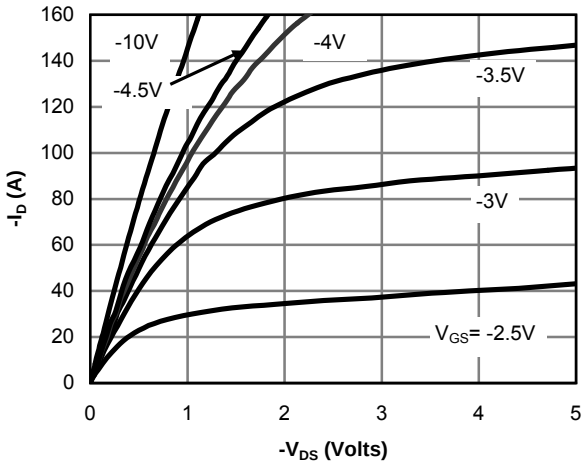


Figure 1: On-Region Characteristics(Note E)

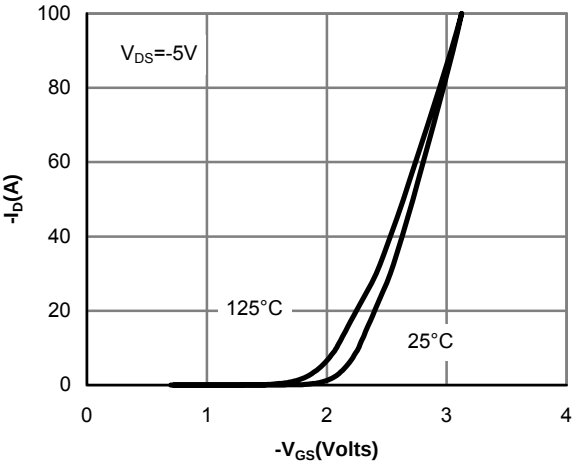


Figure 2: Transfer Characteristics(Note E)

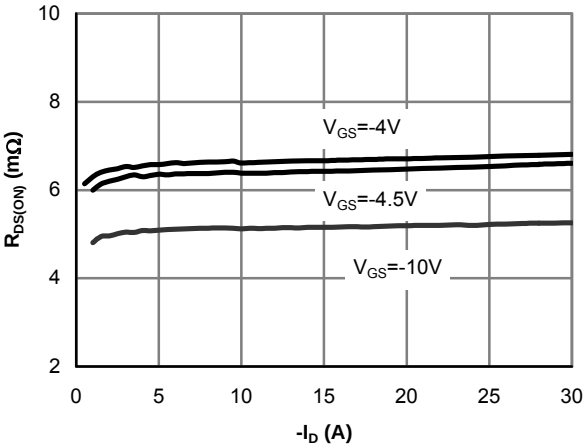


Figure 3: On-Resistance vs. Drain Current and Gate Voltage(Note E)

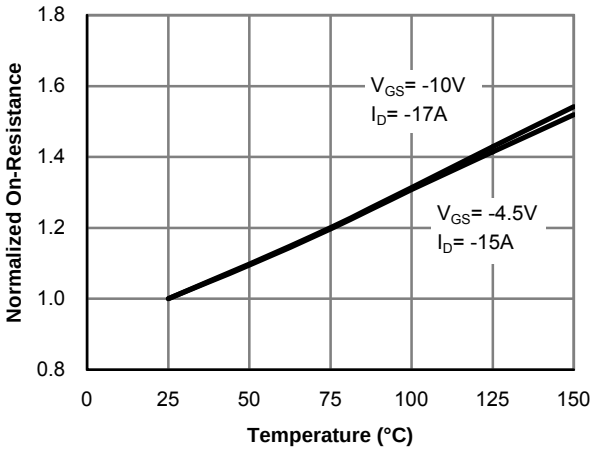


Figure 4: On-Resistance vs. Junction Temperature(Note E)

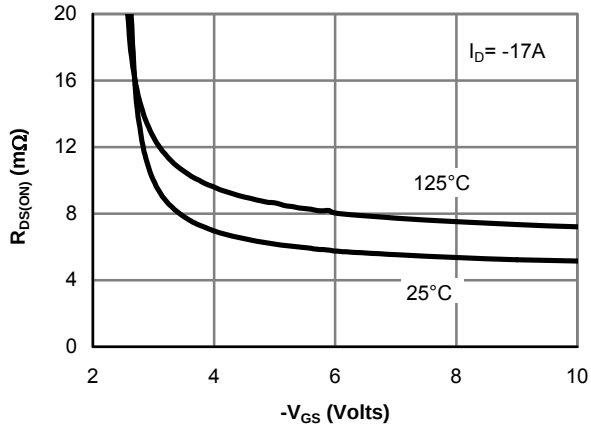


Figure 5: On-Resistance vs. Gate-Source Voltage(Note E)

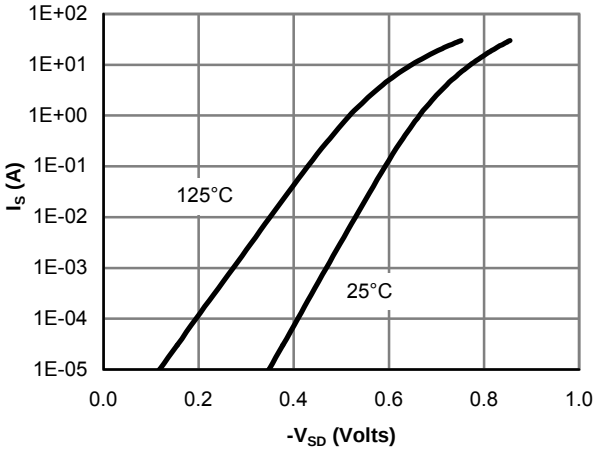


Figure 6: Body-Diode Characteristics(Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

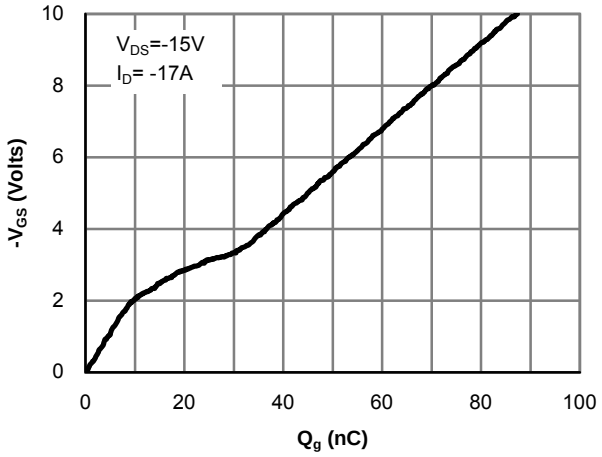


Figure 7: Gate-Charge Characteristics

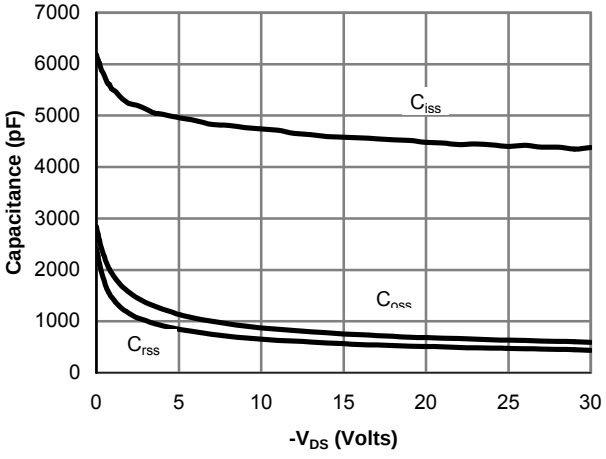


Figure 8: Capacitance Characteristics

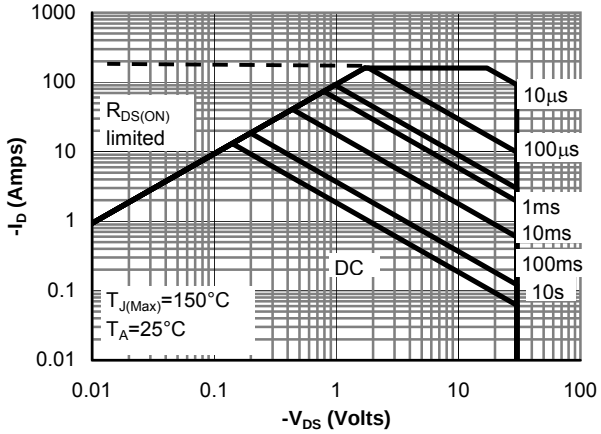


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

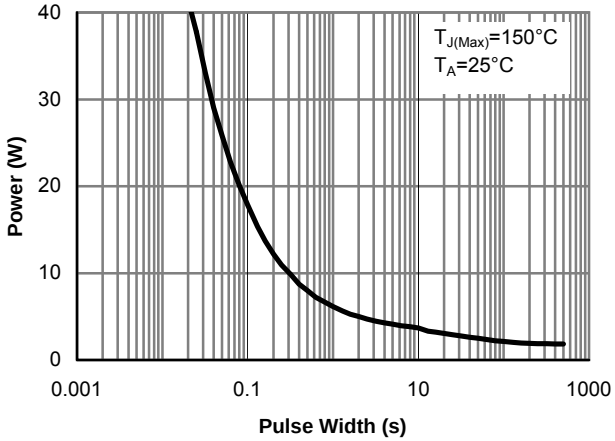


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

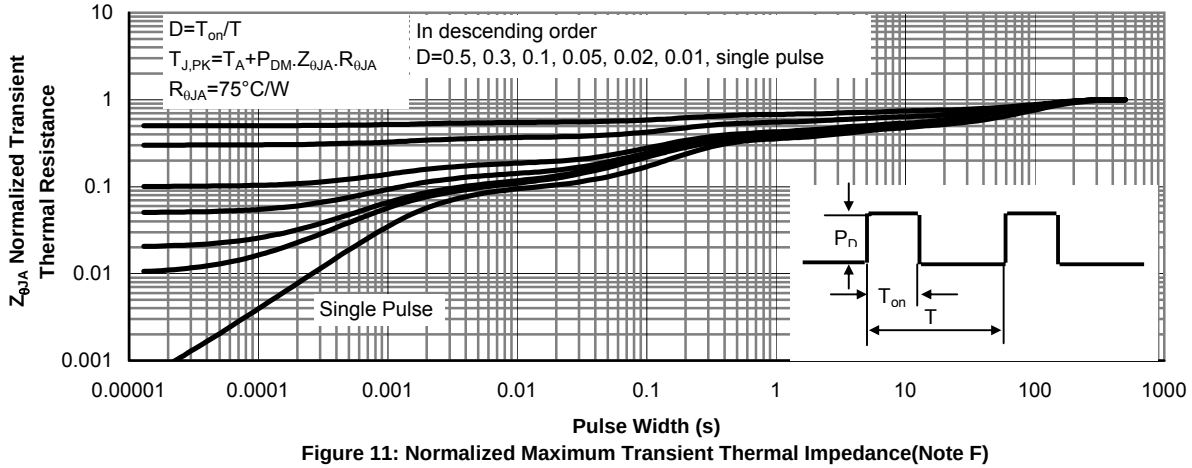
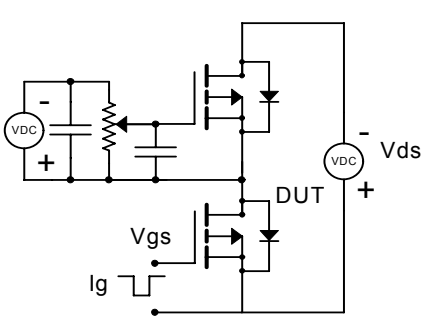
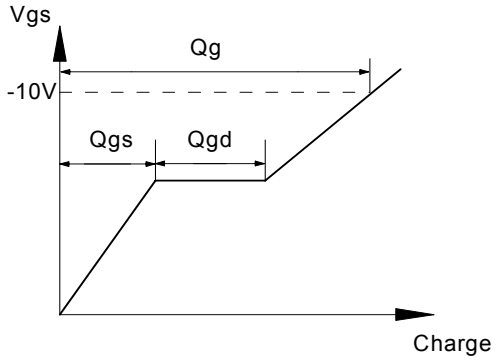


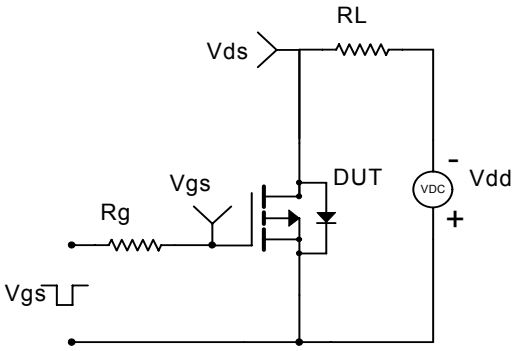
Figure 11: Normalized Maximum Transient Thermal Impedance(Note F)

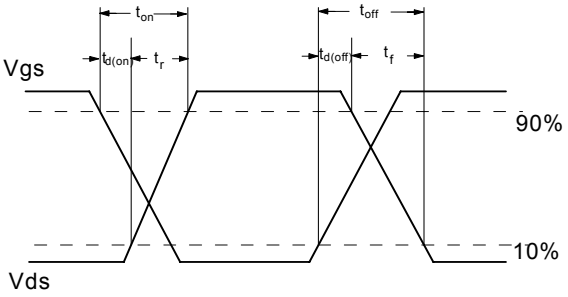
Gate Charge Test Circuit & Waveform





Resistive Switching Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms