# Agilent HPFC-5100, HPFC-5166 Tachyon TL/TS Mass Storage Fibre Channel ICs

## Product Brief


### Description

The Tachyon TL (HPFC-5100) and the Tachyon TS (HPFC-5166) are high-performance PCI native Fibre Channel (FC) controllers. They are collectively known as TL/TS. TL/TS focuses on mass storage applications for any topology that requires Class 3 and Class 2 (via software) and SCSI upper layer protocol handling. The 32/64-bit PCI bus interface provides a cost-effective high-performance mass storage solution. TL/TS carries forward the assurance of interoperability and true Fibre Channel performance. Also, TL/TS advances the Tachyon architecture as a complete hardware-based design in a single chip FC solution. No additional onboard microprocessor is required. Thus, this architecture avoids reduced performance issues related to processor cycles per second and access time to firmware.

### Tachyon TL-Specific Features

- 33 MHz, 32/64-bit PCI interface (compliant to PCI Local Bus Specification, Revision 2.1)
- Optional External Memory Interface: 32-bit at 33 MHz for 132 MBytes/sec

### Tachyon TS-Specific Features

- 66 MHz, 32/64-bit PCI Interface
- Optional External Memory Interface: 32-bit at 66 MHz for 264 MBytes/sec

### Applications

The Tachyon TL/TS is targeted for the following applications:

- Fast/Wide SCSI replacement as a Class 3 loop initiator on FC-AL to connect to the following devices: scanners, disk, tape and CD ROM drives
- Class 3 loop target as a host connection for a mass storage subsystem
- Low-cost direct point-to-point FC connection between an initiator and target (host-based adapter)
- Low-cost shared mass storage on FC-AL

### Features

- **1-gigabaud (1062.5 megabaud) link speed**
- **Supports Class 3 and Class 2 (ACK_0 model)**
- **Supports Fibre Channel Arbitrated Loop (FC-AL), public and private**
- **Supports point-to-point and fabric topologies**
- **Hardware assists for Fibre Channel Protocol for SCSI (FCP)**
- **Fully assisted Class 3 FCP with simultaneous initiator and target functionality**
- **Glueless interface to low-cost, 10-bit, 1-gigabaud transceivers (SERDES)**
- **Complete FCP sequence segmentation and reassembly in hardware**
- **Local 32-bit synchronous static RAM memory option**
- **Support of up to a 1024-byte frame size**
- **Industry standard 32-bit/64-Bit PCI backplane: TL, 0-33 MHz; TS, 16-66 MHz**
- **Loop Map, Loop Broadcast, Loop Directed Reset, and Loop Bypass Support**
- **TL/TS is a Little Endian Device (note that the PCI bus is Little Endian and Fibre Channel is Big Endian)**
- **16-entry inbound FCP cache support**

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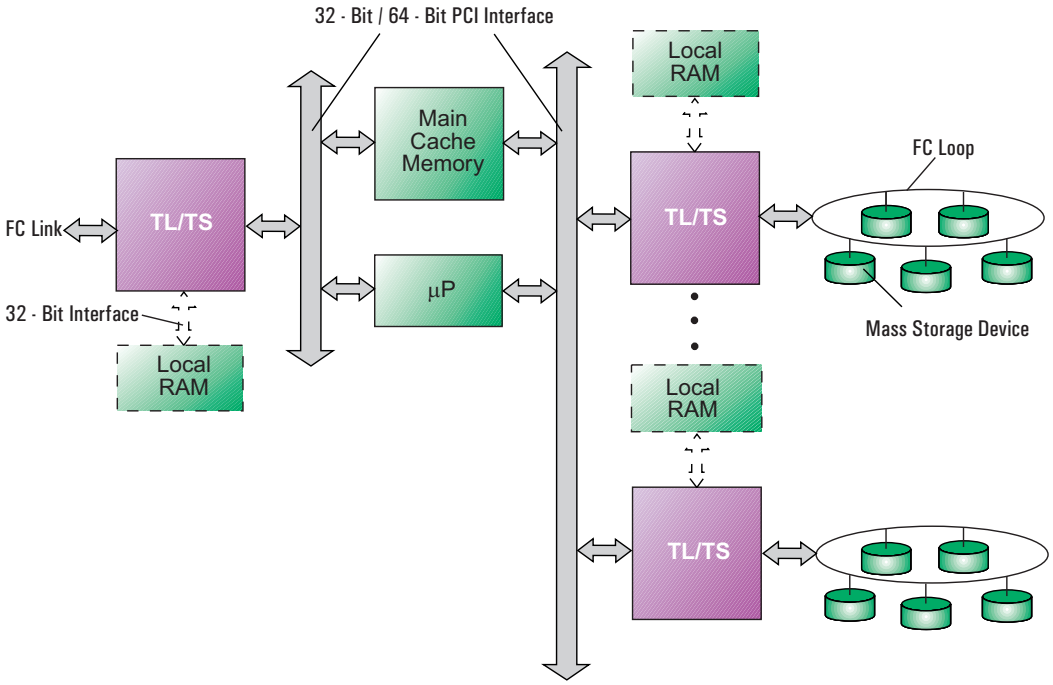


**Typical Subsystem Application**
The figure above shows a TL/TS chip in a typical subsystem application. The TL/TS chip, shown on the left in the diagram, interfaces between the host system and the main memory of the subsystem. The other two TL/TS chips interface between the main memory of the subsystem and the mass storage devices on the Fibre Channel loops.

Optional components include local synchronous static RAM that each TL/TS chip can use to access its own control structures, which reduces transactions on the shared PCI bus and main memory.

## Specifications

### FCP (SCSI) Features

- Byte level addressability on both inbound and outbound data buffers
- I/O Request Queue consists of up to 8,000 commands
- Simultaneous initiator and target mode
- Supports up to 32,767 concurrent SCSI transactions

### PCI Features

- Burst transfer rate
  TL: 264 MBytes/sec (64-Bit at 33 MHz)
  TS: 528 MBytes/sec (64-Bit at 66 MHz)
- 32-bit or 64-bit selectable, 0–66 MHz PCI backplane
- Voltage: 3.3 V, 5 V tolerant
- Dual address cycle support
- Advanced configuration and power interface; Hot plug PCI capable

### Other Features

- Flash ROM support: Boot BIOS and Subsystem Vendor ID
- For test and debug: JTAG and full internal scan support; Link Status pins; and user definable signal pin
- Parity protection on all data paths at byte level
- PCI control overhead reduced through use of local memory option
- 128 KBytes or 256 KBytes of synchronous static RAM for optional low latency control access
- Packaging
  TL: 272-pin Plastic Ball Grid Array (PBGA +)
  TS: 388-pin Plastic Ball Grid Array (PBGA)
- 16-entry on-chip cache for low latency context save and restore, and expensive pipelining techniques
- 44/45 bits per Length/Address Pair (L/A Pair)
- Zero wait states asserted by TL/TS as the bus master
- Ability to insert transactions at head of outbound queue (ERQ) for error recovery or priority adjustment



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Data subject to change.

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